8K

D&N Micro Products

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46815

96 PROTO
DAN MICRO PRODUCTS
A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11
12

CIRCUIT DESCRIPTION

The D&N Micro Products' memory board is an 8K bit static RAM system. The input and output bus is a 48 pin system using Molex type KK-156 connectors. The pinouts are compatible with the OSI® 48 pin bus system. The board can use 2102 type memory chips of any power level and any access time. The 8K memory board has several features: Write protect in two independent 4K blocks, two independently addressable 4K blocks, wait signal for slow memory usage with a fast system clock, and multiple board selection using a PIA.

ADDRESS DECODING

The 8K memory board is addressable in two independent 4K blocks. Dip switches 1 through 4 are used for block A and switches 5 through 8 for block B. Address decoding is accomplished by U8 and U7, 74LS86's EXCLUSIVE-OR gates and U5 74LS20 NAND gate. When the address switches are open U8 and U7 act as invertors, when closed as a non-invertor. This allows all 16 combinations of address lines A15 to A12 to be applied to U5. When the four inputs of U5 are high, the output goes low enabling the memory board. Address lines A11 and A10 are applied to a 74LS139 U3, a one of four decoder. U3 is enabled by the block address and Ø2·VMA. The output of U3 applies the Chip Enable signal to one of four 1K memory blocks. Address lines A0 through A9 are always applied to the memory chips. With the Chip Enable line low, the 2102 memories are ready to receive or send data.

In a very large memory system, up to 4 boards may reside at the same address. This is accomplished by the use of address lines A16 and A17. These address lines can be controlled by a PIA to select one of four boards. Jumper points E1 through E12 can be set to decode the PIA signal. Points E1 through E12 may also be set to have block A and B at the same address.

ADDRESS SELECTION

Do not set block A and B to the same address unless optional address lines A16 and A17 will be used.

BLOCK				
A	S1	S2	S3	S4
B	S5	S6	S7	S8
ADDRESS				
0xxx	off	off	off	off
1xxx	on	off	off	off
A — 2xxx	off	on	off	off
B — 3xxx	on	on	off	off
4xxx	off	off	on	off
5xxx	on	off	on	off
6xxx	off	on	on	off
7xxx	on	on	on	off
8xxx	off	off	off	on
9xxx	on	off	off	on
Axxx	off	on	off	on
Bxxx	on	on	off	on
Cxxx	off	off	on	on
Dxxx	on	off	on	on
Exxx	off	on	on	on
Fxxx	on	on	on	on

TABLE 1

Normal 8K memory board usage does not require any of the following changes. If memory expansion lines A15 and A17 are used, insert a 74LS139 at U4. Cut the P.C. runs from E7 to E12 and E6 to E11. Add jumper wires from E11 and E12 to the correct points for the address desired.

MEMORY EXPANSION ADDRESS		BLOCK A	BLOCK B
A16	A17	Jumper from E11 to	Jumper from E12 to
L	L	E7	E4
H	L	E9	E2
L	H	E8	E3
H	H	E10	E1

TABLE 2

DATA INPUT/OUTPUT

The 8K memory board is interfaced to the system by 8T26s U9 and U10. The 8T26 bi-directional transceivers buffer the data bus and split it into two unidirectional signals. These signals go to the data inputs and outputs of the 2102 memory chips. The 8T26s normally pass data from the system bus to the data inputs of the 2102s. When the board is enabled, Ø2·VMA is high and Read Write line is high, the 8T26s change direction and pass data from the memories to the system bus. When the board is enabled, Ø2·VMA is high and Read Write line is low, data from the bus is written into the memory chips.

Data written into memory may be protected by installing the optional switches at S9 and S10. By closing these switches, further writing into memory is prohibited. The write protect lines may also be brought to unused pins on the system bus and controlled by a PIA.

CONSTRUCTION NOTES

For those purchasing the 8K memory kit, following the assembly instructions carefully will result in highly stable and dependable performance.

CAUTION: The memory chips and bi-directional bus drivers supplied with this kit are MOS (Metal Oxide Silicon) technology devices and may be damaged or destroyed if accidentally exposed to high voltage levels. Static electricity is the least obvious and therefore most dangerous to these devices. Make sure that all test equipment and soldering irons are properly grounded.

All soldering should be done with a pencil tip iron of only 15 to 25 watts.

ASSEMBLY INSTRUCTIONS

( ) Lay out all parts except the 21L02 memory chips and the 8T26 bus drivers. Leave these devices in the anti-static tubes.

( ) Install sixty-four 16 Pin I.C. sockets in the 21L02 memory locations.

( ) Install three 16 Pin I.C. sockets at U10, U9 and U3 locations.

( ) Install six 14 Pin I.C. sockets at Locations U1, U2, U6, U5, U7, and U8.

( ) Install 28 .1 mfd disc capacitors at all locations marked C.

( ) Install ten 4.7K 1/4 watt resistors at R1 through R10.

( ) Install IN914 diode at D2, data direction diode.

( ) Install 8 position dip switch at S1-S8 position.

( ) Install four Molex connectors at board edge.

( ) Using an Ohm Meter, check for solder bridges between any edge connector pins and address lines circuit runs.

( ) Using an Ohm Meter, check for solder bridges on lines leading to and from U10 and U9.

( ) Install sixty-four 21L02A memory chips in sockets.

( ) Install remaining I.C.s per parts list.

( ) Select board address per Table 1.

The 8K memory board is now complete and ready for installation into your system.

PARTS LIST

QUANTITY	#	DESCRIPTION
10	R1-10	4.7K, 5% 1/4 watt resistor
28	C	.1mfd ceramic capacitor
2	D1-2	1N914 Diode
1	U1	SN74LS00
1	U2	SN74LS04
1	U5	SN74LS20
1	U6	SN74LS27
2	U7-8	SN74LS86
2*	U3-4	SN74LS139
2	U10-11	8T26
64		21L02
1	S1-8	SPST dip switch
68		16 Pin I.C. socket
6		14 Pin I.C. socket
2	S9-10	SPST Switch (Write protect opt.)
4		Molex type KK-156 connector

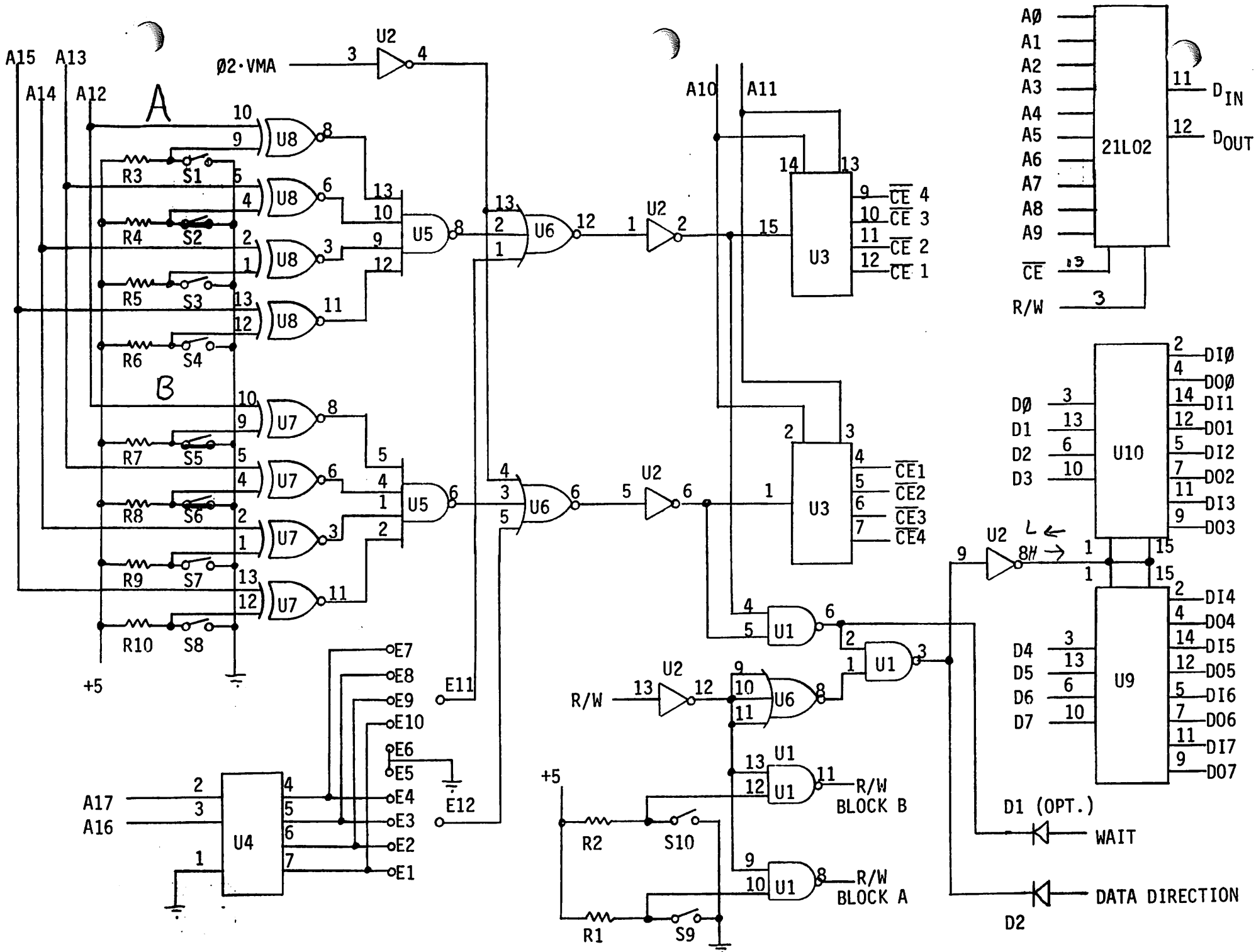
*U4 used with Address Lines A16, A17.

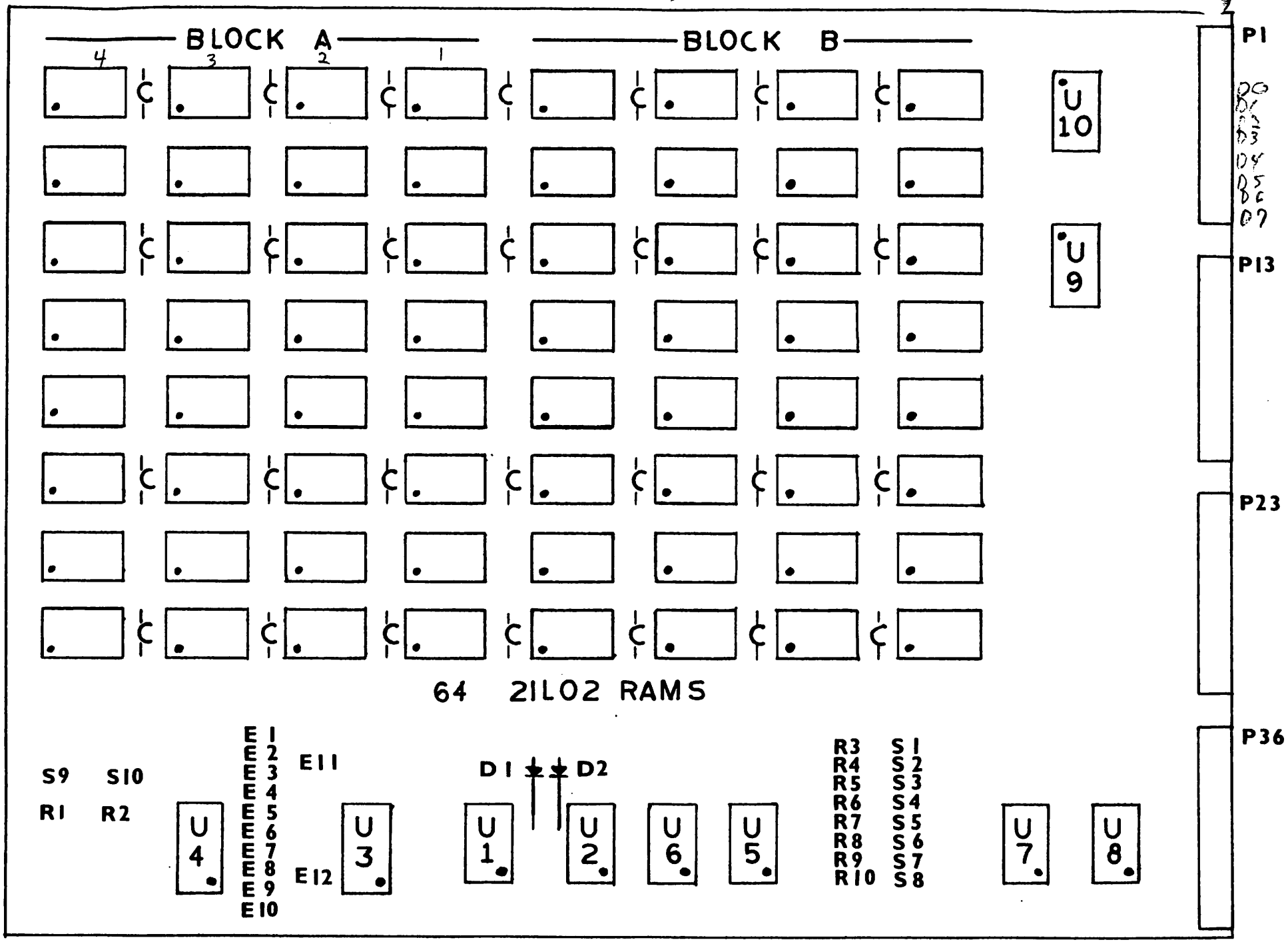
48 PIN SYSTEM BUS PINOUT

P1	Wait (optional)	P25	+5 Volts
P2	NC	P26	+5 Volts
P3	NC	P27	Ground
P4	Data Direction	P28	Ground
P5	DØ	P29	A6
P6	D1	P30	A7
P7	D2	P31	A5
P8	D3	P32	A8
P9	D4	P33	A9
P10	D5	P34	A1
P11	D6	P35	A2

P12	D7
P13	NC
P14	NC
P15	NC
P16	NC
P17	NC
P18	NC
P19	NC
P20	NC
P21	A17
P22	A16
P23	NC
P24	NC

P36	A3
P37	A4
P38	AØ
P39	NC
P40	R/W
P41	NC
P42	Ø2-VMA
P43	A1Ø
P44	A11
P45	A12
P46	A13
P47	A14
P48	A15


A15
A13
A14
A12
A
B
Ø2·VMA
U2
U8
U7
U5
U6
U3
U1
U4
U10
U9
R3
S1
R4
S2
R5
S3
R6
S4
R7
S5
R8
S6
R9
S7
R10
S8
+5
A10
A11
CE 4
CE 3
CE 2
CE 1
CE1
CE2
CE3
CE4
R/W
E7
E8
E9
E10
E6
E5
E4
E3
E2
E1
E11
E12
A17
A16
R2
S10
R1
S9
R/W BLOCK B
R/W BLOCK A
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
21L02
D IN
D OUT
CE
R/W
DI0
DO0
DI1
DO1
DI2
DO2
DI3
DO3
DI4
DO4
DI5
DO5
DI6
DO6
DI7
DO7
D0
D1
D2
D3
D4
D5
D6
D7
8H
L
D1 (OPT.)
WAIT
DATA DIRECTION
D2
CLOSE S10 or S9 for write protect


BLOCK A
BLOCK B
4
3
2
1
U 10
U 9
P1
P13
P23
P36
64 2IL02 RAMS
S9 S10
R1 R2
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10
E11
E12
U 4
U 3
D1 D2
U 1
U 2
U 6
U 5
R3 S1
R4 S2
R5 S3
R6 S4
R7 S5
R8 S6
R9 S7
R10 S8
U 7
U 8