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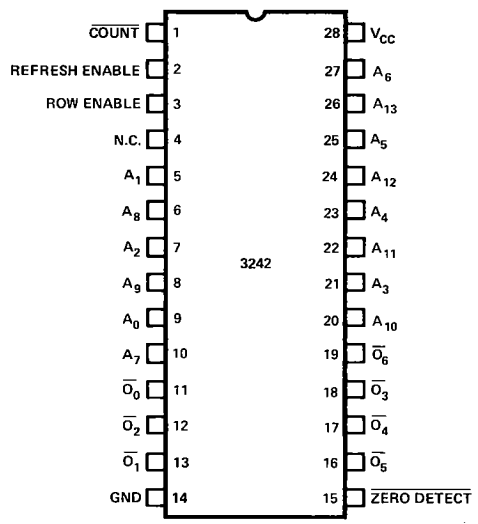
3242
ADDRESS MULTIPLEXER AND REFRESH COUNTER FOR 16K DYNAMIC RAMs

- **Ideal For 2116**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 28-Pin DIP**
- **Suitable For Either Distributed Or Burst Refresh**
- **Single Power Supply: +5 Volts ±10%**
- **Address Input to Output Delay: 9ns Driving 15 pF, 25ns Driving 250pF**

The Intel® 3242 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of 64 or 128 cycles. It multiplexes 14 bits of system supplied address to 7 output address pins. The device also contains a 7 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3242 makes it especially suitable for use with high speed N-channel RAMs like the 2116.

The 3242 operates from a single +5 volt power supply and is specified for operation over a 0 to +75° C ambient temperature range. It is fabricated by means of Intel's highly reliable Schottky bipolar process and is packaged in a hermetically sealed 28 pin Type D package.

PIN CONFIGURATION



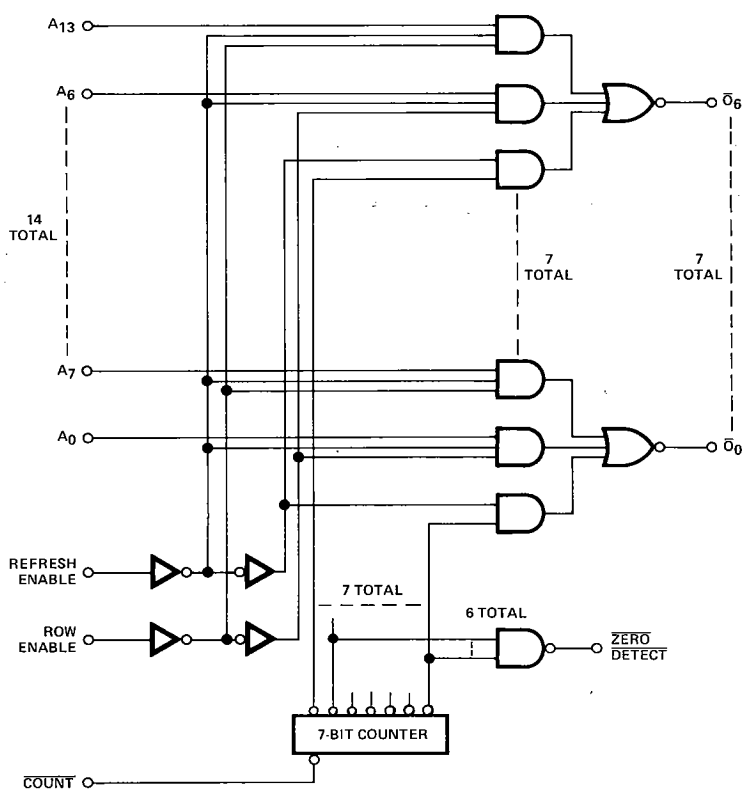
NOTE: A_0 THROUGH A_6 ARE ROW ADDRESSES.
A_7 THROUGH A_{13} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_6)
L	L	COLUMN ADDRESS (A_7 THROUGH A_{13})

$\overline{\text{COUNT}}$ – ADVANCES INTERNAL REFRESH COUNTER.
$\overline{\text{ZERO DETECT}}$ – INDICATES ZERO IN THE FIRST 6 SIGNIFICANT REFRESH COUNTER BITS (USED IN BURST REFRESH MODE)

LOGIC DIAGRAM



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Absolute Maximum Ratings*

Temperature Under Bias ..... -10° to +85°C
Storage Temperature ..... -65° to +150°C
All Input, Output, or
Supply Voltages .....-0.5V to +7 Volts
Output Currents 100mA
Power Dissipation 1W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

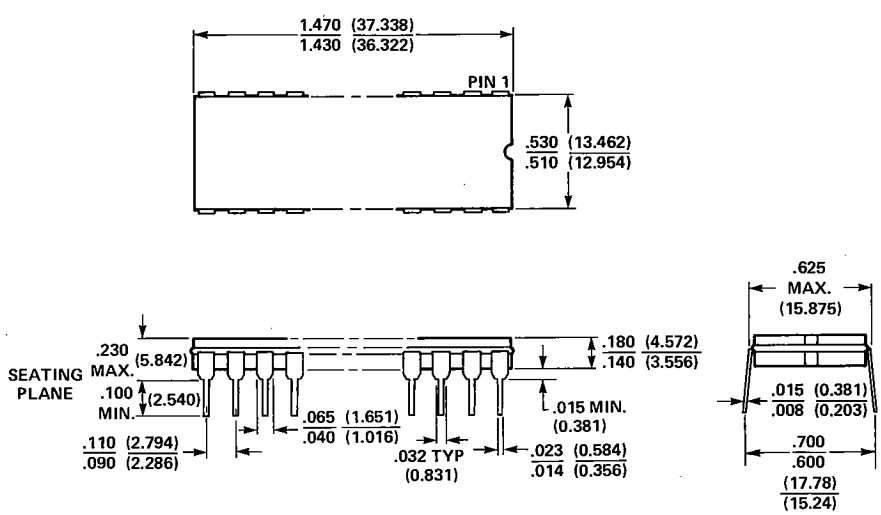
All Limits Apply for V_{CC} = 5.0V ±10%, T_A = 0°C to + 75°C

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. (1)	MAX.		
I_F	Input Load Current		-0.04	-0.25	mA	V_{IN} = 0.45V, Note 2
I_R	Input Leakage Current		0.01	10	μA	V_{IN} = 5.5V
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OL}	Output Low Voltage		0.25	0.40	V	I_{OL} = 8mA
V_{OH}	Output High Voltage ($\overline{O}_0$-$\overline{O}_6$)	3.0	4.0		V	I_{OH} = −1mA
V_{OH1}	Output High Voltage ($\overline{Zero\ Detect}$)	2.4	3.3		V	I_{OH} = −1mA
I_{CC}	Power Supply Current		105	165	mA	V_{CC} = 5.5V

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Inputs are high impedance, TTL compatible, and suitable for bus operation.

Packaging Information

28 LEAD HERMETIC DUAL IN-LINE PACKAGE
TYPE D



A.C. Characteristics

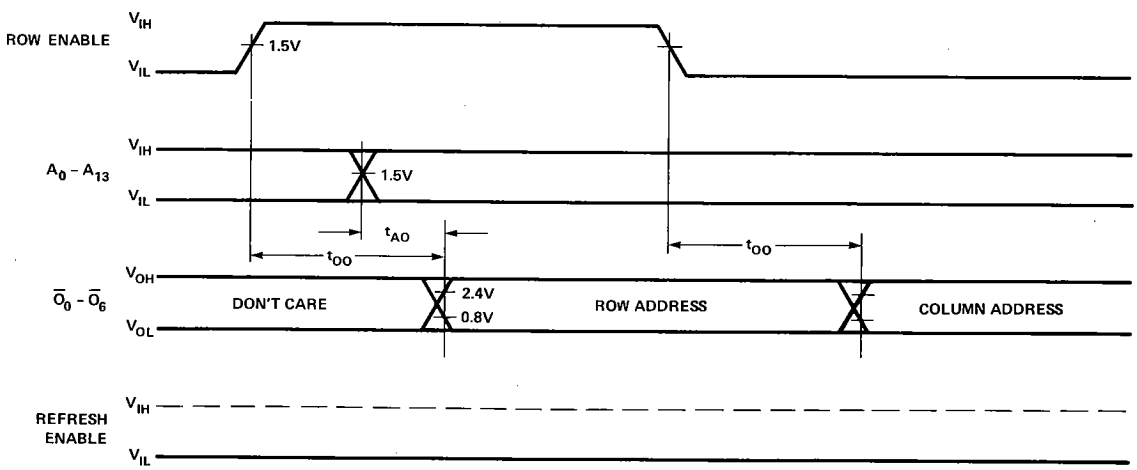
All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to 75°C, Load = 1 TTL, C_L = 250pF, Unless Otherwise Specified.

SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT	CONDITIONS
t_{AO}	Address Input to Output Delay		6	9	ns	Refresh Enable = Low(2)(3)
t_{AOI}	Address Input to Output Delay		16	25	ns	Refresh Enable = Low
t_{OO}	Row Enable to Output Delay	7	12	27	ns	Refresh Enable = Low(2)(3)
t_{OOI}	Row Enable to Output Delay	12	28	41	ns	Refresh Enable = Low
t_{EO}	Refresh Enable to Output Delay	7	14	27	ns	Notes 2, 3
t_{EOI}	Refresh Enable to Output Delay	12	30	45	ns	
t_{CO}	$\overline{\text{Count}}$ to Output	15	40	60	ns	Refresh Enable = High(2)(3)
t_{COI}	$\overline{\text{Count}}$ to Output	20	55	80	ns	Refresh Enable = High
f_C	Counting Frequency			5	MHz	
t_{CPW}	$\overline{\text{Count}}$ Pulse Width	35			ns	
t_{CZ}	$\overline{\text{Count}}$ to $\overline{\text{Zero}}$ $\overline{\text{Detect}}$	15		70	ns	Note 3

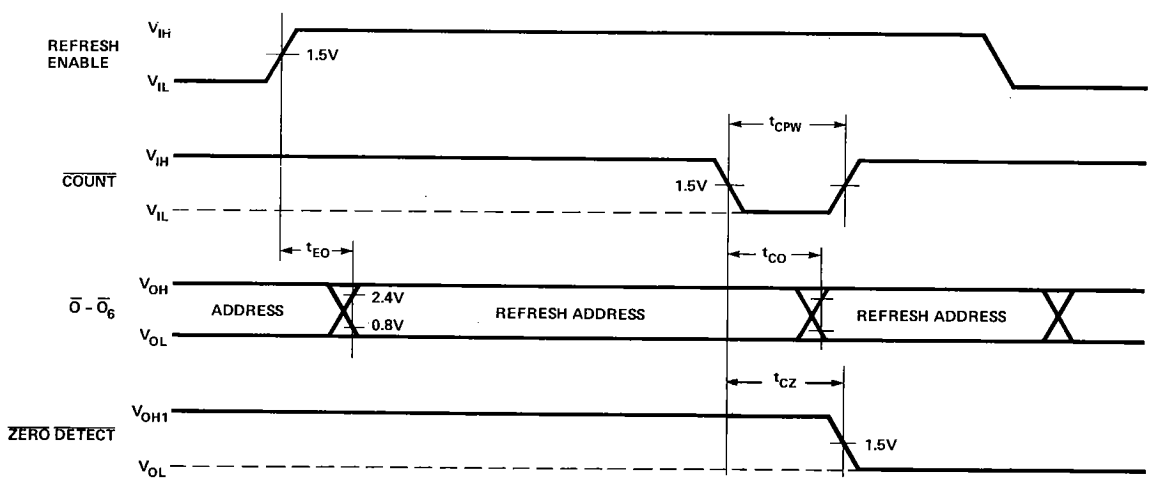
Notes: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. T_A = 25°C, V_{CC} = 5.0V.
3. C_L = 15 pF.

A.C. TIMING WAVEFORMS (Typically used with 2116)

NORMAL CYCLE



REFRESH CYCLE



PIN NAMES AND FUNCTIONS

Pin No.	Pin Name	Function
1	$\overline{\text{Count}}$ Input*	Active low input increments internal 7-bit counter by one for each count pulse in.
2	Refresh Enable Input*	Active high input which determines whether the 3242 is in refresh mode (H) or address enable (L).
9,5,7,21, 23,25,27	A_0–A_6 Inputs*	Row address inputs.
10,6,8,20, 22,24,26	A_7–A_{13} Inputs*	Column address inputs.
11,13,12, 18,17,16, 19	$\overline{O}_0$–$\overline{O}_6$ Outputs	Address outputs to memories. Inverted with respect to address inputs.
14	GND	Power supply ground.
15	$\overline{\text{Zero}}$ $\overline{\text{Detect}}$ Output	Active low output which senses that the six low order bits of refresh address in the counter are zero. Can be used in the burst mode to sense refresh completion.
3	Row Enable Input*	High input selects row, low input selects column addresses of the driven memories.
28	V_{CC}	+5V power supply input.

*The inputs are high impedance, TTL compatible, and suitable for bus operation.

DEVICE OPERATION

The Intel® 3242 Address Multiplexer/Refresh Counter performs the following functions:

1. Row, Column and Refresh Address multiplexing.
2. Address Counting for burst or distributed refresh.

These functions are controlled by two signals: Refresh Enable and Row Enable, both of which are active high TTL inputs. The truth table on page 1 shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter).
2. Row addresses (A_0 through A_6).
3. Column addresses (A_7 through A_{13}).

Burst Refresh Mode

When refresh is requested, the refresh enable input is high. This input is ANDed with the seven outputs of the internal 7-bit counter. At each $\overline{\text{Count}}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0$–$\overline{O}_6$) through 128 row addresses. When the first six significant bits of the counter sequence to all zeros, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output goes low, signaling the end of the refresh sequence. Due to counter decoding spikes, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output is valid only after t_{CZ} following the low-going edge of $\overline{\text{Count}}$. The $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output used in this manner signals the completion of 64 refresh cycles. To use the 128-cycle burst refresh mode, an external flip-flop must be driven by the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$.

Distributed Refresh Mode

In the distributed refresh mode, one row is selected for refresh each ($t_{REFRESH}/n$) time where n = number of refresh cycles required for the device and $t_{REFRESH}$ is the specified refresh rate for the device. For the 2116 $t_{REFRESH}$ = 2 msec and n = 128 or 64, therefore, one row is refreshed each 15.5 or 31 μsec, respectively. Following the refresh cycle at row n_x, the $\overline{\text{Count}}$ input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n_{x+1}. The $\overline{\text{Count}}$ input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address

All 14 system address lines are applied to the inputs of the 3242. When Refresh Enable is low and Row Enable is high, input addresses A_0–A_6 are gated to the outputs and applied to the driven memories. Conversely, when Row Enable is low (with Refresh Enable still low), input addresses A_7–A_{13} are gated to the outputs and applied to the driven memories. Figure 1 shows a typical connection between the 3242 and the 2116 16K dynamic RAM. When the memory devices are driven directly by the 3242, the address applied to the memory devices is the inverse of the address at the 3242 inputs due to the inverted outputs of the 3242. This should be remembered when checking out the memory system.

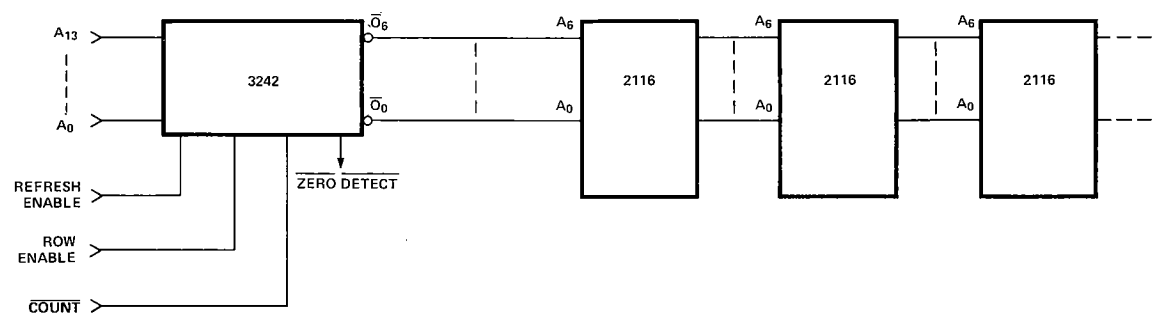


Figure 1. Typical Connection of 3242 and 2116 Memories.

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