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Introduction; OSI 400 Manual 1/7/77

The OSI 400 board can either be a complete stand-alone computer or the CPU board in a large 400 system. The versatility of this board makes it necessary for the user to carefully exaime the documentation BEFORE starting construction of the board. Decisions should be made on what features of the 400 board will be implemented and also on whether RAM memory will be placed on the 400, or just on 420 boards and so on. It is also of prime importance that the user have his over-all configuration in mind when assembling the system.

The following APP Notes are included and should be read carefully.

Number	Subject
2.	System Expansion
3.	Construction Hints
4.	Revised 6502 System Clock

Superboard Customer Services

To aid you in your construction of a Model 400 system, we are providing the following services. Technical questions concerning Model 400 systems can be phoned in during normal business hours (10AM to 5PM EST Monday through Friday). Please identify yourself as a Model 400 purchaser when phoning in questions.

If you obtained the Superboard through a company other than OSI or by other indirect means, be sure to send us your name and address.

Refer to the shipper for expected shipping dates on backordered items.

Thank-you;
The OSI Staff

OSI MODEL 400

THEORY OF OPERATION

This discussion covers the OSI 412A and 413A. Each application note on modifications to the 400 includes its own theory of operation section. Information is included on all ICs used on the Model 400 board. It is suggested that you take one pass through this discussion and then carefully go over the specifications sheets and then take a final pass at the discussion.

The Model 400 Superboard can be configured to accept three processors as stated earlier. The 412A is a 6502 based computer which operates with OSI Superbug 65 Monitor and a serial ASCII terminal. The 413A uses a 6800 and the OSI Superbug 68 Monitor. A 6501 based system can be constructed by using the hardware for a 413A and the 6502 PROMs and software.

Basically, the pin outs of the microprocessors can be divided into three categories; control, address, and data.

The Data Bus

The data lines are the same on all three processors and are pin 26 (D_7) through pin 33 (D_0) of IC-1 on the Superboard. The data lines make up the bi-directional data bus on which instructions and data flow between the processor and memory and I/O devices. The data lines are tristatable, that is, they have three states; high, low, and off (effectively disconnect). These lines are high true and are TTL compatable as inputs and can drive 1 TTL load and 130pf or several MOS devices. D_7 denotes the high order bit or left most bit of data or instruction and D_0 denotes the low order or right most bit. The direction of data is determined by the status of the Read/Write line (R/W) pin 34 of IC-1. This line is internally controlled by the program the processor is executing. When the line is high, the processor is outputting data on to the bus. It is very important that only one device is writing on to the bus at a time. Two devices writing at one time is similar to tying the outputs of two standard TTL gates together... Someone looses! It is also important that only one device be reading to the bus at a time so that the device writing on the bus only has to drive one load. All other devices should be in the tri-state or off mode. (More on the bus in a later section.)

The Address Lines

The address lines are also the same on all three processors with A_0 through A_{11} being pins 9 through 20 respectively, and A_{12} through A_{15} being pins 22 through 25 of IC-1. The 16 address lines provide the binary code which ultimately selects individual memory cells and I/O registers. The 16 address lines allow direct addressing of 65,536 bytes of memory and/or I/O ports. The address lines on the 6800 are tristatable, allowing direct memory access (DMA) by some other device controling the address lines. The address lines of the 6501 and the 6502 are not tristatable. Since the address lines must drive most devices on the address bus all the time, buffering is required on all but the smallest systems. When buffering is required, the tristatable capability of the 6800 is of little advantage.

The Control Lines

The control lines of the three processors are quite different. First, consider the lines which are common to all three processors. Pin 5 of all three processors is the +5volt power. Pins 1 and 21 are ground. All no connection pins (N.C.) should also be connected to ground. These are pins 35 and 38 on the 6800; pins 35, 38, and 39 on the 6501; and pins 5, 35, and 36 on the 6502.

Ready

Pin 2, called RDY (Ready) on the 6501 and 6502 and $\overline{\text{HALT}}$ (not HALT) on the 6800, runs and stops program execution. When RDY goes low, the processor stops executing a program. If the processor stops during phase 2 of the clock (to be described later), the program can resume at any later time coincident with the phase 2 clock by returning RDY high. If RDY is taken low during phase 1, data can be lost barring continuation of the program. RDY is used in conjunction with conventional mini-computer front panels and for accommodating slow memories in systems utilizing some fast memory. The RDY line is OR wired high on the Superboard through a 4.3 or 4.7K resistor. No operator control of this line is neccessary when used with any of the OSI PROM monitors.

Reset

Pin 40 is $\overline{\text{RES}}$ (not RESET). When this line goes low, a processor initialization takes place and a 16 bit address called the restart vector is loaded from memory into the processor's program counter. When the line is returned high, the processor will start executing the program beginning at the location specified by the restart vector. The vector is located at FFFC and FFFD for the 6501 and 6502 and at FFFE and FFFF for the 6800.

The user momentarily brings $\overline{\text{RES}}$ low to start or reset the processor. All OSI monitors contain the appropriate restart vectors so that the processor jumps to the monitor's command mode when a reset occurs. A reset switch is the one and only neccessary front panel control in OSI systems.

Interrupts

By the process of interrupts, it is possible to get the attention of a processor which is executing a program so that it stores in memory all information necessary to resume that program and then jumps to a new program specified by the interrupt. The processor can then, under software control, return from interrupt to the original program with no ill effects. All three processors have three interrupts; a non-maskable interrupt, a conditional interrupt, and a software interrupt.

The non-maskable interrupt is an unconditional interrupt which occurs whenever $\overline{\text{NMI}}$ (pin 6 of IC-1) goes low. This line is OR wired high with a 4.3 or 4.7K resistor. The conditional interrupt is controlled by a bit in the status register and $\overline{\text{IRQ}}$ (interrupt request) pin 4 of IC-1. If $\overline{\text{IRQ}}$ goes low and the mask bit in the status register is not set, an interrupt will occur. If the mask bit is set, no interrupt will occur. $\overline{\text{IRQ}}$ is OR wired high with a 4.3 or 4.7K resistor. Software interrupts are initiated by an instruction in a program and have no external lines. For a more complete discussion of interrupts, please refer to the manufacturer's literature on each specific processor.

The following control lines are only found on the 6501 and the 6800. Both the 6501 and 6800 have external tri-state controls on for the data bus via DBE (Data Bus Enable) pin 36 of IC-1. When this line is low, the data bus is tri-stated; when it is high, the direction of the bus is controlled by R/W. BA (Bus Available), pin 7, goes high when the bus is in the tri-state mode because of a low RDY line or the execution of a wait command on the 6800.

Both processors require an external two phase clock which inputs phase one Ø1 to pin 3 and phase two to pin 37 of IC-1. (more on clocks later)

The 6800 places invalid address codes on the address bus during the execution of some instructions. This could cause problems with devices such as PIAs which have status bits which are automatically reset when the chip is addressed. To cure this problem, a signal called VMA (Valid Memory Address) pin 5 of the 6800 and the 6501 is provided. This line is high when the address is valid. The 6501 always provides a valid address, but includes a "dummy" VMA line which is always high to maintain pinout compatability with the 6800.

The 6800 has one additional line, TSC (tri-state control) pin 39, which tri-states the address lines and R/W when brought high. This line is normally grounded on the Superboard.

The 6502 does not have DBE, VMA, or TSC. It does have two additional lines. SYNC, pin 7, goes high whenever an instruction is fetched from memory. This line capacitively coupled provides a very simple run indicator. It is also useful for scope triggering when trouble shooting. S. O. (Set Overflow), pin 38, sets the overflow bit of the processor's status register when brought high. This line is normally jumpered low on the Superboard, but can be used as a very simple one line output.

Clocks

The 6502 features an internal clock which has three external connections to timing elements. The lines are Ø1 (phase one out) pin 3, Ø2 (phase two out) pin 39, and Ø0 (phase 0 in) pin 37. Clock operation is obtained by connecting a 10pf capacitor between 37 and 39 and a resistor less than 500K from 37 to 3. The internal thresholds and capacitance vary from processor to processor so that the exact value resistor for a given clock frequency can not be predicted. OSI provides a range of resistor values to be used or a good high frequency (i.e. cermit film) trimer pot can be used. The clock can be crystal stabilized by adding a crystal from ground to pin 37. The minimum clock frequency is about 100KHz since internal memory in the processor is dynamic and must be refreshed by clock related signals (internally). The maximum clock frequency for reliable operation is dependent on several factors. These factors include the characteristics of the specific processor chip, address and data bus loading and capacitance, memory and I/O speed, temperature, and supply voltage.

First, consider memory timing. The processor's clock provides two phases Ø1 and Ø2 which make up a machine cycle. Instructions may take two or more cycles to execute. Generally, internal processor operations occur during Ø1 with address bus R/W and VMA settling to the proper pattern by the end of Ø1. The data bus and memory are enabled during Ø2, allowing data communications. Data need only be valid for the last 30ns of Ø2 for proper operation. When a low capacitance address bus is used as in the Superboard, the address lines are typically valid 100ns into Ø1. This means

that the address time of the memory need only be 130ns shorter than Ø1 and Ø2 combined (disregarding propagation delays in TTL). The other timing restriction is that the chip enable to output time be less than Ø2 minus 30ns. For 2102 type memories, this parameter is generally less than one half the access time.

Unfortunately, the system can only be run as fast as its slowest memory unless circuitry is provided to stretch Ø2 selectively when the slow memory is addressed. The slowest memory supplied by OSI is the 1702A PROM. This device is factory specified at 700ns access time at 25°C. This implies approximately 1MHz clock operation (1us cycle time) without Ø2 stretching. The 6502 processors supplied by OSI are either 1MHz guarenteed (2MHz typical) or 2MHz guarenteed.

Clock stretching techniques, timing requirements and determination of maximum processor speed for the 6502 are the subject of a separate OSI applications note.

6800, 6501 Clock

The 6501 and 6800 both require an external two phase clock. The clock must provide non-overlapping pulses which have highs very close to +5volts. The minimum clock rates for these processors are also 100KHz. The 6800 is rated at 1MHz typical. The Superboard uses a 74123 dual one shot to generate Ø1 and Ø2. The Ø2 one shot has provisions for clock stretching by normally paralleling the two charging resistors via a diode. When the diode is reverse biased, only one charging resistor is active, doubling the Ø2 period. It is recommended that the 1702A PROMs be connected to the clock stretcher for 1MHz operation with the 6800. Refer to the OSI applications note on high speed operation for details on operating a 6501 faster than 1MHz.

The 74123 clock is IC-3 of the Superboard with Ø1 coming out pin 13 and Ø2 coming out pin 5. These signals do not have sufficient voltage swing to drive the processor directly so they are buffered through a 7417 open collector driver (IC-2). The buffers are pulled up through 1K resistors and provide Ø1 at pin 8 of IC-2 and Ø2 at pin 10.

System Control Signals

Ø2 must also be provided to gate all data bus parts. The Superboard uses a 7417 buffer to provide Ø2 to the bus. Pin 1 of IC-2 is either connected to pin 39 of the 6502 or to pin 11 of IC-2. Ø2 out is available at pin 2 of IC-2. A 470ohm pull up should be provided at the far end of this line.

VMA is also buffered and is available at pin 4 of IC-2. 6501 and 6502 systems should have this gate left disconnected by not providing a feed through on the P.C. foil associated with this pin. The 470ohm VMA pull up will assure a high. R/W is diode OR wired to a buffer to allow a front panel memory load switch to force a low on the R/W line. When a front panel is not anticipated, R/W from the processor can be connected directly to pin 5 of IC-2.

Buffered R/W is available on pin 6 of IC-2. VMA and Ø2 are ANDed with a front panel enable control which can force this line high producing VMA·Ø2+FPC at pin 8 of IC-T. This line is generally refered to as VMA·Ø2. If a front panel is not used, pin 9 of IC-T should be tied to pin 13 of IC-S. VMA·Ø2 is used to enable each device on the data bus.

The Adress Bus

The 16 address lines from the processor are buffered via three 7417s IC-B, K, and R. The +5 power for these three buffers can be provided through the front panel enable switch or a transistor instead of directly through the +5 supply. The 7417s tri-state when power is turned off. The input characteristics do not change when power is disconnected. This technique provides a very low cost tristatable address bus for front panel control and DMA. All address bus lines should be pulled up at the far end of the bus with 470ohm resistors. The 10 low order address lines are fed to all 2102 memories in the system. Since a typical system will have several memory expansion boards, the 10 low order address lines are brought out to the card edge in the same order as the pinouts on the 2102 memories to minimize layout complexity. The eight lowest address lines are also provided to the 1702A memories. Additionally, A_0 is provided to the ACIA to select its two memory locations.

The six high order address lines go to address decoders to define address locations for memory and I/O. The address configuration of the computer is very important and the user must fully understand it to successfully use the unit. OSI minimal system address configuration is given in Table 1.

Table 1. OSI Minimal System Address Configuration

Device	Primary Address	Address Range
1K RAM	0000 to 03FF	0000 - EFFF
256 Word PROM	FE00 to FEFF	FE00 - FFFF
ACIA	FC00 and FC01	FC00 -FCFF

The basic 412A and 413A have three addressable devices or groups in memory. These are a 1024 byte RAM, a 256 word PROM, and an ACIA for serial communications which has two addressable locations. These devices, which require only 1272 address locations have over 65,000 possible locations. If their addresses are fully decoded, they will occupy 1,272 address locations specified by the primary addresses listed in Table 1. However, in a small system, it is not desirable to fully decode the addresses because it unnecessarily increases the hardware and decreases the software versatility.

The address range given in Table 1 is the range of the addresses which will "access" the device. By addressing 0401, one is addressing the same location as 0001, 0801, 0C01, etc. A good example of why this is beneficial is the OSI Superbug PROM Monitor which is a 256 word PROM. The actual monitor is preprogrammed to operate at FE00 through FEF9. The monitor also contains the restart and interrupt vectors at FFFA to FFFF. By placing the monitor at both FE00 to FEFF, it performs two importnat functions. The user can then add another PROM with a program and the vectors at FF00 to FFFF at a later time without obsoleting his Superbug Monitor.

Although the basic Superboard has only 1K of RAM, it can run any 1K long program written anywhere within the range of 0000 to EFFFF without modification. A good example of this is the OSI game package for the 650X. Only one game can reside in the basic 1K at a time. But, by following the OSI system expansion plan, as more memory is added, all programs can be stored in memory at the same time with no modification to software.

Diagram 1 shows the basic address decoding logic on the Superboard. The user has at least two 16 pin locations (IC-Q and X) and some left over gates to further decode addresses for the first step of system expansion. The two sections on the right show possible approaches for further decoding. The RAM decoder will fully decode the 2102 memories for the first 1K memory locations. The PIA decoder locates an optional PIA at FDXX. The 1702 address can be split into two addresses: FFXX and FEXX, to accommodate an additional PROM. Each system expansion board has its own address decoder so that only the 16 address lines need to be fed to the bus.

RAM Memory

The eight 2102s which make up the 1K by 8 RAM memory are located at IC-C through J. The implementation scheme is shown in diagram 2A. As stated before, the 10 low order address lines go directly to the eight 2102 memories. The chip enable ($\overline{CE}$) pin 13 is connected as indicated in the addressing section. The data input (pin 11) is connected directly to the data bus. Although the data output (pin 12) is tristatable, it can not be tied directly to the data bus because the output can not be disabled during write operations. Consequently, the output must be gated with R/W which is also fed to pin 3 of each 2102. The data out lines are first inverted via 7404s (IC-L and M) and ANDed with R/W via 7403 open collector gates (IC-N, O).

PROM Memory

The Superboard can accept two 1702A PROMs. OSI systems typically have only one PROM which contains a system monitor and/or bootstrap loader. Any Superboard system must have either a PROM containing the restart vector and a program to load memory from some external device, or a dedicated program, or a front panel which allows manual program entry.

When only a front panel is used, RAM memory must be placed at the restart vector location so that this vector can be loaded from the front panel. A scheme for accomplishing this is shown in the upper portion of Diagram 1B.

1702As and the Data Bus

The implementation of the 1702A on the bus is shown in Figure 2B.

The 1702As data outputs are unusual in that they can go approximately -4volts on logical lows with no loading. 68XX and 65XX parts are rated only to -.3volts input. This can obviously cause a problem. The processor alone does not provide sufficient load to raise this voltage to a safe range. A 1702A should NEVER be used alone with a 6501, 6502, or 6800 microprocessor. Additional parts and pull ups are necessary on the data bus to insure bus levels above -.3volts. Table 2 lists the typical levels from a 1702A as more parts are added to the bus. The right column shows the current the processor must sink to drive a low on the bus. The 1702A must sink considerably more current since it is working against the clamping action of the 7403 and the 8T26; but it is still within its specifications. The low levels given are for static measurements. At 1MHz operation, the logic levels will typically be .2volts higher because of bus capacitance and the access time of the 1702A.

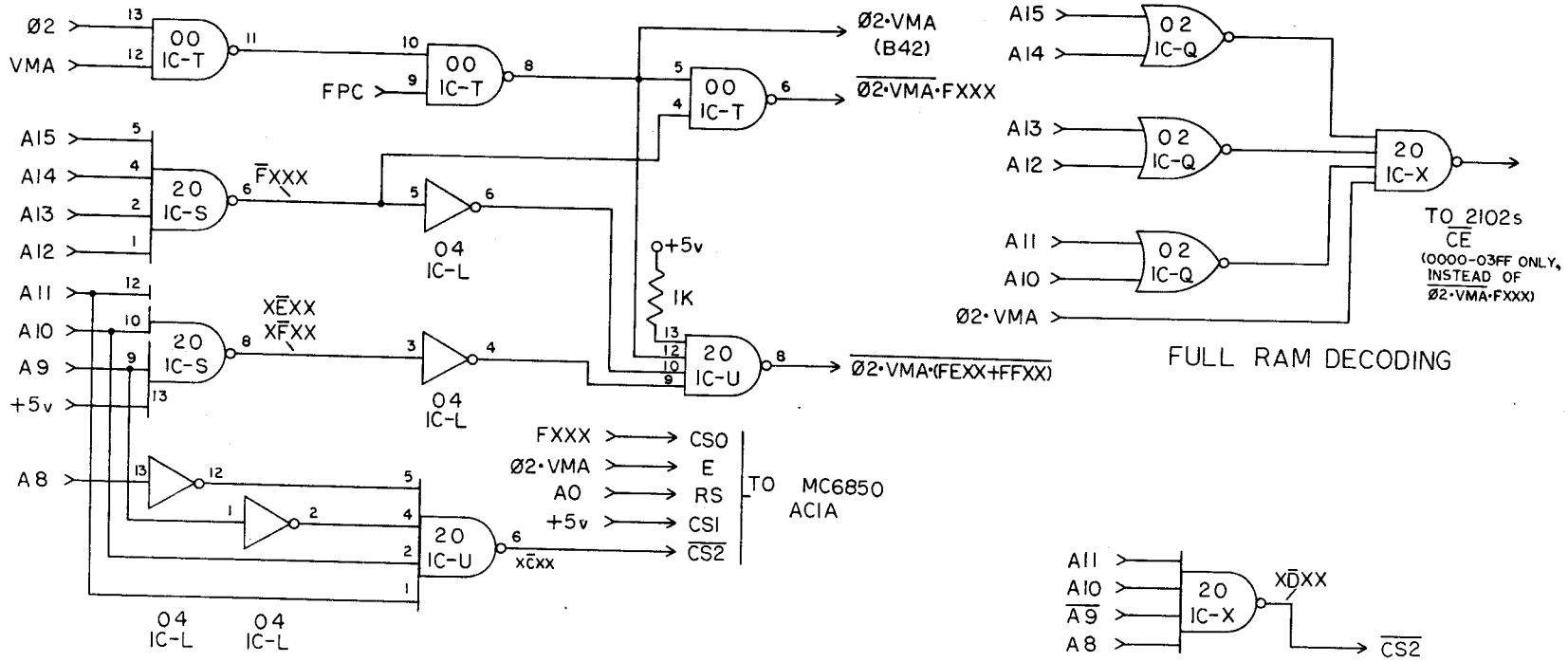
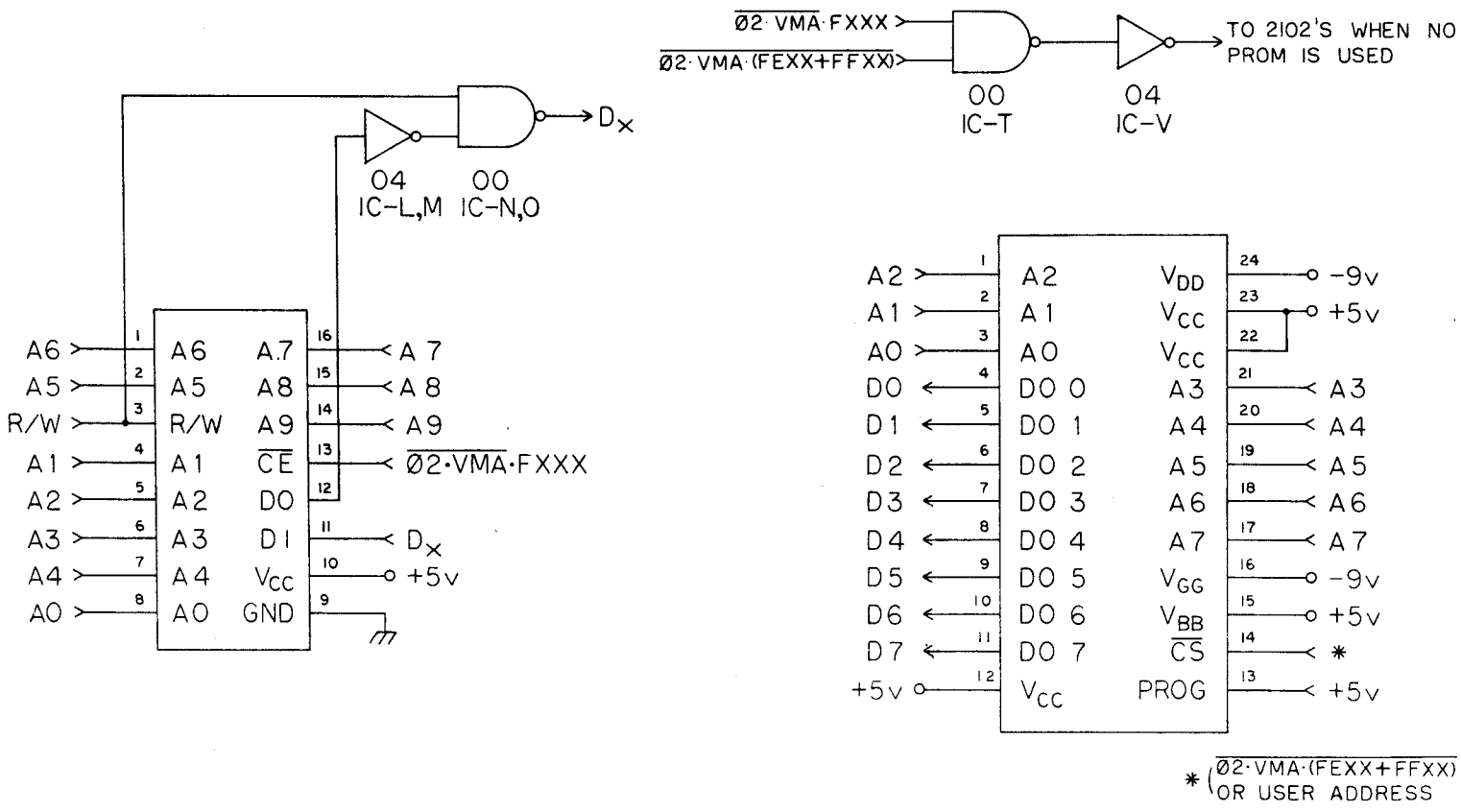

Ø2
VMA
00 IC-T
FPC
00 IC-T
Ø2·VMA (B42)
Ø2·VMA·FXXX
00 IC-T
A15
A14
A13
A12
20 IC-S
FXXX
04 IC-L
+5v
1K
A11
A10
A9
+5v
XEXX
XFXX
20 IC-S
04 IC-L
20 IC-U
Ø2·VMA·(FEXX+FFXX)
A8
FXXX → CS0
Ø2·VMA → E
A0 → RS
+5v → CSI
CS2
TO MC6850 ACIA
20 IC-U
XCXX
04 IC-L
04 IC-L
A15
A14
02 IC-Q
A13
A12
02 IC-Q
20 IC-X
TO 2102s CE (0000-03FF ONLY, INSTEAD OF Ø2·VMA·FXXX)
A11
A10
02 IC-Q
Ø2·VMA
FULL RAM DECODING
BASIC ADDRESS DECODING
A11
A10
A9
A8
20 IC-X
XDXX
CS2
FXXX → CS0
+5v → CSI
Ø2·VMA → E
A0 → RS0
A1 → RS1
PIA ADDRESSING
Ø2·VMA·(FEXX+FFXX)
A8
02 IC-Q
04 IC-V
Ø2·VMA·FEXX (TO CE IC-8)
00 IC-T
Ø2·VMA·FFXX (TO CE IC-7)
04 IC-V
ADDRESSING FOR TWO PROMS

DIAGRAM 1



2102/9102

1702A PROM

DIAGRAM 2- RAM/PROM IMPLEMENTATION

Table 2. Typical Levels From a 1702A as More Parts are Added to the Bus

Part	1702A Low Logic Output (Static)	Processor Sink Current
1702A only	-4volts	0
+Processor	-2volts	.05ma
+7403	-.7volts	.15ma
+4.7K pull ups	-.4volts	1.15ma
+2102s	-.3volts	1.20ma
+8T26 Buffers	-.1volts	1.40ma
+ACIA, PIA and second 1702A	0volts	1.55ma

Dynamic undershoot measurements are extremely difficult to make on the bus. A low capacitance wide band FET input probe on a scope with at least 75MHz bandwidth should be used. A recent hobby or service quality scope or an older lab scope with a 10X probe will double the bus capacitance and will have a 5 to 10% overshoot, yielding ???? results.

Fortunately, it should not be necessary to make this measurement. The standard 412A or 413A operating at 1MHz has a respectable safety margin. However, if a front panel is used with a PROM, additional precautions should be taken. 8T26s should be installed or 74LS03s can be substituted for the 7403s to insure static levels above -.3volts if the PROM is manually addressed.

ACIA

The 6850 ACIA is a bus oriented serial I/O device very similar to a UART. On the 412A and 413A, it is the only I/O device supplied. The ACIA form of serial communications has many advantages over the software form of serial communications used by the Motorola MIKBUG[tm] and virtually all the other hobby 6800 systems. Via a software system, serial output and input are accomplished by rotating bits in the processor's accumulator in or out; a one bit I/O. This means that the processor must devote its full attention to communicating with its I/O. Furthermore, the I/O communications routines are quite clumsy and utilize the full resources of the processor (i.e. all registers), making linkage to these routines by an outside program difficult. Motorola initially utilized the software approach before the ACIA was released. Their new evaluation board now utilizes an ACIA and an extended version of MINIBUG[tm] instead of MIKBUG[tm].

The ACIA is essentially a self contained I/O processor. The main processor simply loads it with data as it would any other memory location. The ACIA then automatically adds start and stop bits, parity (optionally) and sends it out at the proper baud rate. On incoming data, the processor simply reads the ACIA as it would any other memory location. The ACIA then automatically adds start and stop bits, parity (optional) and sends it out at the proper baud rate. On incoming data, the processor simply reads the ACIA as any other memory location. It obtains inputted data stripped of start and stop bits and prechecked for parity errors. Additionally, the ACIA provides status flags and an interrupt request for use by the processor.

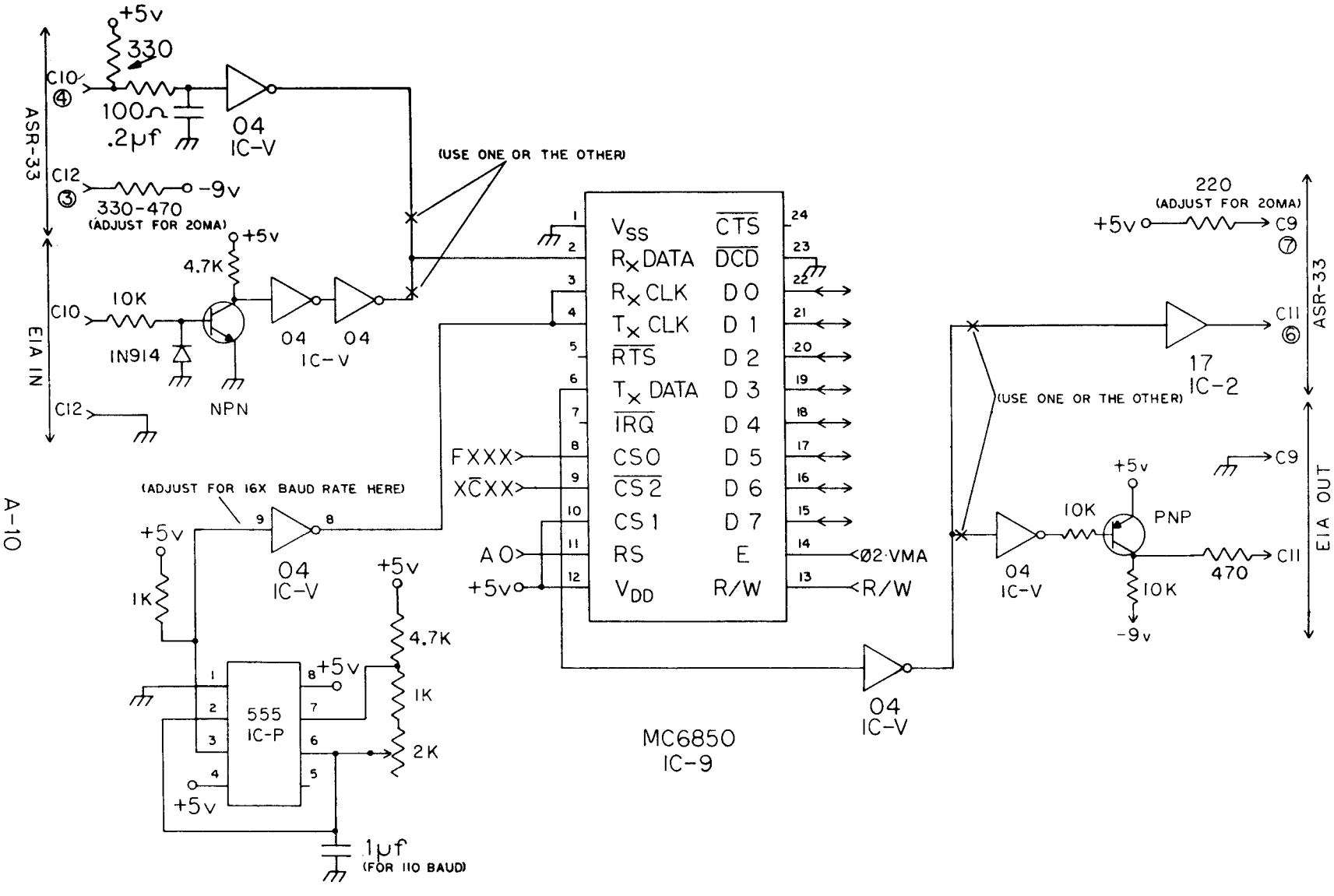


DIAGRAM 3- ACIA IMPLEMENTATION

REVISION 3.0

A simple example of ACIA superiority is the program loader. A loader takes inputted data and places it in memory. Typically, the data is in some other form from what is desired in memory such as ASCII coded hexidecimal. Also the data may be loaded at several different specified locations; not just sequentially in memory. The device providing the data may be a paper tape reader, magnetic tape, a modem or floppy disk. These devices do not wait between characters. A software serial communications system must spend nearly all of its time communicating, restricting loaders to very low speed communications (110 baud) and very simple functions. An ACIA based system requires only three to 10usec processor time to service each character, leaving the rest of the time between characters for code conversion and memory loading. This allows the use of conventional computer loaders and very high communications rates. Baud rates above 40,000 are possible, allowing direct communications with floppy disks, etc.

Diagram 3 shows the Superboard implementation of the ACIA. Please refer to the manufacturer's specifications sheets on the signal lines and internal register architecture. A conventional 555 timer is used as the ACIA clock. OSI software sets the ACIA for ÷ 16 so the clock frequency should be 16 times the desired baud rate. The .1uf capacitor should be changed for different baud rates as per the 555 specifications sheet. The 2K pot should be used for fine adjustment only. Both 20ma current loop and RS-232C interfaces are shown. Only one should be used with the system. Both interfaces are usable from 0 to 9600 baud. OSI supplied software will generally operate to 9600 baud.

The 20ma current loop biasing resistors should be adjusted for 20ma idle current with the terminal in the loop. The circled numbers indicate the connection numbers on the black barrier strip at the right rear of a standard ASR-33 Teletype.

The RS-232C interface shown meets all standards for voltage levels, impedance, slew rate, open circuit status, and short circuit. It may be possible to reduce the voltages on the output op amp (to +5, -9) depending on characteristics of the terminal it is used with.

The ACIA is designed for seven bit or eight bit communications; it is not suited for Baudot five level code. Refer to the OSI Applications note on Baudot Communications Via Superboard.

Options

The Superboard will accept two 8T26 Quad tristatable bus transceivers for data bus expansion. These devices are necessary if any system expansion boards are used because the Superboard's internal bus is fully loaded when completely populated and all expansion boards accept a low true data bus (8T26s invert). The 8T26s have a fan out of 250 boards! The OSI backplane board scheme and buffering scheme has a capability in line with this number of boards, providing essentially infinite system expansion with full multiprocessor and distributed processing capabilities. The 8T26s are configured so that the bus direction is normally from the processor to system boards. When a system card brings the data direction (D.D.) low, data flows from a system card on to the bus.

IC-A is a 40 pin catch-all location. The 10 lines common to the 6820 and 6530 including the TIM and KIM monitors are committed to foil. The other lines are uncommitted. This location can easily accept a 6820 or 6530. It can also accept a 6830 such as the 6830L7 MIKBUG™ or an S1883 UART for Baudot communications with some foil cutting. Refer to each specific Applications Note for implementation of this location.

System Expansion

The Superboard is designed for use as a stand alone computer or as the basis for an extremely powerful computer system. The system is designed for step by step expansion without any large jumps or requirements for backtracking along the way. The key to large system capability is the OSI system bus as shown in Diagram 4. There are 48 lines available on the right hand side of each system board. These lines will be refered to as B_1 through B_{48}. They are in four groups of 12 connectors on .156" centers for use with the Molex KK-156 card connection system. In systems with four or fewer boards where system expansion is not anticipated, boards may be jumpered together.

Lines B_1 through B_{12} and B_{25} through B_{36} are common to all system cards which plug into the backplane. Lines B_{13} through B_{24} are generally unique to each card, If used at all. Lines B_{37} through B_{48} are common to all cards with the exception of Ø2 and VMA. Ø2 is a non-gated signal which is on whenever power is applied to the Superboard. It is used to synchronize the other devices on the bus which should not be stopped by VMA being low or the front panel enabled. If a 6501 or 6502 is used without a front panel, this line can be eliminated. VMA is used only with 6800s. In moderate to large systems, Ø2•VMA should be buffered via IC-R before coming out to B_{42}.

Control Connector

On the top left of the board is a 12 pin connector area compatable with the KK-156 series Molex connectors. The pin designations from left to right are given in Diagram 4.

The Front Panel

The front panel for systems utilizing any of the OSI ROM monitors need only have a reset switch. This switch would be a SPST momentary configuration to simply bring $\overline{RST}$ low to initialize the system. The reset routine provides a short debounce period. Switches which have long bounce periods may require an RC or flip flop debounce circuit for reliable operation. The 7417 buffers IC-B, K and and R should be powered via the +5 bus. The F.P.C. line on IC-T (pin 9) should be tied to pin 13 of IC-S. A halt switch may be desired to stop the processor in unusual circumstances, but it is generally not of much use without a complete front panel.

A very simple complete minicomputer type front panel is shown in Diagram 5. A useful subset of the complete front panel is the address display which is simply 7417s driving LED indicators. Address indicators provide indication of activity in the computer and are especially useful when writing and debugging routines. The inputs to the 7417 address display can be connected directly to the OSI bus. The complete front panel uses switch logic for control functions.

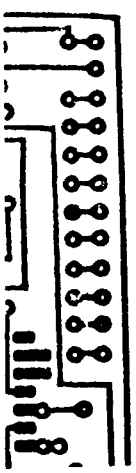
B1 - WAIT
2 - $\overline{NMI}$
3 - $\overline{IRQ}$
4 - Data Direction
5 - D0
6 - D1
7 - D2
8 - D3
9 - D4
10 - D5
11 - D6
12 - D7

B13 - *
14 - *
15 - *
16 - *
17 - *
18 - *
19 - *
20 - *
21 - *
22 - *
23 - *
24 - -9volts

*User for PIA or Other Signals

B25 - +5volts
26 - +5volts
27 - ground
28 - ground
29 - A6
30 -A7
31 - A5
32 - A8
33 - A9
34 - A1
35 - A2
36 - A3

B37 - A4
38 - A0
39 - Ø2
40 - R/W
41 - VMA
42 - Ø2·VMA
43 - A10
44 - A11
45 - A12
46 - A13
47 - A14
48 - A15



C1 - Processor RDY or $\overline{HLT}$
C2 - Power Ground
C3 - $\overline{RESET}$
C4 - *
C5 - *
C6 - *
C7 - *
C8 - *
C9 - Serial Trans. G or +
C10- Serial Receiver
C11- Serial Transmitter
C12- Serial Receiver G or -

*User and for Front Panel Control Functions

Diagram 4.

A SIMPLE FRONT PANEL FOR THE MODEL 400

A front panel is particularly useful for system and program debugging and I/O development. It is not recommended for program loading. The simple memory load circuit shown is for use only with 2102 memories.

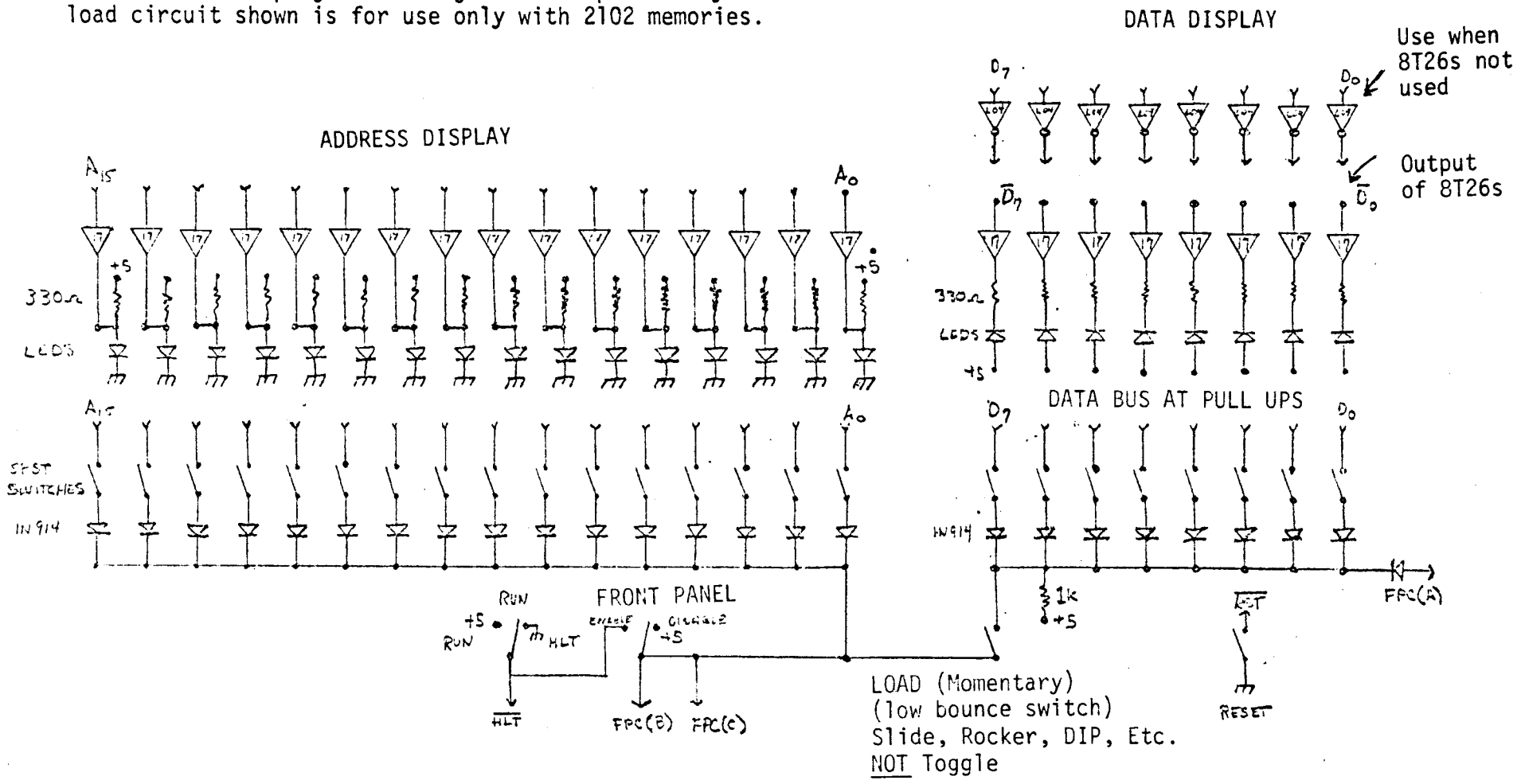


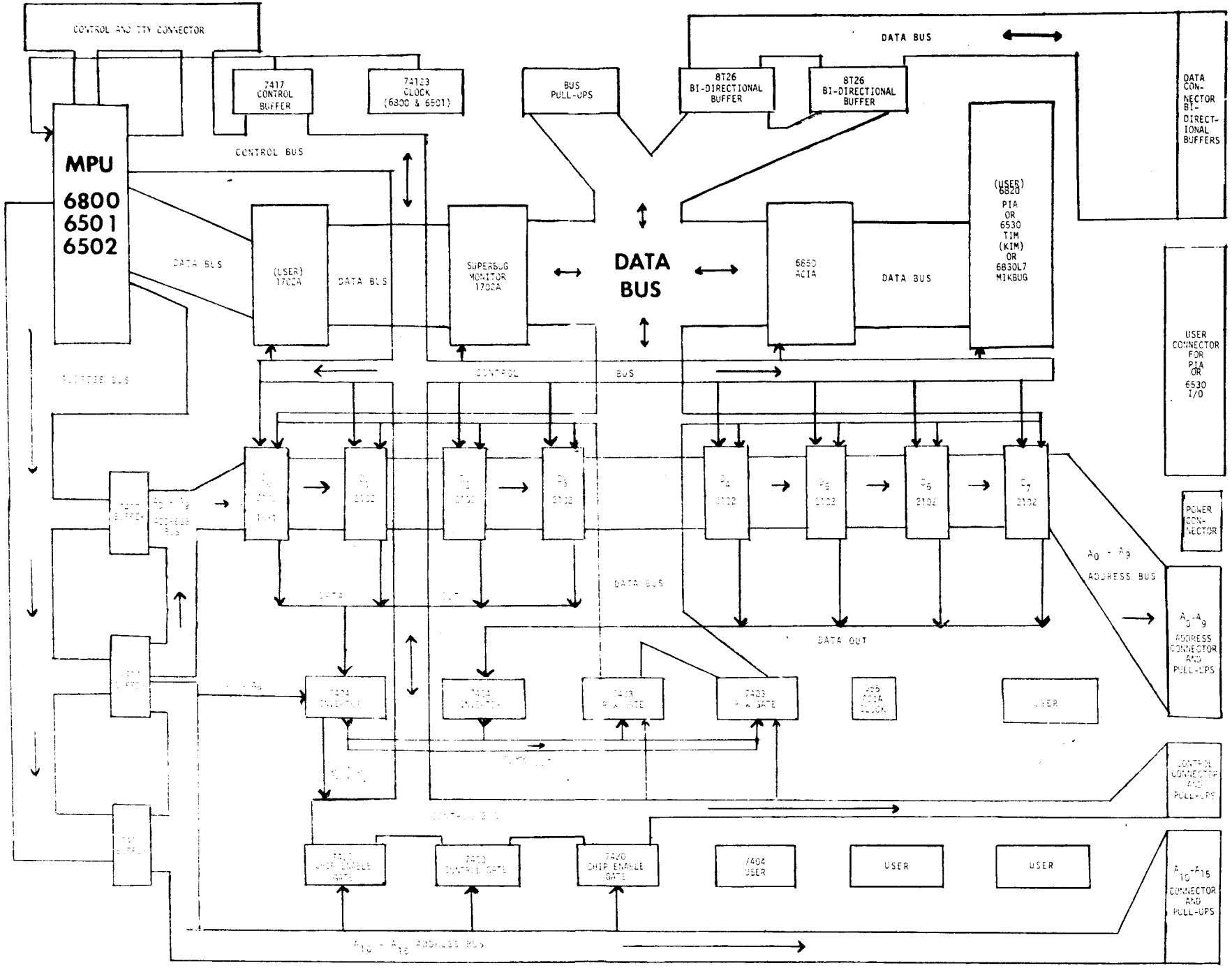
DIAGRAM 5

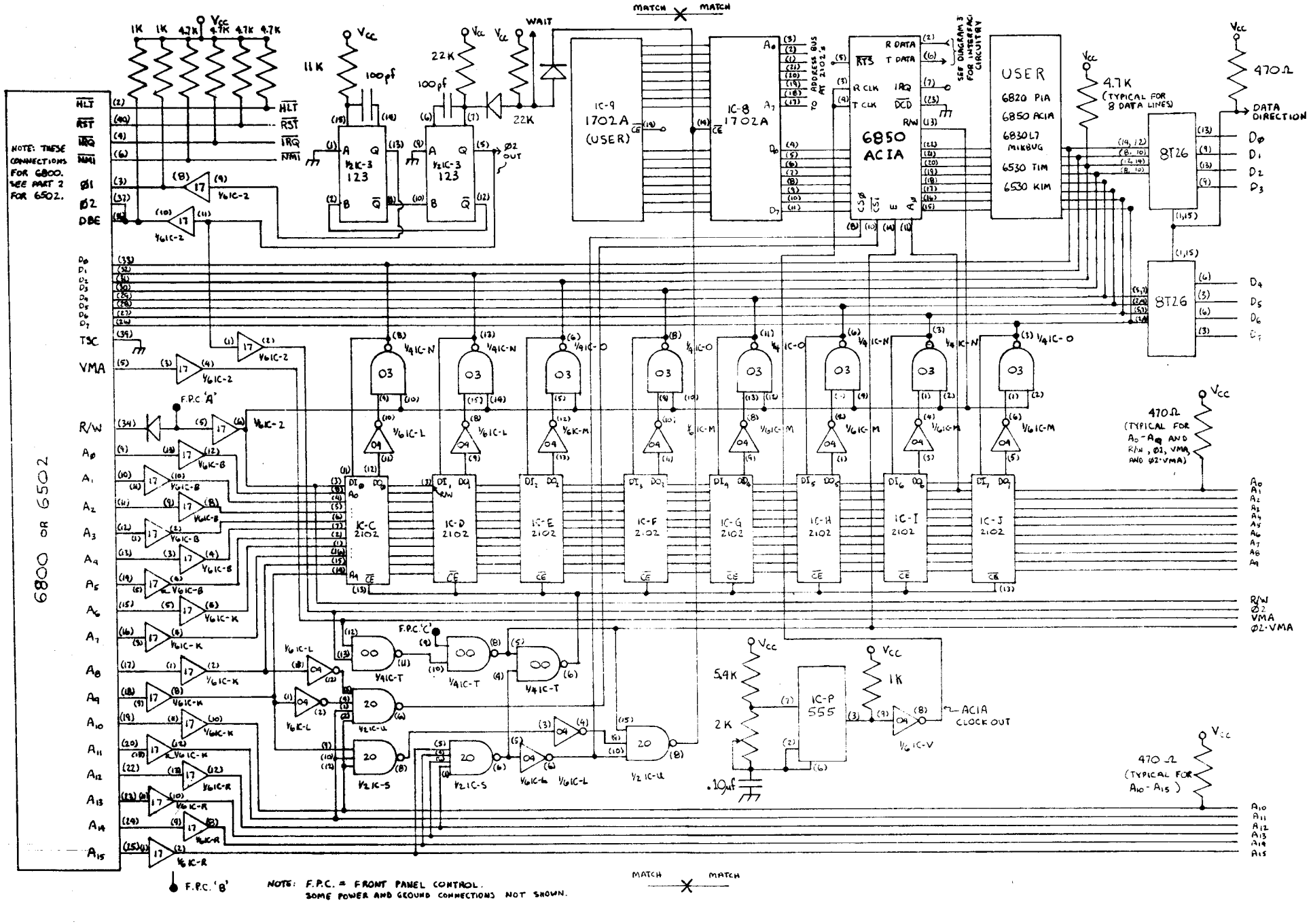
With the run switch in the run mode, all switches are disabled via back biased diodes. The address and data displays will be displaying the contents of their respective buses. The address bus display provides useful information when the processor is running as stated earlier, but the data bus is gated via Ø2 so that all data lines are high half the time. When the front panel is enabled, power is shut off to the 7417s driving the bus, effectively tri-stating them. The address switches are now enabled via forward biased diodes and command the bus. Ø2·VMA is also forced high via F.P.C.(C.) so the data display shows the contents of the memory locations specified by the address switches.

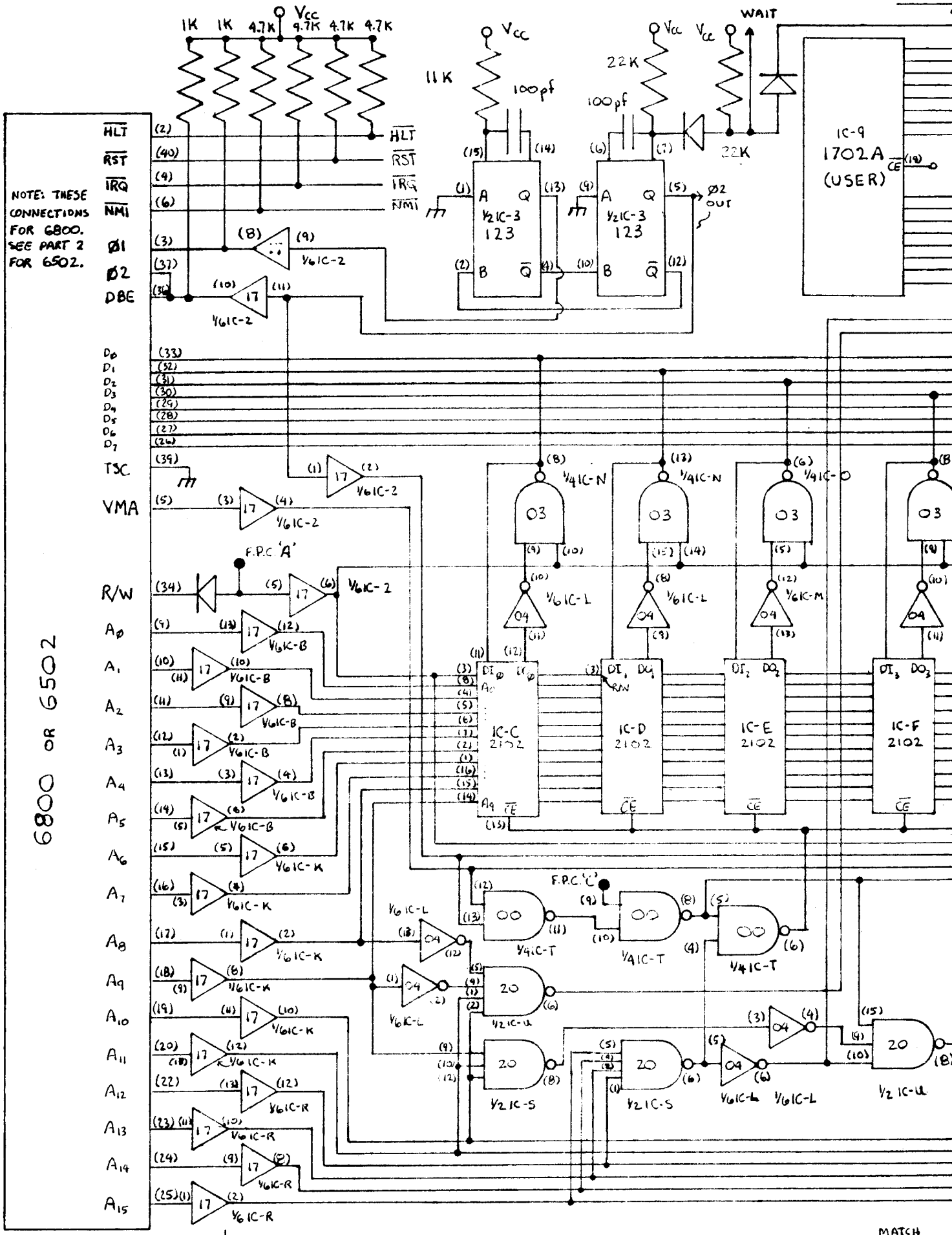
When the load switch is activated, the data switches are activated via forward biasing of their diodes and the R/W line is brought low via F.P.C.(A.): loading the memory location specified by the address switches with the data switches. Since the R/W line on the 2102 memories responds much faster than the data input lines timing on the load switch opening is not critical. However, if the switch bounces excessively, "garbage" will occassionally be loaded, requiring a reloading of that memory location. Since the run switch is not gated with Ø2, programs must be restarted once the processor is stopped via the front panel. The reset line should be low before returning to the run condition. To be completely insensitive to switch bounce on the run line, the processor should be stopped by first bringing reset low and then run low. Reset can then be returned high or left low while the front panel operations are performed. The data bus switches must be connected to the internal bus of the processor. This is best accomplished by placing a ribbon cable at location 4 instead of the bus pull ups. The bus pull ups can then be located at the front panel.

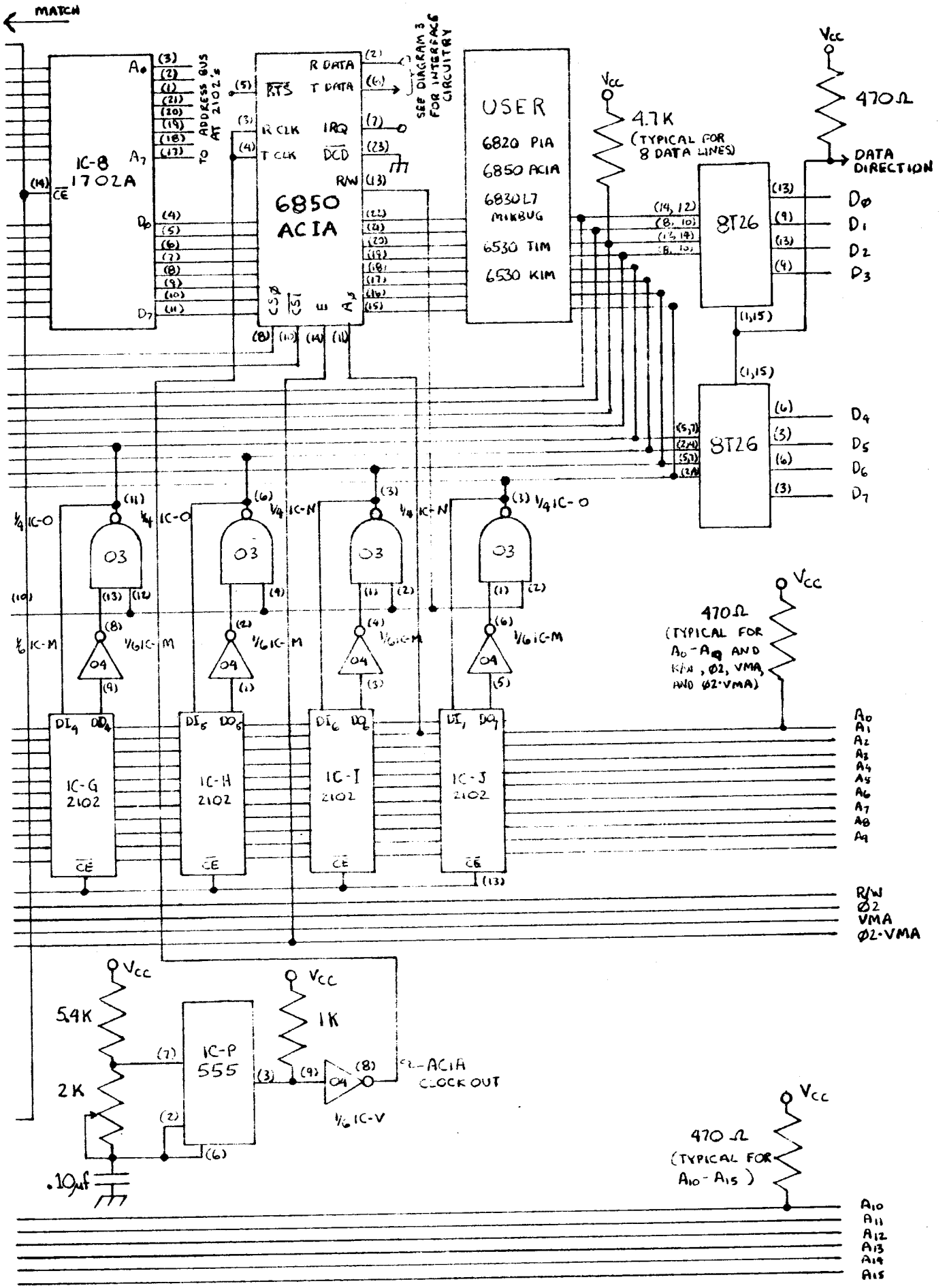
An Overview

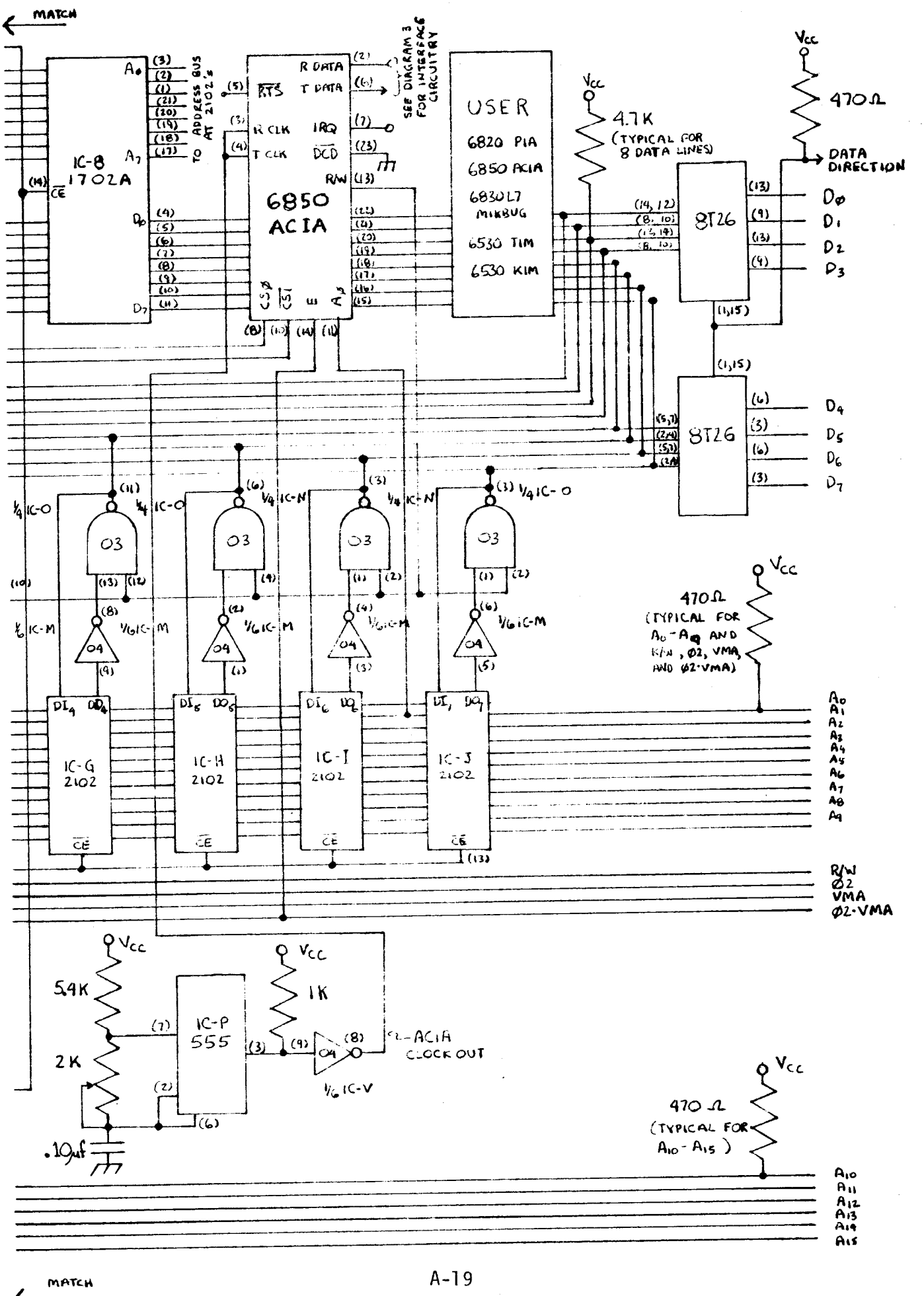
Diagram 6 is a functional schematic for the Model 400. You should now have a good idea of what each part is for and an understanding of the layout of the P.C. board. Diagrams 7 and 8 are schematics for the Model 412A and the Model 413A. A 2X enlargement of Diagram 7 is included as a construction aid.

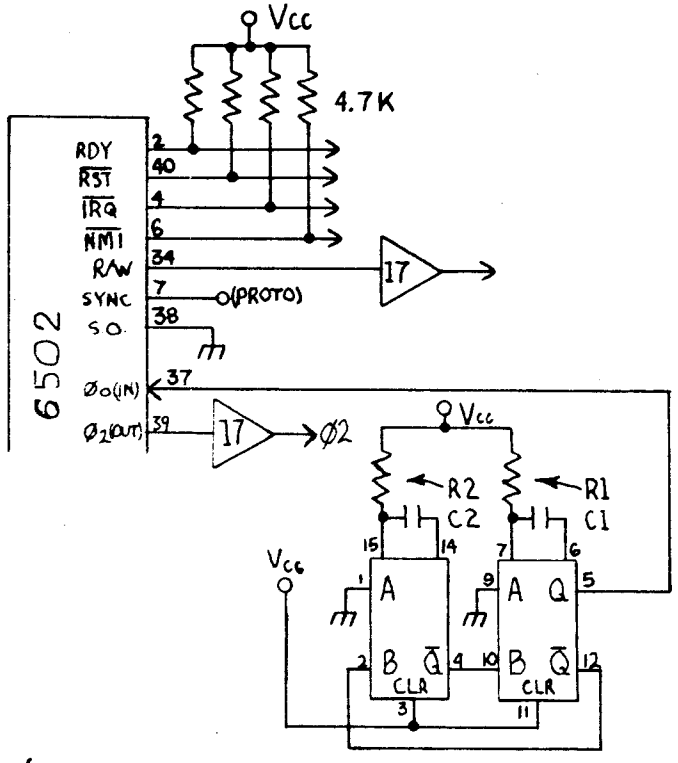

CONTROL AND TTY CONNECTOR
7417 CONTROL BUFFER
74123 CLOCK (6800 & 6501)
BUS PULL-UPS
8T26 BI-DIRECTIONAL BUFFER
8T26 BI-DIRECTIONAL BUFFER
DATA BUS
DATA CONNECTOR BI-DIRECTIONAL BUFFERS
MPU 6800 6501 6502
CONTROL BUS
DATA BUS
(USER) 1702A
DATA BUS
SUPERBUG MONITOR 1702A
DATA BUS
6850 ACIA
DATA BUS
(USER) 6820 PIA OR 6530 TIM (KIM) OR 6830L7 MIKBUG
USER CONNECTOR FOR PIA OR 6530 I/O
CONTROL BUS
POWER CONNECTOR
2102
2102
2102
2102
2102
2102
2102
2102
DATA BUS
DATA OUT
A0 - A9 ADDRESS BUS
A0-A9 ADDRESS CONNECTOR AND PULL-UPS
7404 USER
7403 P.I.A. GATE
7403 P.I.A. GATE
ACIA CLOCK
USER
CONTROL CONNECTOR AND PULL-UPS
7420 CHIP ENABLE GATE
7420 CHIP ENABLE GATE
7420 CHIP ENABLE GATE
7404 USER
USER
USER
A10 - A15 ADDRESS BUS
A10-A15 CONNECTOR AND PULL-UPS


6800 OR 6502
NOTE: THESE CONNECTIONS FOR 6800. SEE PART 2 FOR 6502.
HLT
RST
IRQ
NMI
Ø1
Ø2
DBE
TSC
VMA
R/W
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7
F.P.C. 'A'
F.P.C. 'B'
F.P.C. 'C'
1K
4.7K
11K
22K
100pf
.10µf
5.9K
2K
Vcc
WAIT
MATCH
1/2 IC-3 123
IC-9 1702A (USER)
IC-8 1702A
6850 ACIA
R DATA
T DATA
R CLK
T CLK
IRQ
DCD
RTS
RW
CSØ
CS1
CS2
E
TO ADDRESS BUS AT 2102's
SEE DIAGRAM 3 FOR USER'S CIRCUITRY
USER
6820 PIA
6850 ACIA
6830L7 MIKBUG
6530 TIM
6530 KIM
4.7K (TYPICAL FOR 8 DATA LINES)
470Ω
DATA DIRECTION
8T26
IC-C 2102
IC-D 2102
IC-E 2102
IC-F 2102
IC-G 2102
IC-H 2102
IC-I 2102
IC-J 2102
470Ω (TYPICAL FOR A0-A8 AND R/W, Ø2, VMA, AND Ø2·VMA)
470Ω (TYPICAL FOR A10-A15)
IC-P 555
ACIA CLOCK OUT
R/W
Ø2
VMA
Ø2·VMA
NOTE: F.P.C. = FRONT PANEL CONTROL. SOME POWER AND GROUND CONNECTIONS NOT SHOWN.

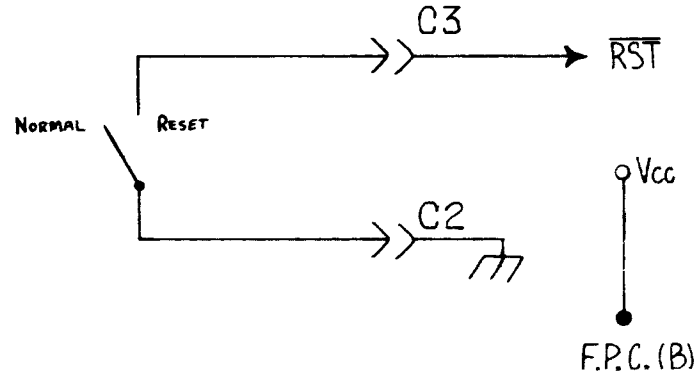

MATCH
WAIT
Vcc
1K 1K 4.7K 4.7K 4.7K 4.7K
11K
100pf
22K
100pf
22K
IC-9
1702A
(USER)
NOTE: THESE CONNECTIONS FOR 6800. SEE PART 2 FOR 6502.
HLT
RST
IRQ
NMI
Ø1
Ø2
DBE
TSC
VMA
R/W
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
6800 OR 6502
½IC-3 123
Ø2 OUT
1/6IC-2
1/4IC-N
1/6IC-L
1/6IC-M
IC-C 2102
IC-D 2102
IC-E 2102
IC-F 2102
F.P.C. 'A'
F.P.C. 'B'
F.P.C. 'C'
1/4IC-T
½IC-U
½IC-S
1/6IC-K
1/6IC-B
1/6IC-R
MATCH
NOTE: F.P.C. = FRONT PANEL CONTROL
SOME POWER AND GROUND CONNECTIONS NOT SHOWN.


MATCH
IC-8
1702A
ADDRESS BUS AT 2102's
6850
ACIA
R DATA
T DATA
R CLK
T CLK
IRQ
DCD
R/W
RTS
SEE DIAGRAM 3 FOR INTERFACE CIRCUITRY
USER
6820 PIA
6850 ACIA
6830L7
MIKBUG
6530 TIM
6530 KIM
Vcc
4.7K
(TYPICAL FOR 8 DATA LINES)
470Ω
DATA DIRECTION
8T26
D0
D1
D2
D3
D4
D5
D6
D7
1/4 IC-O
1/4 IC-N
1/6 IC-M
03
04
IC-G 2102
IC-H 2102
IC-I 2102
IC-J 2102
470Ω
(TYPICAL FOR A0-A9 AND R/W, Ø2, VMA, AND Ø2·VMA)
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
R/W
Ø2
VMA
Ø2·VMA
5.4K
2K
.10μf
IC-P
555
1K
1/6 IC-V
Ø2-ACIA CLOCK OUT
470Ω
(TYPICAL FOR A10-A15)
A10
A11
A12
A13
A14
A15
MATCH


MATCH
IC-8
1702A
ADDRESS BUS AT 2102's
6850
ACIA
R DATA
T DATA
IRQ
DCD
R/W
SEE DIAGRAM 3 FOR INTERFACE CIRCUITRY
USER
6820 PIA
6850 ACIA
6830L7
MIKBUG
6530 TIM
6530 KIM
Vcc
4.7K
(TYPICAL FOR 8 DATA LINES)
470Ω
DATA DIRECTION
8T26
D0
D1
D2
D3
D4
D5
D6
D7
1/4 IC-O
1/4 IC-N
1/6 IC-M
03
04
IC-G 2102
IC-H 2102
IC-I 2102
IC-J 2102
470Ω
(TYPICAL FOR A0-A9 AND R/W, Ø2, VMA, AND Ø2·VMA)
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
R/W
Ø2
VMA
Ø2·VMA
5.4K
2K
.10μf
IC-P
555
1K
1/6 IC-V
Ø2-ACIA CLOCK OUT
470Ω
(TYPICAL FOR A10-A15)
A10
A11
A12
A13
A14
A15
MATCH



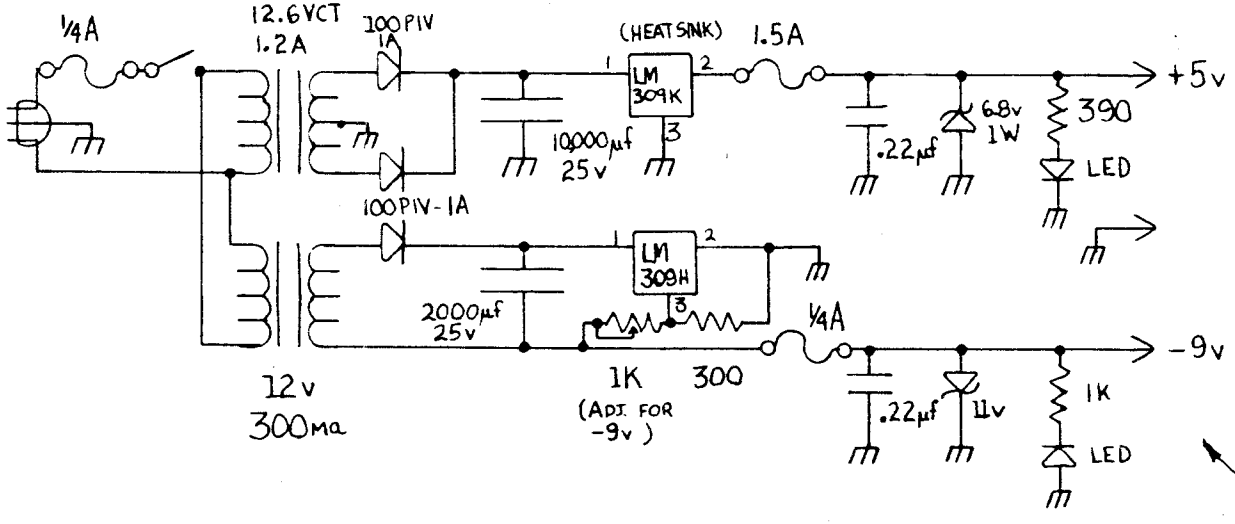
C1=C2=82 p.f.
R1=R2=22K



MINIMAL EXTERNAL CONTROLS

A-20

MODEL 400 - 6502 CONFIGURATION (PART 2)



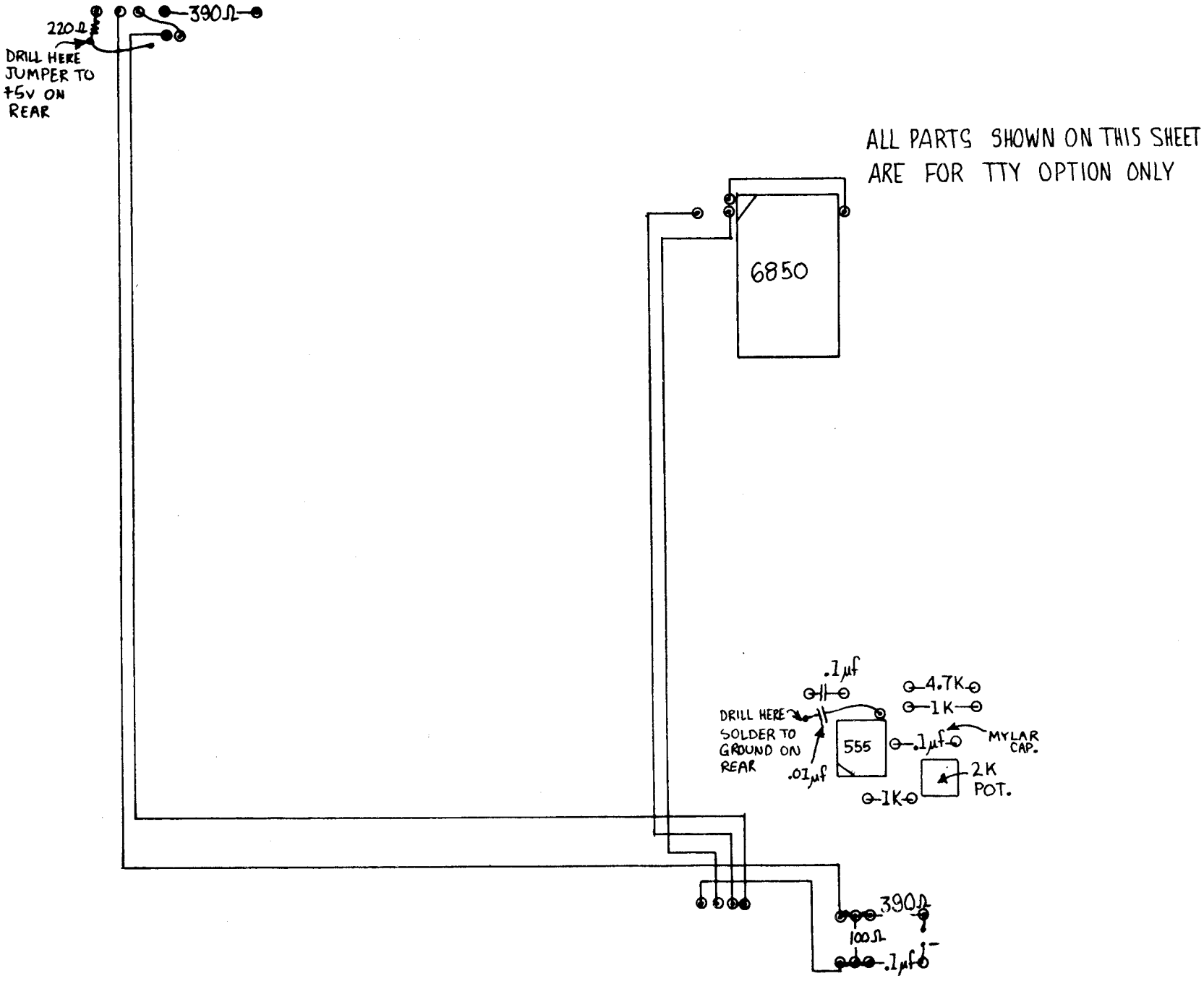
POWER REQUIREMENTS:

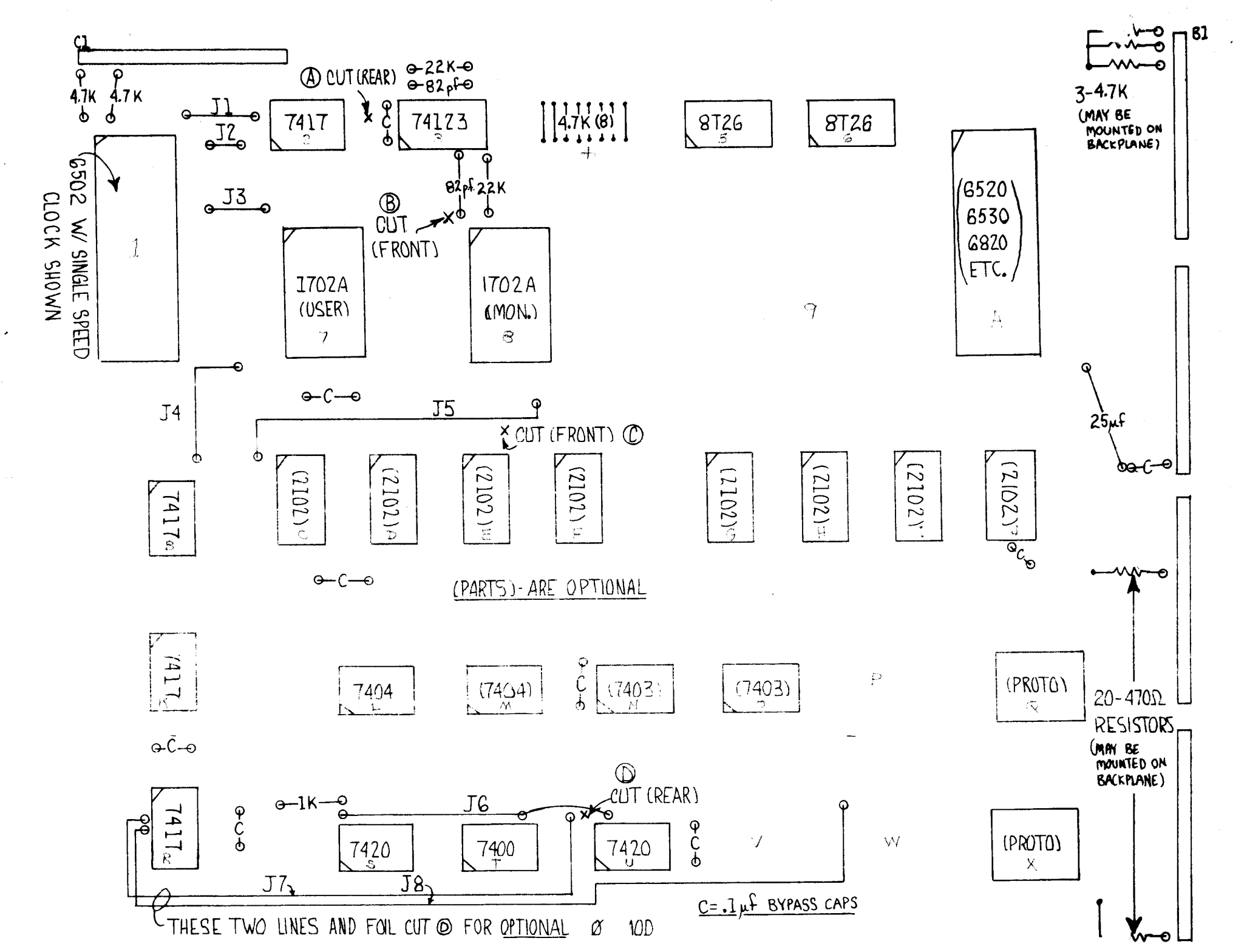
MINIMAL SYSTEM:
+5v @ 1A
-9v @ 140ma

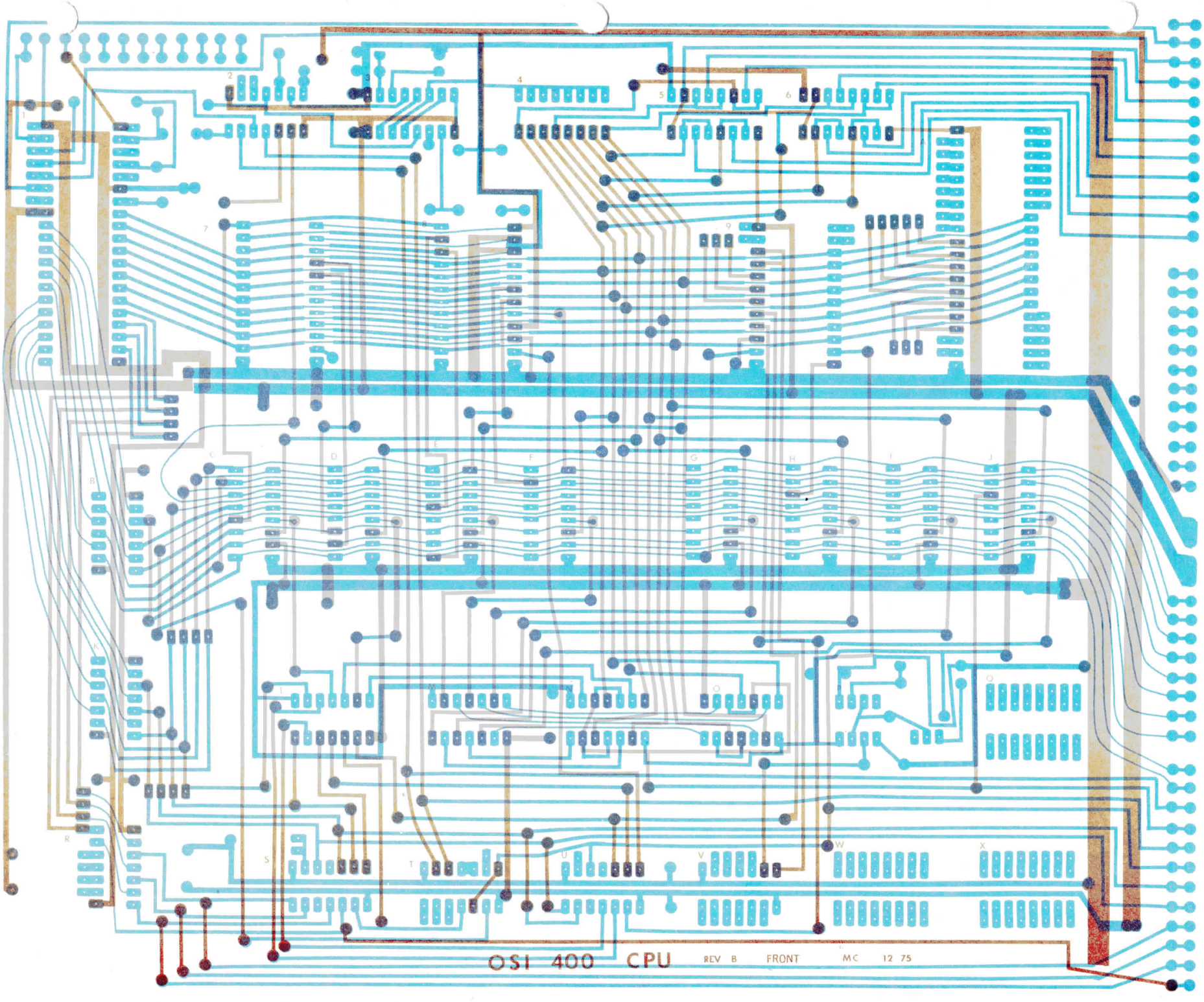
MIDI SYSTEM (8K + 2 I/O BOARDS):
+5v @ 5A
-9v @ 700ma

DOUBLY PROTECTED POWER SUPPLY FOR USE WITH MINIMAL SYSTEM

DIAGRAM 8


220Ω
390Ω
DRILL HERE
JUMPER TO
+5V ON
REAR
ALL PARTS SHOWN ON THIS SHEET
ARE FOR TTY OPTION ONLY
6850
.1µf
4.7K
1K
DRILL HERE
SOLDER TO
GROUND ON
REAR
555
.1µf
MYLAR
CAP.
.01µf
2K
POT.
1K
390Ω
100Ω
.1µf


C1
4.7K
4.7K
J1
J2
J3
J4
J5
J6
J7
J8
Ⓐ CUT (REAR)
22K
82pf
7417
74123
4.7K (8)
8T26
8T26
6502 W/ SINGLE SPEED CLOCK SHOWN
1
Ⓑ CUT (FRONT)
82pf
22K
1702A (USER)
1702A (MON.)
6520
6530
6820
ETC.
B1
3-4.7K (MAY BE MOUNTED ON BACKPLANE)
25µf
C
Ⓒ CUT (FRONT)
(2102)
7417
(PARTS) - ARE OPTIONAL
7404
(7404)
(7403)
(7403)
(PROTO)
20-470Ω RESISTORS (MAY BE MOUNTED ON BACKPLANE)
1K
Ⓓ CUT (REAR)
7420
7400
7420
(PROTO)
C=.1µf BYPASS CAPS
THESE TWO LINES AND FOIL CUT Ⓒ FOR OPTIONAL Ø 10D


OSI 400 CPU REV B FRONT MC 12 75

OSI MODEL 414V PARTS KIT (AS SUPPLIED BY OSI)

____ 1 - OSI 400 Superboard
____ 1 - 6502A
____ 1 - 65V PROM Monitor (1702A PROM)
____ 1 - 7400
____ 2 - 7403
____ 3 - 7404
____ 4 - 7417
____ 2 - 7420
____ 1 - 74123
____ 8 - 2102A Memories 650ns or faster. Use only "A" suffix or zero data hold time memories. (OSI supplied memories are 350ns. or better)
____ 2 - 8T26 Buffers
____ 3 - 1N914

RESISTORS--$\frac{1}{4}$watt 10% or better

____ 1 - 100
____ 1 - 220
____ 2 - 390
____ 21 - 470
____ 6 - 1K
____ 18 - 4.7K
____ 3 - 22K
____ 1 - 47K

CAPACITORS

____ 2 - 82pf to 100pf NPO (temperature stable)
____ 11 - Bypass capacitors .1uf 10V or better
____ 1 - OPTIONAL 25uf 10V or better electrolytic

OSI MODEL 414A PARTS KIT (AS SUPPLIED BY OSI)--DIFFERENCES FROM 414V PARTS KIT

Substitute:

____ 1 - OSI 65A PROM Monitor for OSI 65V PROM Monitor

Add:

____ 1 - 6850 ACIA
____ 1 - 555 or 1455 timer
____ 1 - .1uf temperature stable capacitor and .01uf bypass capacitor
____ 1 - 2K or 5K pot

OSI MODEL 415A PARTS KIT (AS SUPPLIED BY OSI)--DIFFERENCES FROM 414A PARTS KIT

Substitute:

____ 1 - 6800 for 6502A
____ 1 - 68A PROM Monitor for 65A PROM Monitor

Note: OSI supplied parts kits typically contain additional capacitors and resistors due to our packaging techniques and inventory procedures.

REQUIRED PARTS NOT SUPPLIED BY OSI--Solder wire, Power Supply, terminal or monitor and keyboard, an SPST switch, and Case.

RECOMMENDED ACCESSORIES-- Sockets: 2 - 40 pin, 3 - 24 pin. Card Connectors: 5 - 12 pin plugs and sockets Molex KK-156 series. OSI offers a backplane board using Molex part #09-52-3121 connectors on boards and #09-64-1121 connectors on backplane.

SYSTEM EXPANSION-- 1 - 6820 PIA (16 I/O lines), 1 - 1702A PROM (user program), 1-7420 Address Decoding, 1 - 7402 Address Decoding, and any of OSI's 12 system compatible accessory boards.

Construction of the 414 or the 415A

Although building a computer is much simpler today than a few years ago, it is still no trivial task. If you are not experienced in fine detail electronic assembly, please enlist the aid of someone who is.

REQUIRED ITEMS

1. Fine tipped soldering iron
2. Fine gauge 60% tin 40% lead core solder
3. Hookup (#22) copper wire (preferably tinned)
4. Wire cutters, needle nose pliers, tweasers, etc.
5. All parts listed in the 414 or 415A parts list
6. A good, clean, well lit working area and lots of patience
7. 5 to 10 hours assembling time

GENERAL TIPS FOR INSTALLING ICs ON THE SUPERBOARD

Most hobby computer authors strongly recommend the use of sockets on all ICs on a computer. However, our own repair experience has been that bad sockets are the number two cause of kits not working. (Bad soldering is the number one cause) Use only medium or high quality sockets and insert and remove ICs only when absolutely necessary.

CONSTRUCTION

Step 1 Visual Inspection

Inspect both sides of the board for foil bridges and tape cuts (scratches). The board has been inspected twice before you have received it so foil bridges are quite unlikely. Refer to the schematic before cutting any tapes apart. If there are any deep scratches, especially in the areas along the .015" foils, simply solder the foil across the scratch.

Step 2 Board Modifications

Refer to the accompanying red/blue artwork and tissue overlays in conjunction with these instructions.

Foil Cuts:

- On all versions, cut the foil leading to Pin 16 of IC-E. This cut is Ⓒ on the overlay.
- On all 6502 systems, cut the foil from Pin 4 of IC-2 as shown by Ⓑ.
- On 6502 systems using the external clock circuit of App Note 4A, cut the foil from Pin 9 of IC-2, shown as Ⓐ.
- Optional foil cut D is discussed later in the construction details.

Summary of Step 2:

Cut Ⓒ and optionally cut Ⓐ and Ⓑ.

Step 3 Pull Up Resistors

Install the resistors indicated on the parts overlay as follows:

At IC-4, install 8 - 4.7K resistors (Pin 1 to Pin 16, Pin 2 to Pin 15, Pin 3 to Pin 14, etc.) Install the 1K resistor from +5 to pin 13 of IC-S as shown. Install three 4.7K resistors from the +5 bus (the wide tape running nearly the full height [8" dimension] of the board) to B_2, B_3, and B_4. These resistors must be soldered to this tape by laying the leads directly on the tape. Install 20 - 470 ohm resistors from the +5 bus to B_{29} through B_{48} (B_{29}, B_{30}, B_{31}, etc.)

There are two alternate procedures for installing the 23 resistors at the end of the board. The resistors can be installed standing up with the +5 being supplied via a large wire to all the resistors. When a backplane is used with the board, the bus pull ups can be installed on the backplane

instead. However, the superboard will not operate stand-alone with this modification.

Summary of Step 3

A. Install 8 - 4.7K resistors at IC-4

B. Install 1 - 1K resistor from Pin 13 of IC-S to +5

C. Install 3 - 4.7K pull ups from B_2, B_3 and B_4 to +5

D. Install 20 - 470 ohm pull ups from B_{29} through B_{48} to +5

Step 4 Capacitors

The Superboard uses nine .1uf capacitors on the +5 bus for bypassing along with a 25uf electrolytic. A .1uf bypass is provided for the -9. The locations of the .1uf capacitors are indicated on the overlay by a capacitor symbol. These capacitors are located in the following areas:

1. To the immediate left of IC-3
2. Near Pin 12 and 13 of IC-7
3. Near Pin 9 of IC-C and Pin 8 of IC-D
4. Near Pin 9 of IC-J
5. Between IC-K and IC-R
6. Between IC-R and IC-S
7. Between IC-M and IC-N
8. Near Pin 8 of IC-O and Pin 8 of IC-P
9. Between IC-U and IC-V

Additionally the 25uf electrolytic and .1uf -9V bypass are located near B_{24} on the card edge. Install all capacitors upright.

Summary of Step 4

1. Install the 9 - .1uf +5 bypass capacitors
2. Install the .1uf -9V bypass capacitors
3. Install the 25uf +5 filter capacitor

Step 5 Jumpers

Install a jumper (J5) which ultimately goes from Pin 1 of IC-C to Pin 18 of IC-8. Install a jumper from Pin 13 of IC-S to Pin 13 of IC-U.

Jumpering for the Front Panel Option Pin 9 of IC-T is Front Panel Control C(FPCC). If a front panel is used, jumper it to the front panel via the control connector. If a front panel is not used, jumper it to pin 13 of IC-S (J6).

The pad at the 7417 side of J4 (directly above pin 16 of IC-B) is FPC(B). Connect FPC(B) to the front panel via the control connector or jumper it to +5 volts (J4).

The pad at the right end of J3 (also connected to Pin 5 of IC-2) is FPC(A). When a front panel is used, a 1N914 is connected between Pin 34 (cathode) of IC-1 and FPC(A). FPC(A) [(anode) instead of J3] is also jumpered to the front panel through the control connector. If a front panel is not used, replace the diode with a jumper. If a diode is used, a 4.7K pull up must always be present on the anode side of the diode for proper operation.

Summary of Step 5

1. Jumper Pin 1 of IC-C to Pin 18 of IC-8.
2. Jumper Pin 13 of IC-S to Pin 13 of IC-U.
3. Jumper FPC(A), (b), and (C) appropriately.

Step 6

Install the ICs specified in the overlay on the FRONT of the board. Be careful to observe Pin 1 orientations. The ICs in parenthesis should be omitted if the board is to be used immediately with an external memory board. If expansion to additional memory above 1K is EVER anticipated, socket the chips in parenthesis so that they can be easily removed.

If the 400 board is to be used as a stand-alone computer, the two 8T26 buffers can be omitted.

Step 7

Install the socket for IC-8. DO NOT INSTALL THE PROMS AT THIS POINT.

Step 8 Initial Testing

About 60% of the board can now be tested with a power supply, some jumper leads, and a DC voltmeter. A current limited +5volt supply can now be connected to B_{26} (+5) and B_{28} (ground). +5 should also be supplied to FPC(B). The board should draw lamp or less. Verify that +5 is available to all ICs. All pulled up bus lines should be at a logical high. All data lines should be at a logical high when tested at the data bus pull ups. The address lines AT THE PROCESSOR should be brought low one at a time and confirmed at the bus connector and PROM socket. When the board passes these tests, the address decoder can be tested by jumpering the appropriate lines to ground at the bus connector and checking the chip enables for the 2102 memories, the PROM, and the ACIA.

If a front panel is available, full RAM Read/Write capability should now be present.

Step 9 ACIA

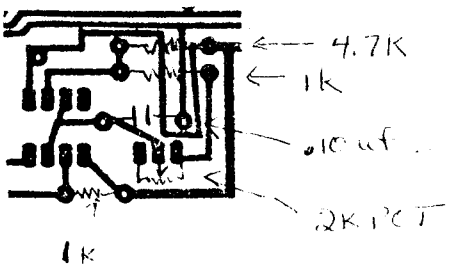
OMIT STEP 9 ON 414V KITS

Install the ACIA socket (if used) at IC-9. DO NOT INSTALL THE ACIA at this time. Install a jumper from Pin 1 of IC-9 to Pin 23 of IC-9.

Install a jumper from Pin 6 of IC-9 to Pin 11 of IC-V as shown on the serial interface overlay. Install a 7404 at IC-V.

ACIA CLOCK

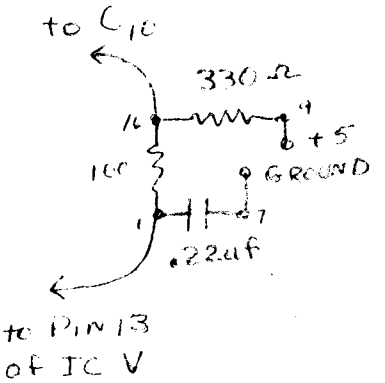
Install the 2 - 1K resistors, the 4.7K resistor, the .1uf capacitor, and the pot as shown below and on the serial interface overlay. Be sure to use a zero temperature coefficient capacitor, not a common bypass capacitor.



Refer to Diagram 3 for the schematic of this installation. Install either the Teletype interface or the RS-232C interface (not both).

Teletype Interface

Follow the following diagram for Teletype operation. The components shown are installed at IC-W and are shown on the serial interface overlay.



Install a jumper from Pin 2 of IC-9 to pin 12 of IC-V. Install a jumper from Pin 10 of IC-V to Pin 13 of IC-2. Install a jumper from Pin 12 of IC-2 to C_{11}. Install a 390 ohm resistor from C_{12} to -9V. (The upper most foil on the front of the board).

Improved RS-232C Interface

Diagram 3, revision 3.0 shows improved RS-232 interfaces. The RS-232 circuits will work with virtually any small signal transistors. The 7404s are used to protect the rather expensive ACIA in case of a circuit failure. They could be omitted. This schematic superceeds Diagram 3 (op amp interfaces) of early 400 manuals.

TVT Connections

To interface the 400 system to a TV Typewriter, install the RS-232 interface as per Diagram 3. On the TVT's serial interface board remove all jumpers to the UART (pins 33,35,38 and 39). This configures the TVT for 8 bits with no parity and two stop bits. Ground pin 8 of the TVTs I/O connector for full duplex operation and connect the 400 system to the TVT as follows:

400 System	TVT
Ground	Ground
C_{10}	I/O 6
C_{11}	I/O 7

Be sure that both the 400 system and the TV Typewriter are set for the same baud rate.

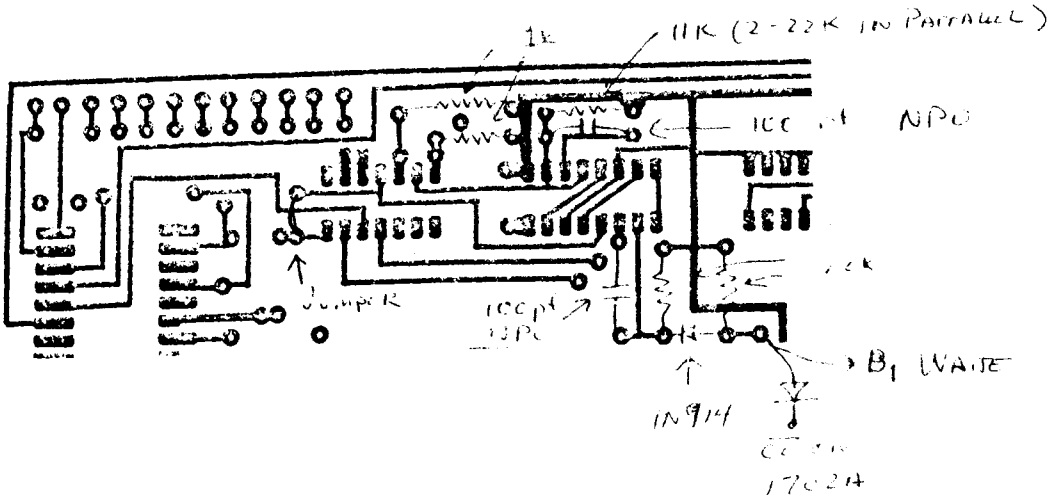
Step 10 MPU and Clock

Install 4.7K pull ups from C_1 and C_3 to +5 which is available just above Pin 1 of IC-1. Refer to the following list for pin grounding (Pins 1, 21, and 35 are already grounded).

Processor	Grounds
6502	5, 36, 38
6501	38, 39
6800	38, 39

6501 and 6800 Installation

Jumper Pin 36 to Pin 37 of IC-1. Jumper Pin 3 of IC-1 to Pin 8 of IC-2. Jumper Pin 37 of IC-1 to Pin 10 of IC-2. Install a 74123 at IC-3. Install the clock parts as shown in the following diagram.



6502

Refer to App Note #4A for 6502 clocks. It is recommended that the user start with the single speed clock and later up-grade to the multi-speed clock. The single speed clock components are shown on the construction overlay along with J1, J2, and foil cut A which make up the appropriate clock circuit.

Step 11 More Testing

Apply all power supply voltages to the board. With a 270 ohm resistor across the voltmeter's leads, check all pins on the processor, PROM, and ACIA. Verify power and check outputs which should be low. Inputs and bi-directional lines should be between 0 and +5 volts. With a scope and/or frequency meter, check and adjust the ACIA clock for the proper baud rate.

In 6501 and 6800 systems, the processor clock should be running with Ø2 twice as long as Ø1 with the address line high (FFFF). Ø1 should be approximately 500ns and Ø2 should be approximately 500ns and Ø2 should be 1us. By bringing A_{15} low, Ø2 should drop to 500ns. On 6502 systems, an approximately 700KHz signal should be present at J1.

Step 12 Final Testing

Install the MPU, 1702A, and ACIA (with power off, of course). On 6502 systems, initially adjust the clock resistors for 700KHz to 1MHz operation. If a 20ma loop is used, the two receiver inputs should be jumpered together.

On Serial Systems

The ACIA should output two serial words at Pin 6 of IC-9 each time reset is returned high from a low. The processor is now running in the monitor command loop. The address lines should indicate addressing in the FEXX range and complicated patterns should be present on tha data bus and the 1702A chip enable (Pin 14) of IC-8. The ACIA should regularly be enabled. R/W should always be high and the 2102s should not be enabled. Now, by opening the jumper on the current loop interface or by taking the RS-232C input below -3 volts and holding that condition, R/W should go low a few times in step with the baud rate selected and the 2102's chip enable should have similar patterns.

Step 11 More Testing

Apply all power supply voltages to the board. With a 270 ohm resistor across the voltmeter's leads, check all pins on the processor, PROM, and ACIA. Verify power and check outputs which should be low. Inputs and bi-directional lines should be between 0 and +5 volts. With a scope and/or frequency meter, check and adjust the ACIA clock for the proper baud rate.

In 6501 and 6800 systems, the processor clock should be running with Ø2 twice as long as Ø1 with the address line high (FFFF). Ø1 should be approximately 500ns and Ø2 should be approximately 500ns and Ø2 should be 1us. By bringing A_{15} low, Ø2 should drop to 500ns. On 6502 systems, an approximately 700KHz signal should be present at J1.

Step 12 Final Testing

Install the MPU, 1702A, and ACIA (with power off, of course). On 6502 systems, initially adjust the clock resistors for 700KHz to 1MHz operation. If a 20ma loop is used, the two receiver inputs should be jumpered together.

On Serial Systems

The ACIA should output two serial words at Pin 6 of IC-9 each time reset is returned high from a low. The processor is now running in the monitor command loop. The address lines should indicate addressing in the FEXX range and complicated patterns should be present on tha data bus and the 1702A chip enable (Pin 14) of IC-8. The ACIA should regularly be enabled. R/W should always be high and the 2102s should not be enabled. Now, by opening the jumper on the current loop interface or by taking the RS-232C input below -3 volts and holding that condition, R/W should go low a few times in step with the baud rate selected and the 2102's chip enable should have similar patterns.

When the board passes these tests, it is very unlikely that anything is wrong.

On 414V systems, an OSI 440 Video Graphics Board is necessary to test the CPU. With the two boards connected together, reset should clear the video screen and should place six digits in the upper left hand corner of the screen.

Step 14 Connection to a Terminal

The 20ma loop connections for an ASR-33 Teletype are shown in Diagram 3. Any half duplex jumpers should be removed. The teletype chassis should be connected to the power supply ground. The resistors indicated may need to be adjusted for 20ma currents.

For RS-232C connections, refer to the documentation supplied with the computer terminal.

Operation with Superbug Monitors

As stated earlier, connect the board to a terminal, appropriate power supply, and a front panel consisting of at least a reset switch. Power everything up and momentarily reset. The terminal should respond with a carriage return then line feed. You should now be in the monitor command loop. Refer to the approptiate OSI PROM Monitor write up for details of operation.

Front Panel Operation

On Superboard systems using only a front panel, connect the completed board to the front panel and a power supply. Turn the unit on, set the Run/Halt switch to halt, and set the front panel enable switch to enable. To load and examine memory, set the address switches to the desired memory location. The data lights will now show the contents of that location. By momentarily actuating the load switch, the data specified by the data switches will be loaded in to the memory location specified by the address switches. Load the following simple jump program to verify operation.

6800	
Location	Data
FFFE	00
FFFF	00
0000	7E
0001	00
0002	00

6501, 6502	
Location	Data
FFFC	00
FFFD	00
0000	4C
0001	00
0002	00

Next, bring reset low. Then bring run high and then reset high. The processor should now be in a tight jump loop. The address lights should show a 0003 (A superimposition of 0000, 0001, and 0002). The data lights should all be on since they are gated by Ø2. A front panel or 65A or 65V equipted 6501 or 6502 Superboard can be used directly with the OSI Model 300 Computer Trainer Lab Manual which has 20 experiments in basic machine language programming.

User Support

As of this manual revision, there are approximately 2,000 OSI 400 boards in use around the world. Uses and lots of software for the OSI 400 system are the topics of a regular bimonthly publication, the OSI Systems Journal.

The Journal costs $6.00 for a one year subscription. Subscriptions can be obtained from:

The OSI Systems Journal
P. O. Box 134
Hiram, Ohio 44234

Factory Documentation

MOS Technology offers the 650X Hardware and Programming Manuals which have about 400 pages of useful information on the 6501 and 6502. This set of manuals is available directly from MOS Technology for $10.00. MOS Technology is located at Valley Forge Corporate Center; 950 Rittenhouse Road; Norristown, Pennsylvania 19401.

The 6800 series specification sheets are offered by Motorola and AMI (American Microsystems International) free of charge through most of the major nation-wide industrial distributors including Arrow Electronics, Pioneer/Standard, and Schweber Electronics.

Motorola also offers the M6800 Microprocessor Applications Manual and the M6800 Microprocessor Programming Manual; totaling about 800 pages. They are available from the above distributors for $25.00 per set.

Refer to the "Yellow Pages" of a large city near you (500K population) for the address of the branch offices of these distributors nearest you.

Series 54/74

DM5407/DM7407,DM5417/DM7417 (SN5407/SN7407,SN5417/SN7417) hex buffers/drivers

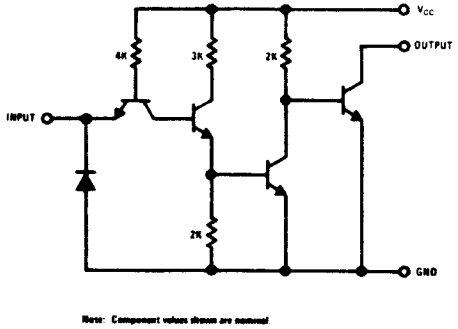
general description

These TTL hex buffers/drivers are fully compatible for use with TTL and DTL logic circuits. Each buffer features high-voltage, open-collector outputs (DM5407/DM7407 30V minimum breakdown and DM5417/DM7417 15V minimum breakdown). These buffers also feature high sink current capability (DM5407, DM5417 30 mA and DM7407, DM7417 40 mA).

features

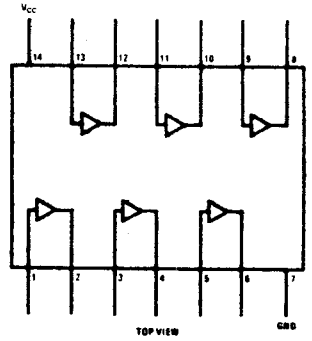
- Input clamp diodes
- High voltage open-collector outputs
  - DM5407/DM7407 30V
  - DM5417/DM7417 15V
- High sink current capability
  - DM5407,DM5417 30 mA
  - DM7407,DM7417 40 mA
- 14 ns typical propagation delay time
- 145 mW typical power dissipation

schematic and connection diagrams



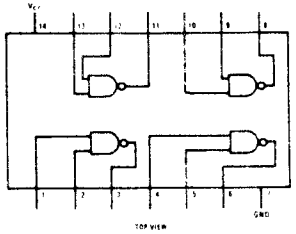
Note: Component values shown are nominal

Dual-In-Line and Flat Package



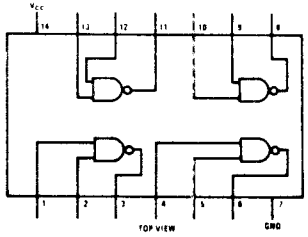
DM5400/DM7400

Dual-In-Line Package



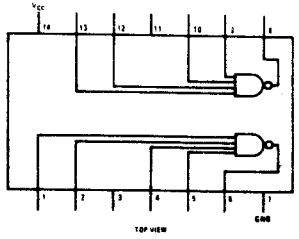
DM5403/DM7403

Dual-In-Line Package



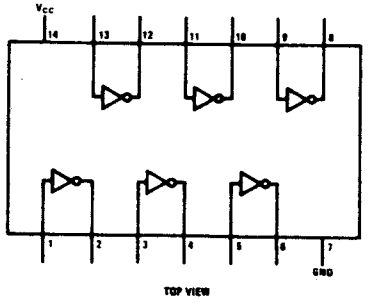
DM5420/DM7420

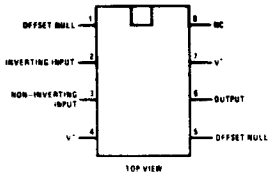
Dual-In-Line Package



DM5404/DM7404

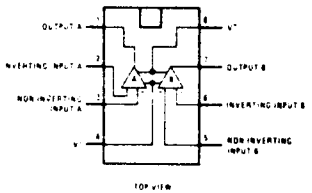
Dual-In-Line Package





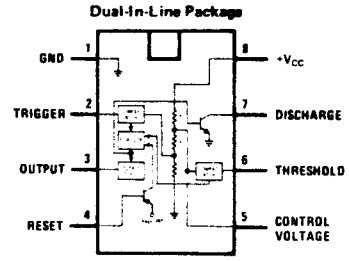
Order Number LM741CN
See Package 20

Dual-In-Line Package



Order Number LM1458N
See Package 20

Dual-In-Line Package



TOP VIEW
Order Number LM555CN
See Package 20

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\ R_B)\ C}$$

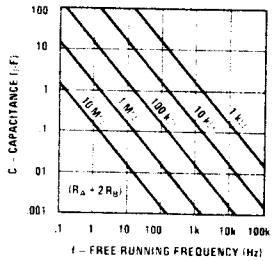


FIGURE 6. Free Running Frequency

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$