OHIO SCIENTIFIC

Comprehensive Information Package II

for reference & service

FALL '77

CONTENTS

B1 - WAIT
2 - NMI
3 - IRQ
4 - Data Direction
5 - D0
6 - D1
7 - D2
8 - D3
9 - D4
10 - D5
11 - D6
12 - D7

B13 - *
14 - *
15 - *
16 - *
17 - *
18 - *
19 - *
20 - *
21 - *
22 - *
23 - *
24 - -9volts

*User for PIA or Other Signals

B25 - +5volts
26 - +5volts
27 - ground
28 - ground
29 - A6
30 -A7
31 - A5
32 - A8
33 - A9
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B37 - A4
38 - A0
39 - Ø2
40 - R/W
41 - VMA
42 - Ø2·VMA
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44 - A11
45 - A12
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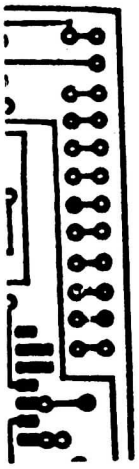
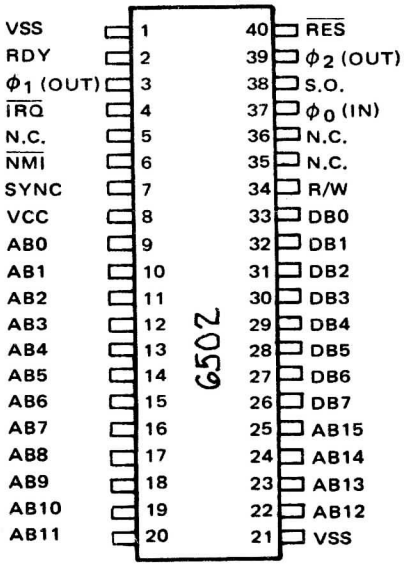
47 - A14
48 - A15

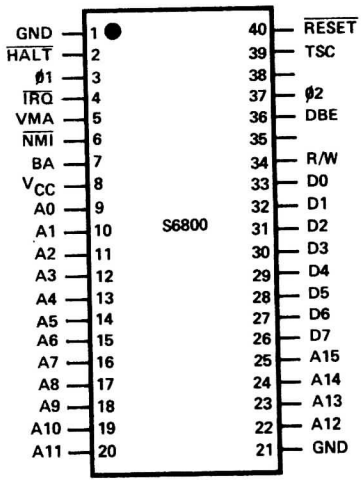


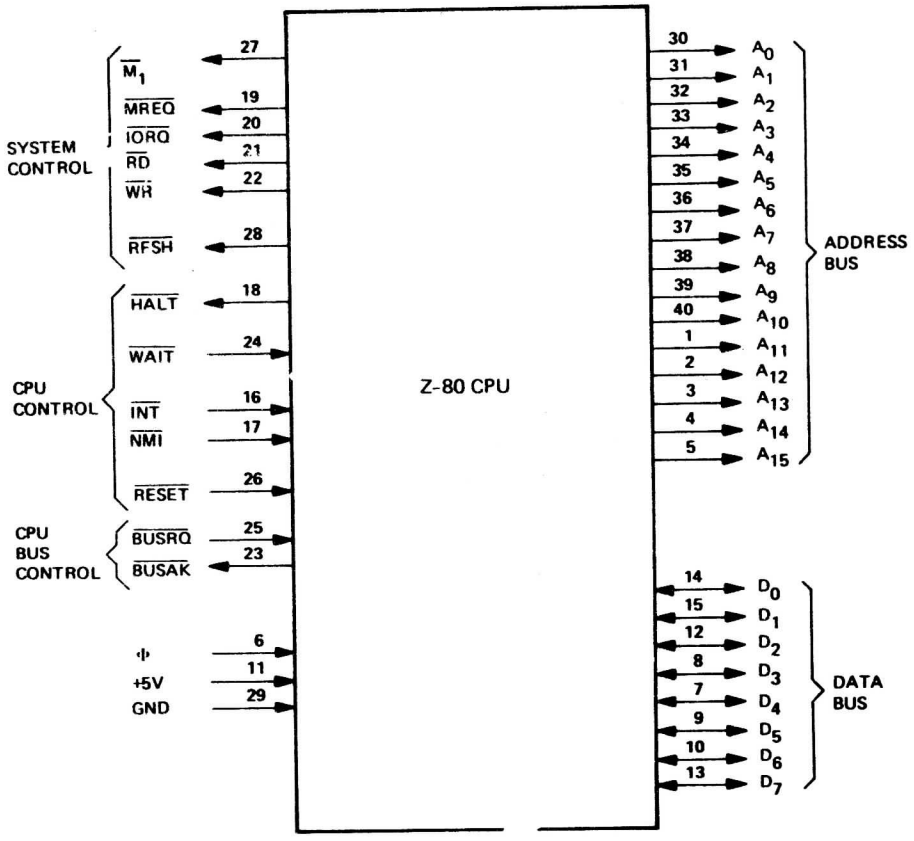
C1 - Processor RDY or $\overline{\text{HLT}}$
C2 - Power Ground
C3 - $\overline{\text{RESET}}$
C4 - *
C5 - *
C6 - *
C7 - *
C8 - *
C9 - Serial Trans. G or +
C10- Serial Receiver
C11- Serial Transmitter
C12- Serial Receiver G or -

*User and for Front Panel Control Functions

Diagram 4.



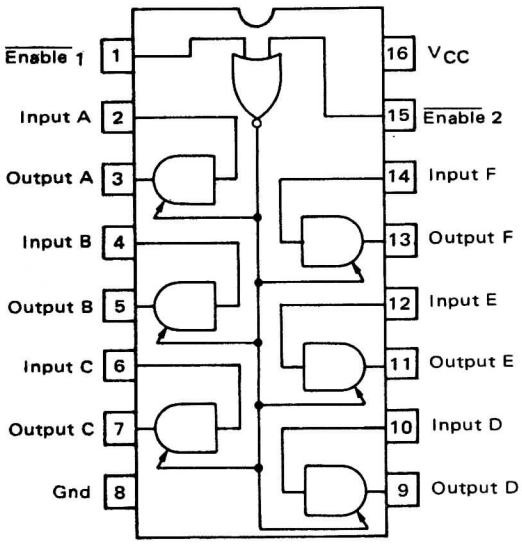




Z-80 PIN CONFIGURATION

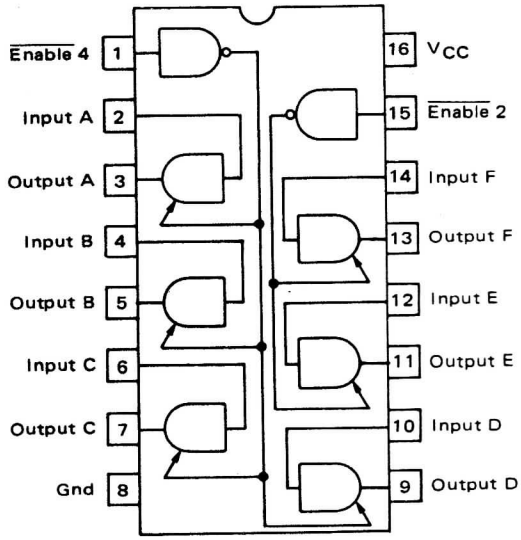
BUFFERS/DRIVERS

XC6885/XC8T95



Enable 2	Enable 1	Input	Output
L	L	L	L
L	L	H	H
L	H	X	O
H	L	X	O
H	H	X	O

XC6887/XC8T97



Enable	Input	Output
L	L	L
L	H	H
H	X	O

L = Low Logic State
H = High Logic State
O = High Impedance State
X = Irrelevant

PIN CONNECTIONS — MC6880 MC8T26

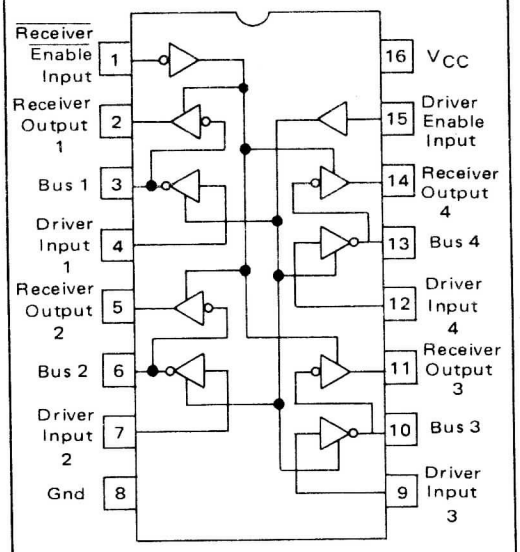
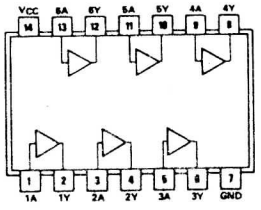


TABLE 1		
B/E	I/E	OPERATION
0	0	Driver Disabled, Receiver Enabled
0	1	Driver Disabled, Receiver Disabled
1	0	Driver Enabled, Receiver Enabled
1	1	Driver Enabled, Receiver Disabled

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

17

positive logic:
Y = A

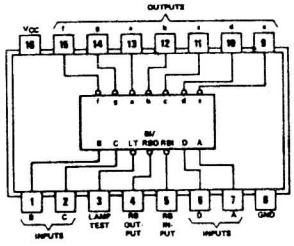


SN5417 (J, W) SN7417 (J, N)

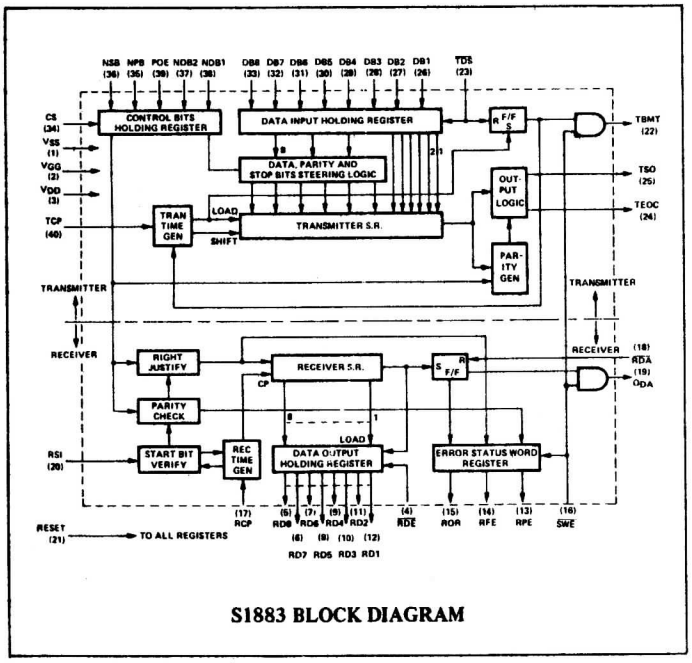
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

46 ACTIVE-LOW, OPEN-COLLECTOR, 30-V OUTPUTS

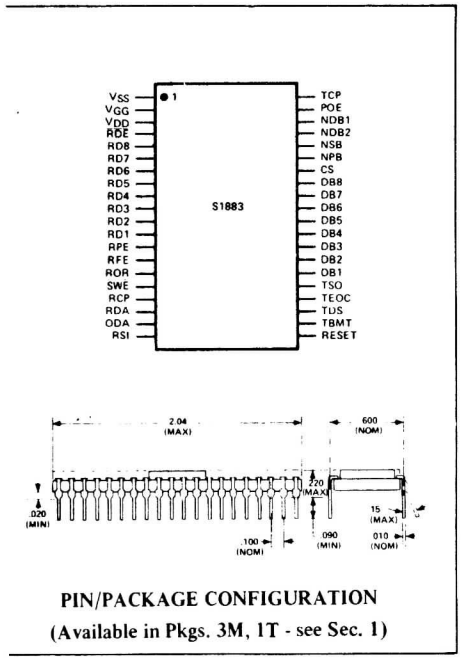
47 ACTIVE-LOW, OPEN-COLLECTOR, 15-V OUTPUTS



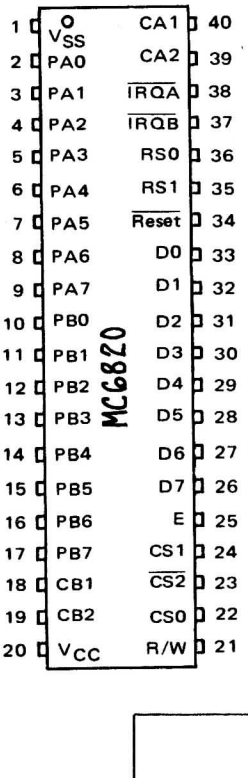
SN5446A (J, W) SN7446A (J, N)
SN54L46 (J) SN74L46 (J, N)
SN5447A (J, W) SN7447A (J, N)
SN54L47 (J) SN74L47 (J, N)
SN54LS47 (J, W) SN74LS47 (J, N)

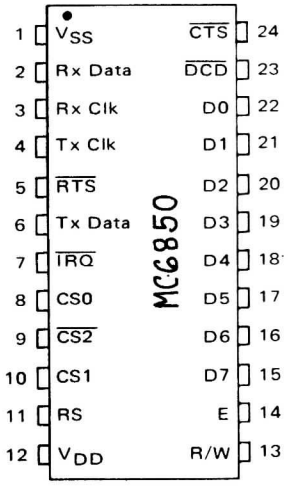


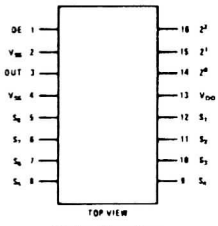
S1883 BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 3M, 1T - see Sec. 1)

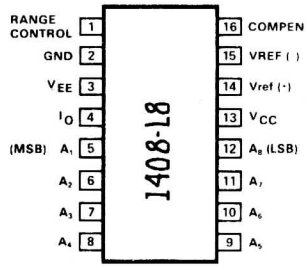






Order Number
AM3705D or AM3705CD
See Package 2
AM3705F or AM3705CF
See Package 5

F,N PACKAGE*



*N = Plastic DIP
F = Cerdip

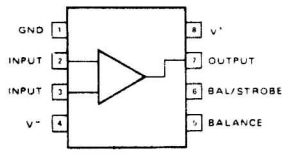
truth table

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	ON
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

AM3705 - 8 CHANNEL ANALOG MULTIPLEXER

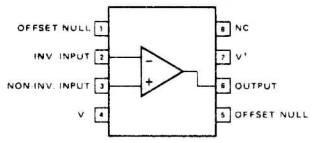
I/O DEVICES / LINEAR

N PACKAGE

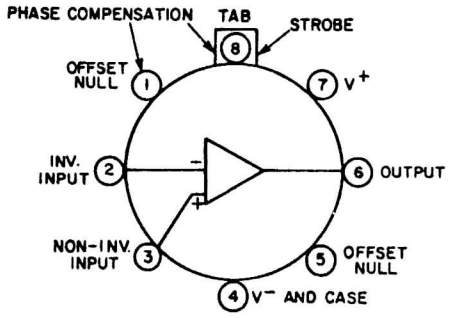


ORDER PART NO.
LM211N/LM311N

N PACKAGE



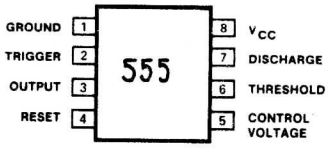
ORDER PART NO.
μA741N
μA741CN
SA741CN



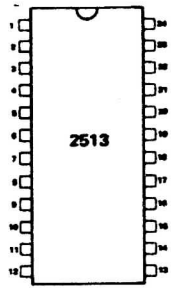
92CS-24713

Fig. 1—Functional diagram of the CA3130 Series.

N PACKAGE



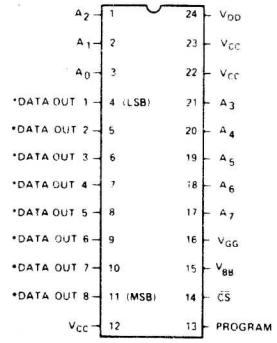
N/I PACKAGE



1.	V_{GG}	24.	V_{CC}
2.	NC	23.	NC
3.	NC	22.	Address 9
4.	Out 1	21.	Address 8
5.	Out 2	20.	Address 7
6.	Out 3	19.	Address 6
7.	Out 4	18.	Address 5
8.	Out 5	17.	Address 4
9.	NC	16.	Address 3
10.	Ground	15.	Address 2
11.	Chip Enable	14.	Address 1
12.	V_{DD}	13.	NC

CHARACTER GENERATOR ROM

PIN CONFIGURATION



*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

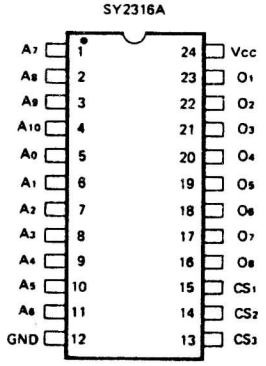
PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

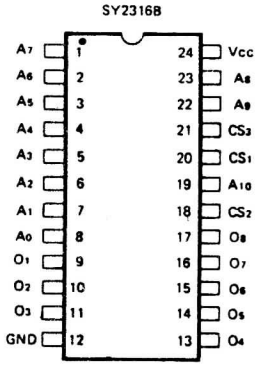
1702A

PIN CONFIGURATION

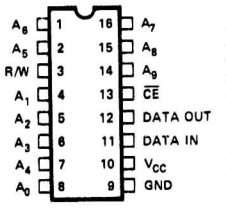
SY2316A



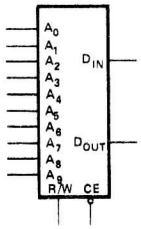
SY2316B



PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

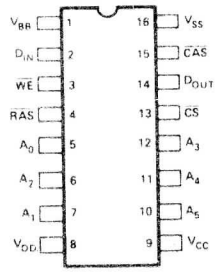
D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{CC}	POWER (+5V)

TRUTH TABLE

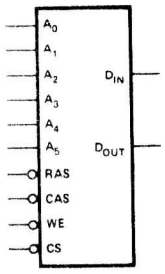
$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

2102A

PIN CONFIGURATION



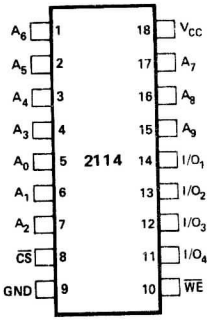
LOGIC DIAGRAM



PIN NAMES

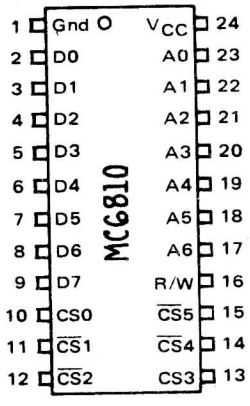
A_0 A_5	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

2104



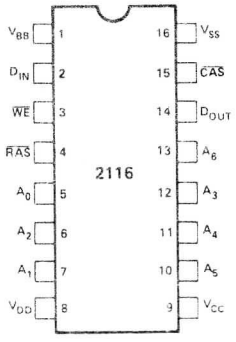
PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

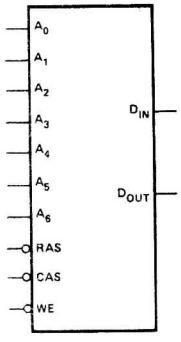


RAM

PIN CONFIGURATION



LOGIC SYMBOL



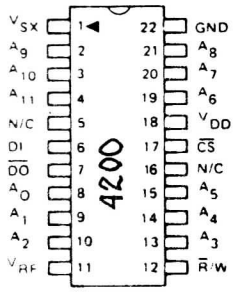
PIN NAMES

A_0 - A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

22 PIN DUAL IN-LINE

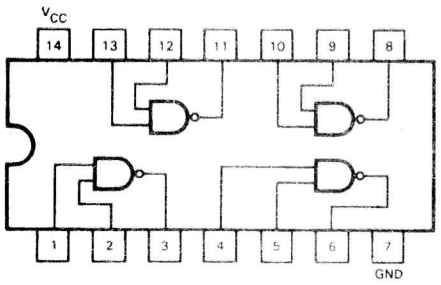
PIN	SYMBOL	FUNCTION
1	V_{SX}	Supply Voltage (−5V)
2	A_9	Address Input
3	A_{10}	Address Input
4	A_{11}	Address Input
5	N/C	
6	D_1	Data In
7	$\overline{D_0}$	Data Out
8	A_0	Address Input
9	A_1	Address Input
10	A_2	Address Input
11	V_{RF}	Supply Voltage (5V)
12	$\overline{R}/W$	Read/Write Input
13	A_3	Address Input
14	A_4	Address Input
15	A_5	Address Input
16	N/C	
17	$\overline{CS}$	Chip Select
18	V_{DD}	Supply Voltage (12V)
19	A_6	Address Input
20	A_7	Address Input
21	A_8	Address Input
22	GND	Ground

TOP VIEW



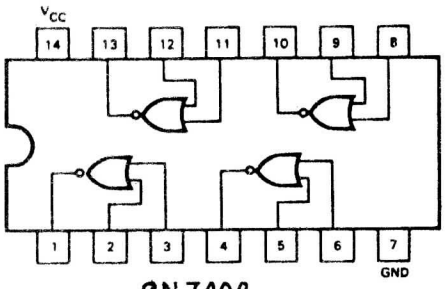
PIN ASSIGNMENT

QUAD 2-INPUT NAND GATE



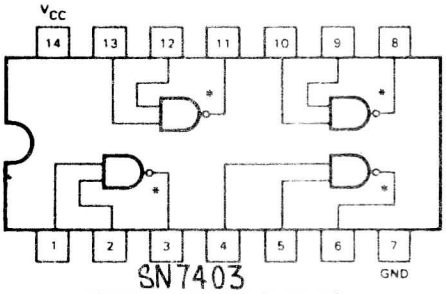
SN7400

QUAD 2-INPUT NOR GATE



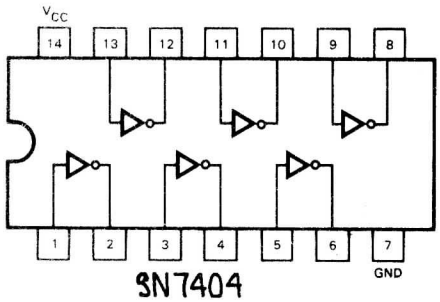
SN7402

QUAD 2-INPUT NAND GATE



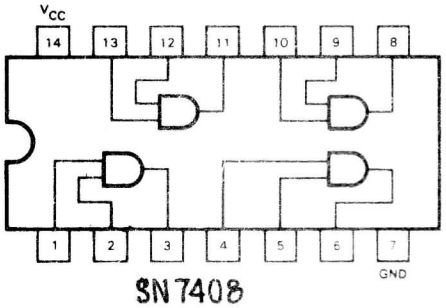
SN7403
*OPEN COLLECTOR OUTPUTS

HEX INVERTER



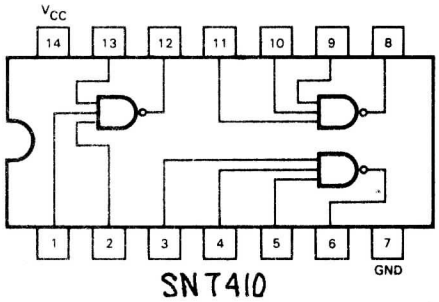
SN7404

QUAD 2-INPUT AND GATE



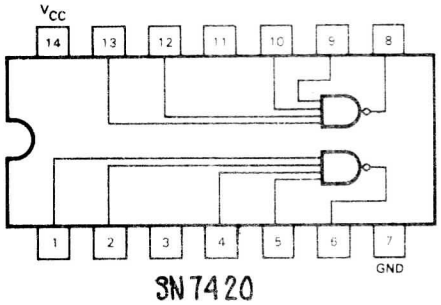
SN7408

TRIPLE 3-INPUT NAND GATE



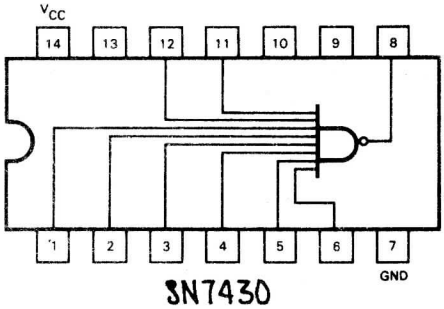
SN7410

DUAL 4-INPUT NAND GATE



SN7420

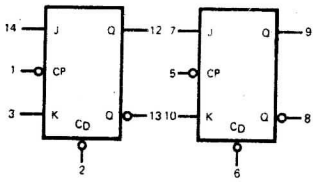
8-INPUT NAND GATE



SN7430

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Reset (Clear)	L	X	X	L	H
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$



V_{CC} = Pin 4
GND = Pin 11

SN7473

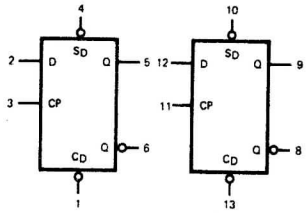
DUAL J-K FLIP FLOPS

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.



V_{CC} = Pin 14
GND = Pin 7

SN 7474

DUAL D-TYPE FLIP FLOP

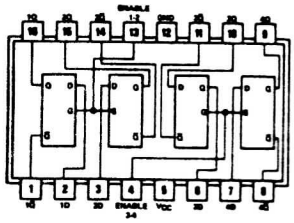
4-BIT BISTABLE LATCHES

75

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transistion of G



SN5475 (J, W) **SN7475 (J, N)**
SN54L75 (J) **SN74L75 (J, N)**
SN54LS75 (J, W) **SN74LS75 (J, N)**

DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

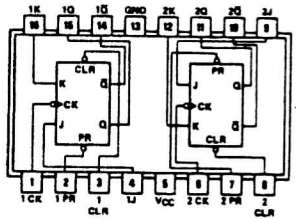
76

'76, 'H76
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

'LS76
FUNCTION TABLE

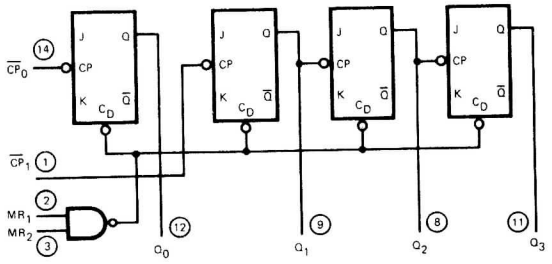
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$



SN5476 (J, W) **SN7476 (J, N)**
SN54H76 (J, W) **SN74H76 (J, N)**
SN54LS76 (J, W) **SN74LS76 (J, N)**

LOGIC DIAGRAM

SN7493- 4-BIT BINARY COUNTER

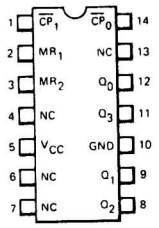


○ = Pin Numbers

V_{CC} = Pin 5

GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LS93
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input CP_1.

MONOSTABLE MULTIVIBRATORS

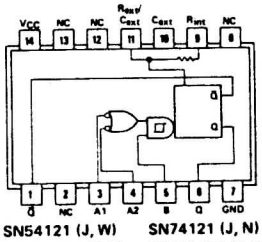
121

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

See page 6-64

NOTES: 1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext}.
2. To use the internal timing resistor, connect R_{int} to V_{CC}. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.



SN54121 (J, W) SN74121 (J, N)
SN54L121 (J, T) SN74L121 (J, N)
'121 . . . R_{int} = 2 kΩ NOM
'L121 . . . R_{int} = 4 kΩ NOM

NC—No internal connection

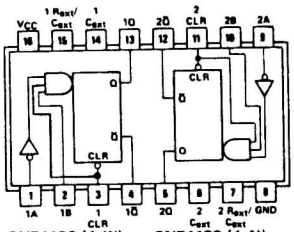
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

123

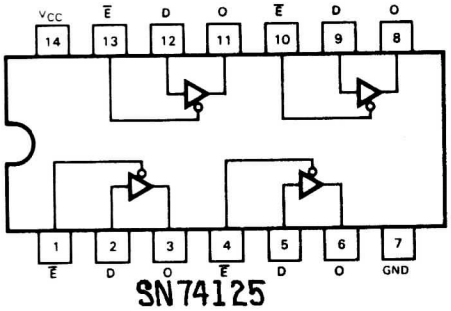
FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

See page 6-76

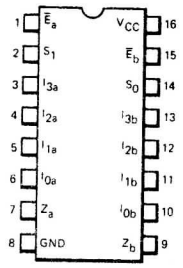


SN54123 (J, W) SN74123 (J, N)
SN54L123 (J) SN74L123 (J, N)
SN54LS123 (J, W) SN74LS123 (J, N)



SN74125

SN74125- QUAD TRI-STATE BUFFER



SN74153

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

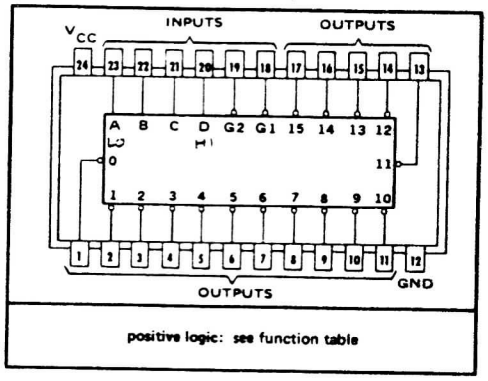
logic

FUNCTION TABLE

INPUTS						OUTPUTS													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

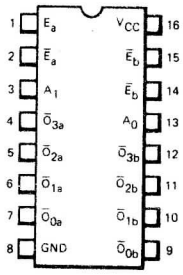
H = high level, L = low level, X = irrelevant

SN54154 . . . J OR W PACKAGE
SN54L154 . . . J PACKAGE
SN74154, SN74L154 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN 74154

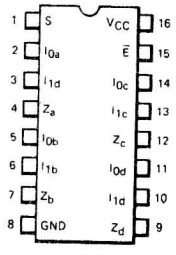


SN74155

TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{E}_b$	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care



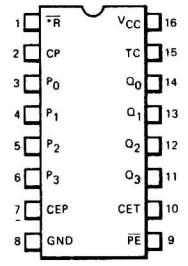
SN 74157

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TTL



SN74163

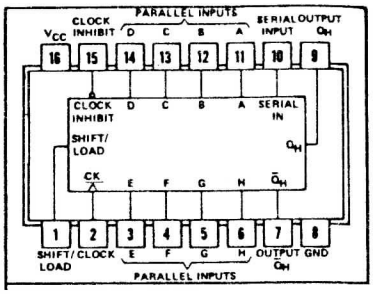
*$\overline{MR}$ for 160 and 161
*$\overline{SR}$ for 162 and 163

MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the 162 and 163 only.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

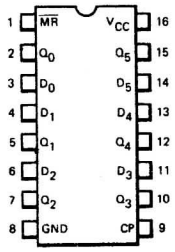
SN54165, SN54LS165 . . . J OR W PACKAGE
SN74165, SN74LS165 . . . J OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

SN74165



SN74174

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1
D	Q
H	H
L	L

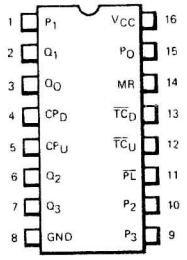
Note 1: t = n + 1 indicates conditions after next clock.

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asnyn.)
L	H	H	H	No Change
L	H	⌐	H	Count Up
L	H	H	⌐	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH Clock Transition

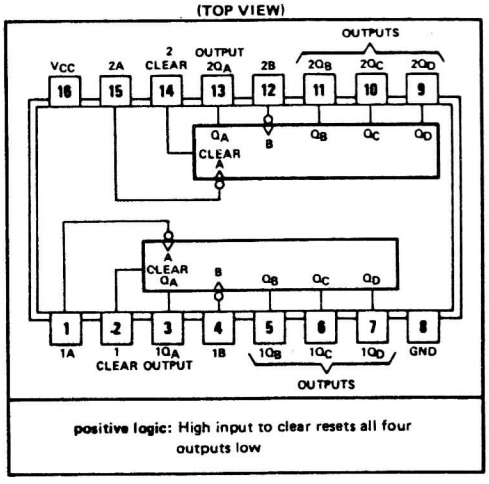
CONNECTION DIAGRAM
DIP (TOP VIEW)



SN74193

SN74390

SN54390, SN54LS390 . . . J OR W PACKAGE
SN74390, SN74LS390 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: High input to clear resets all four outputs low

'390, 'LS390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

FUNCTION TABLES
'390, 'LS390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. H = high level, L = low level.

Model 420C
4K Memory Board

Description:

The 420C is an extremely economical 4K by 8 RAM memory board which uses standard 2102 memories. The 420C features battery back-up capability when used with L-type 2102s. Battery back-up can be done via two on-board Ni-Cad AA cells and/or an external power source. The board also has switchable and externally programmable write protect. The 420C has 18 address bits, allowing up to 256K bytes of memory by using memory management or block switching techniques. The 420C can be populated for 4K by 12 bits for use with the 560Z's PDP-8 equivalent 6100 chip. The 420C is carefully laid out so that plated through holes are not required at the memory chip pins (The board does, of course, have plated through holes). This feature allows easy replacement of soldered-in memory chips without danger of damaging the board. This eliminates the need for sockets on memory boards.

Applications:

The 420C Memory Board is used as the main memory in medium sized OSI systems (4K to 16K). It can be used as pseudo-ROM via the write protect and battery back-up options. The 420C is used as the memory for the 6100 in the 560Z (4K by 12) and as the dedicated graphics memory on 440 systems with the graphics option (2K by 8).

Specifications:

Mechanical: 8" X 10" G-10 double-sided plated through hole board

Electrical: +5V at 600ma to 1,000ma depending on memory type

Supports: 1K, 2K, 3K, or 4K by 8; or 1K, 2K, 3K, 4K by 12 memory.
Uses any zero data hold-type 2102 memory such as 9102. 91L02, 2102AL, 2102LFPC

Options: Battery Back-up, Write Protect, 18-Bit Address

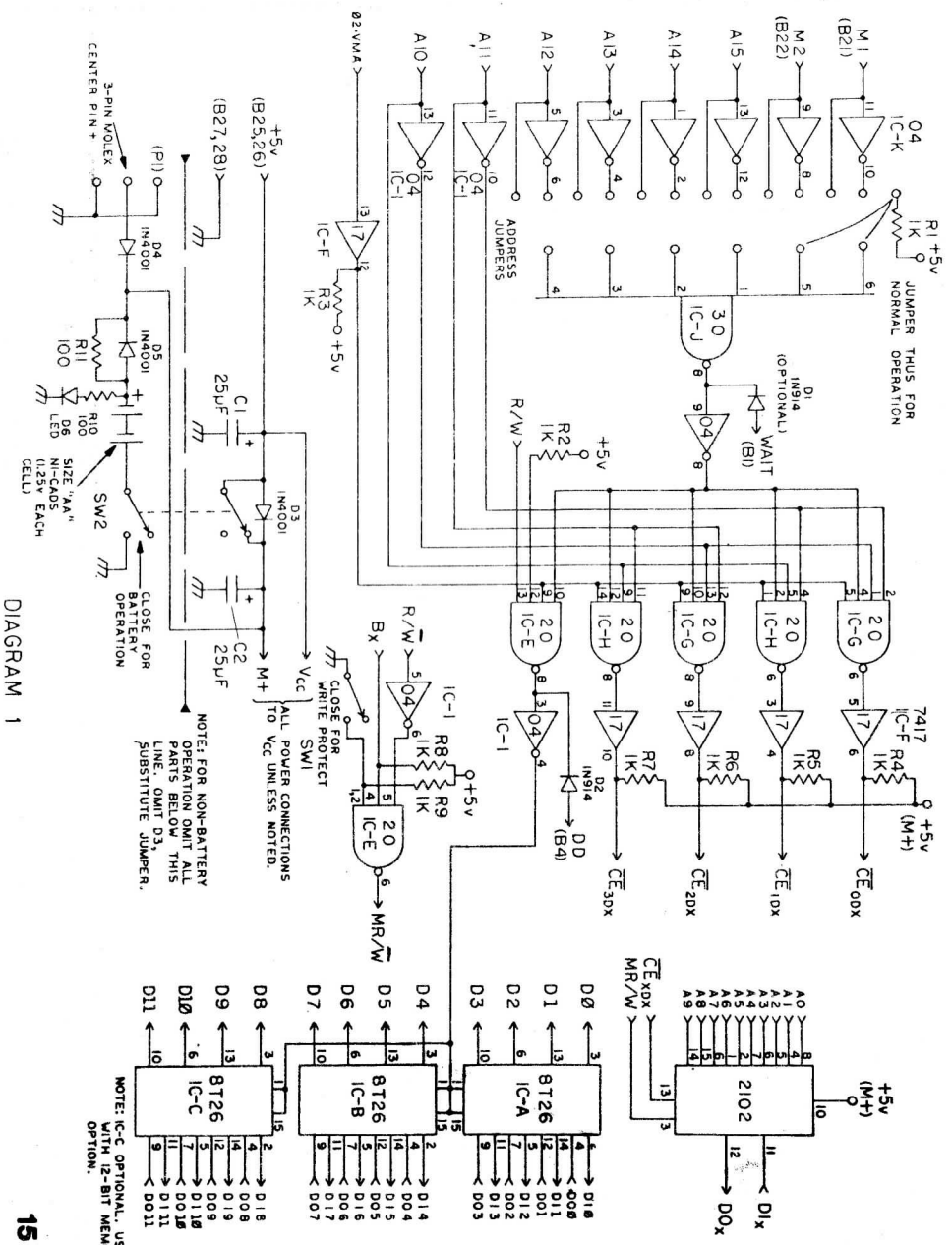


DIAGRAM 1

420C PARTS LIST

1 Model 420C Memory Expansion Board

2 8T26 Buffers (3 for 12 bit operation)

8 to 48 2102 Type Memories

3 7420

2 7404

1 7430

1 7417

1 IN914 (D_2)

19 Bypass Capcitors .1uf Typical

1 25uf Electrolytic

9 1K 1/4 watt R_1- R_9

Battery Backup (Optional)

1 25uf Capacitor

3 IN4001 (D_3, D_4, D_5)

1 Switch (SW_2)

1 100 ohm 1/4 watt (R_{11})

Write Protect (Optional)

1 Switch (SW_1)

Accessories Not Supplied by OSI (Optional)

4 or 5 Molex KK-156 Connectors (Supplied with Backplane Boards)

2 Nicad "AA" Cells

1 LED and 100 ohm Resistor (R_{10})

1 Wait Diode IN914 (D_1)

430B Cassette & Analog I/O

Description:

The OSI 430B is a complete analog I/O subsystem occupying only one board! The 430B can be used simply as a Kansas City Standard Cassette Interface which is fully supported by the OSI 65V PROM Monitor. Or, it can be used fully populated to contain the audio cassette interface or an RS-232 port and 8 parallel I/O lines, 2 fast 8-bit D/A converters, and an ultra-fast tracking A/D converter with an 8 channel input multiplexer.

Applications:

The 430B populated with the audio cassette interface is the fundamental mass storage of a video-based OSI 500 system. The D/A converters can be used for X,Y graphics, plotting, signal generation, music, and voice synthesis. The A/D converter can easily digitize voice and music as well as up to 8 channels of slower 8-bit information. The parallel I/O can be used independently or to supplement the other functions such as tape recorder on/off control, etc.

Specifications:

Mechanical: 8" X 10" G-10 double-sided plated through hole board with 36 I/O pins.

Audio Cassette Interface: Kansas City Standard two-tone system using a UART-based serial converter. Normally used at 300 baud, but can be used to 1,200 baud with selected tape recorders. Has mic. and aux. outputs and an ultra-wide range input.
Note: If the cassette interface is not used, a standard RS-232 port is available and is adjustable for up to 50,000 baud.

D/A Converters (2): 8-bit precision and accuracy 2V output. 300ns settling time. One converter also has an unblank one-shot for X,Y, graphics.

A/D Converter: 8-bit accuracy. -1 to +1 Volt in, one conversion per system clock cycle. Usable with signals up to 20 KHz bandwidth.

8-Channel Multiplexer: National 3705 type. Fully compatible with A/D. Can multiplex 8 inputs at over 1,000Hz!

8-Line Parallel I/O: 8 TTL compatible latched outputs. Three are used by optional 8 channel multiplexer. 8 TTL compatible inputs non latched.

Electrical: +5V at 600ma Maximum
-9V at 150ma Maximum

OHIO SCIENTIFIC			product name/number 430B/CA-6/CA-7	
date 8/77	revision B	page 16	status Production	sheet 1 of 1

OSI Model 430 Super I/O Board Parts List

(All resistors 1/4 watt)

A. Support Circuitry used by all options
- 1 - 7402
- 3 - 7404
- 1 - 7410
- 1 - 7430
- 1 - 74154
- 2 - 8T26
- 1 - 1N914
- Up to 18 bypass capacitors .1 uf or larger
- Up to 3-25 uf electrolytics

B. D/A Converters (per converter) 2 Maximum
- 1 - 1408L8 D/A Converter
- 1 - 741 type op amp (5556 recommended)
- 2 - 7475
- 2 - 1K
- 1 - 10 pf
- 1 - .01 uf or larger

C. 2 volt reference for D/A converters and A/D converter
- 1 - 2.7 volt Zener diode 1/2 watt
- 1 - 4.3 K
- 1 - 1K
- 1 - .1 uf capacitor
- 1 - NPN transistor (2N2270 or similar)

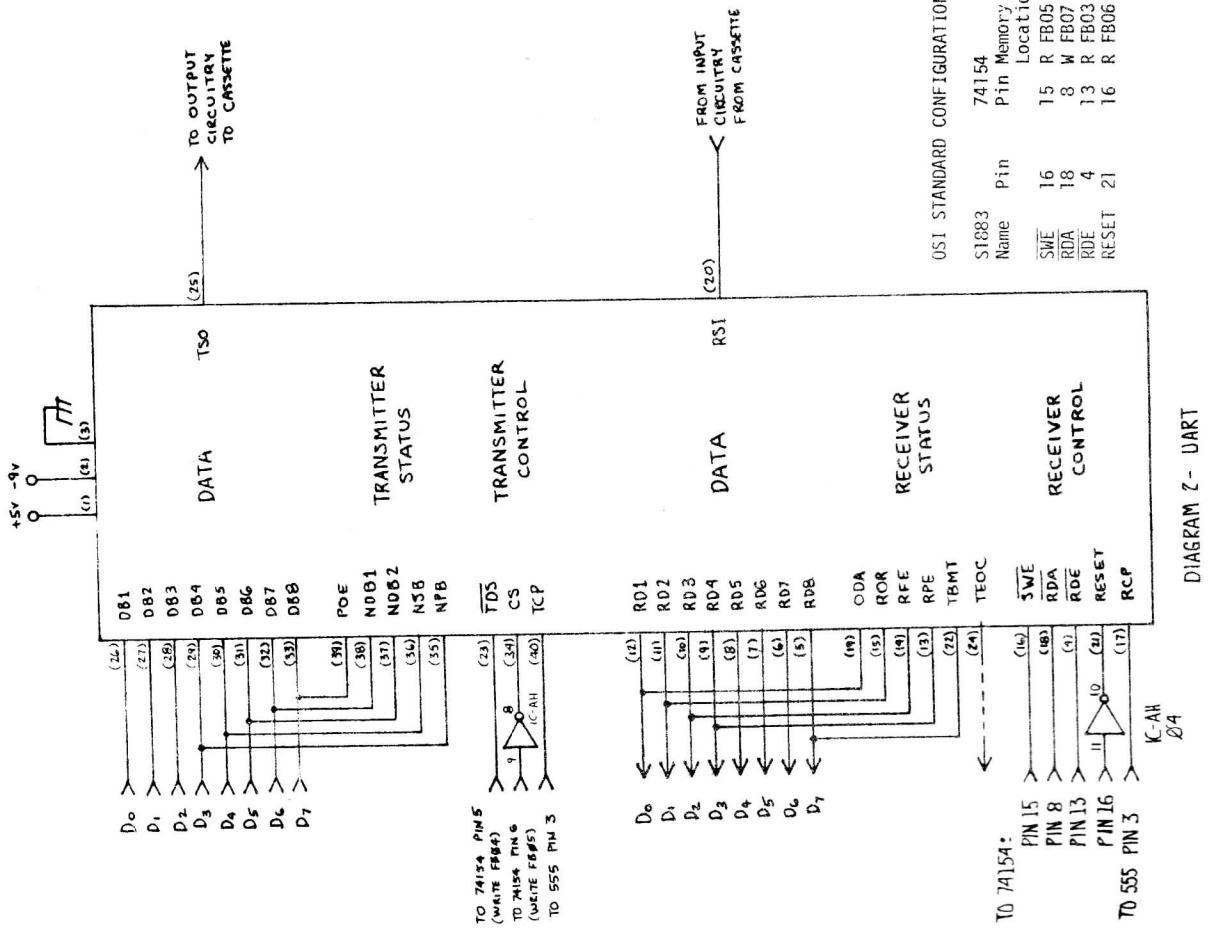
D. Unblank One Shot
- 1 - 74121
- 1 - 560 pf
- 1 - 4.7K
- 1 - 1K (2 μseconds t.c.)

E. A/D Converter
- 1 - 741 type op amp (5556 prefered)
- 1 - 311 Comparitor
- 1 - 1408L8
- 2 - 74193
- 2 - 74125
- 6 - 1K
- 1 - 2.7K
- 2 - 4.7K
- 1 - 100K to 1 Meg.
- 1 - 10 pf
- 1 - .01 uf
- 1 - 2k to 10K pot.

F. Auxilary Parallel I/O
- 2 - 7475
- 2 - 74125

G. Audio Tape Interface 300 Baud
- 1 - S1883 UART or equivalent
- 1 - 555 Timer
- 2 - .01 uf
- 1 - .01 uf (high quality)
- 2 - 10K
- 2 - 10K pot.
- 5 - 1K
- 1 - 7404
- 1 - 7476
- 1 - 100K

- 1 - .005 uf
- 1 - .001 uf
- 1 - .1 uf
- 1 - 50 pf
- 1 - 4.3K
- 2 - 1N914
- 1 - 100 ohms
- 1 - CA3130 op amp
- 1 - 74123
- 1 - 7474



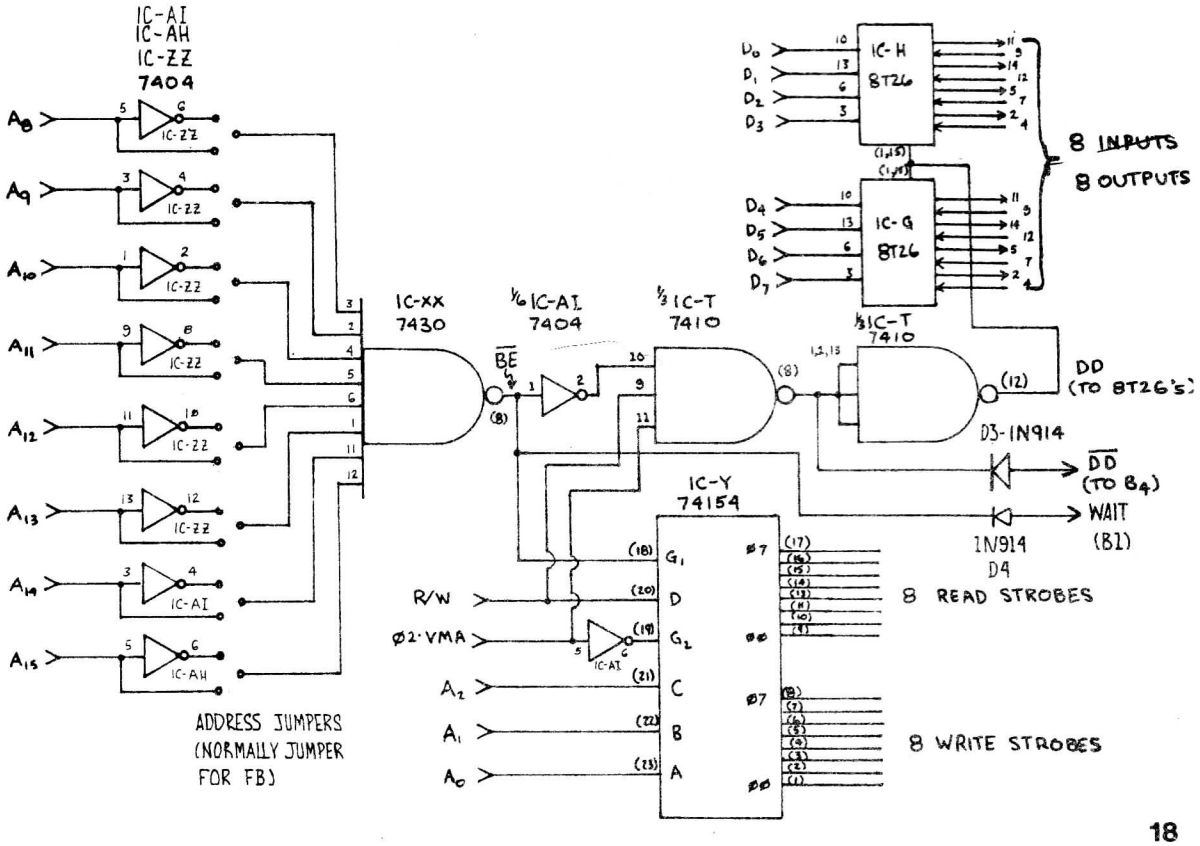


DIAGRAM 1- ADDRESS DECODER AND DATA BUFFER

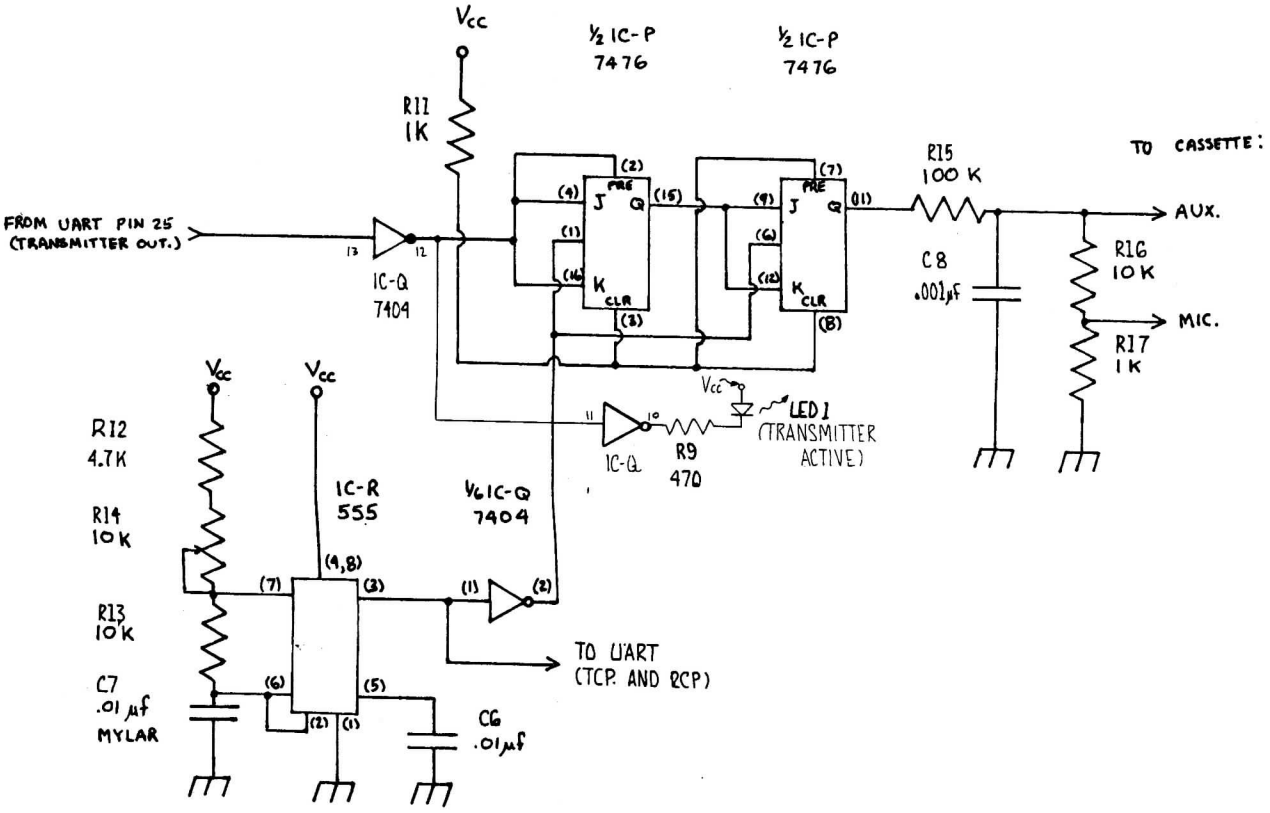
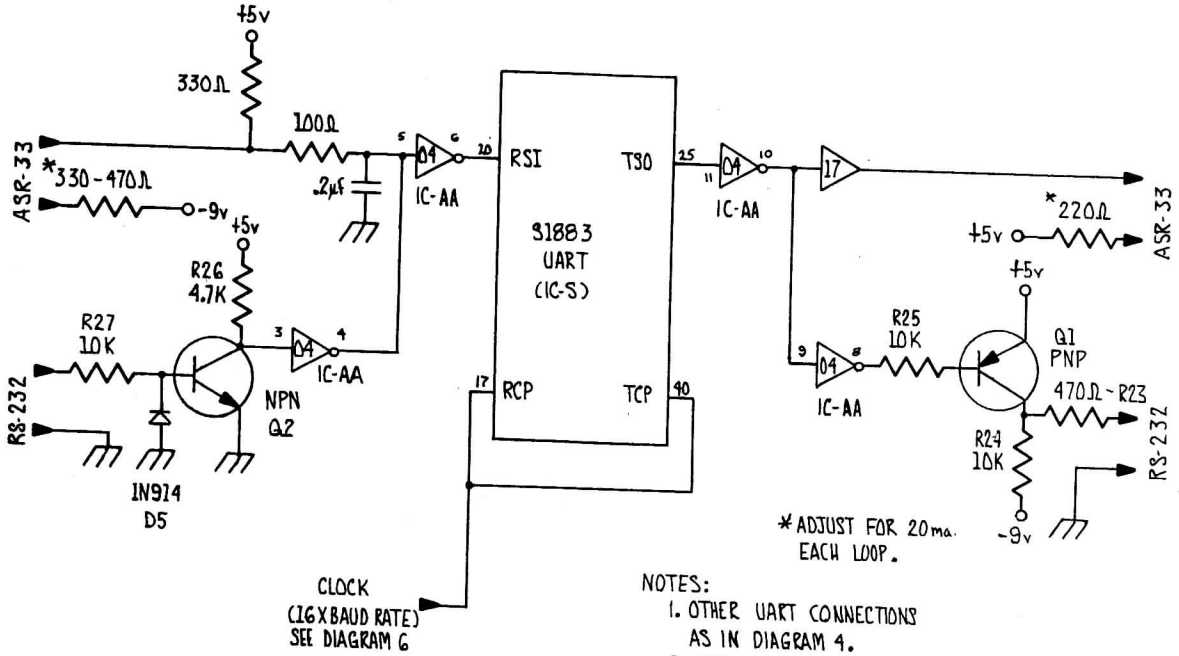


DIAGRAM 4- AUDIO CASSETTE TRANSMITTER



NOTES:
1. OTHER UART CONNECTIONS AS IN DIAGRAM 4.
2. USE EITHER ASR-33 OR RS-232.
3. ASR-33 SHOWN FOR REFERENCE ONLY. IT IS NOT IMPLEMENTED ON 430 BOARD.

DIAGRAM 3 – ASR-33 AND RS-232 INTERFACE

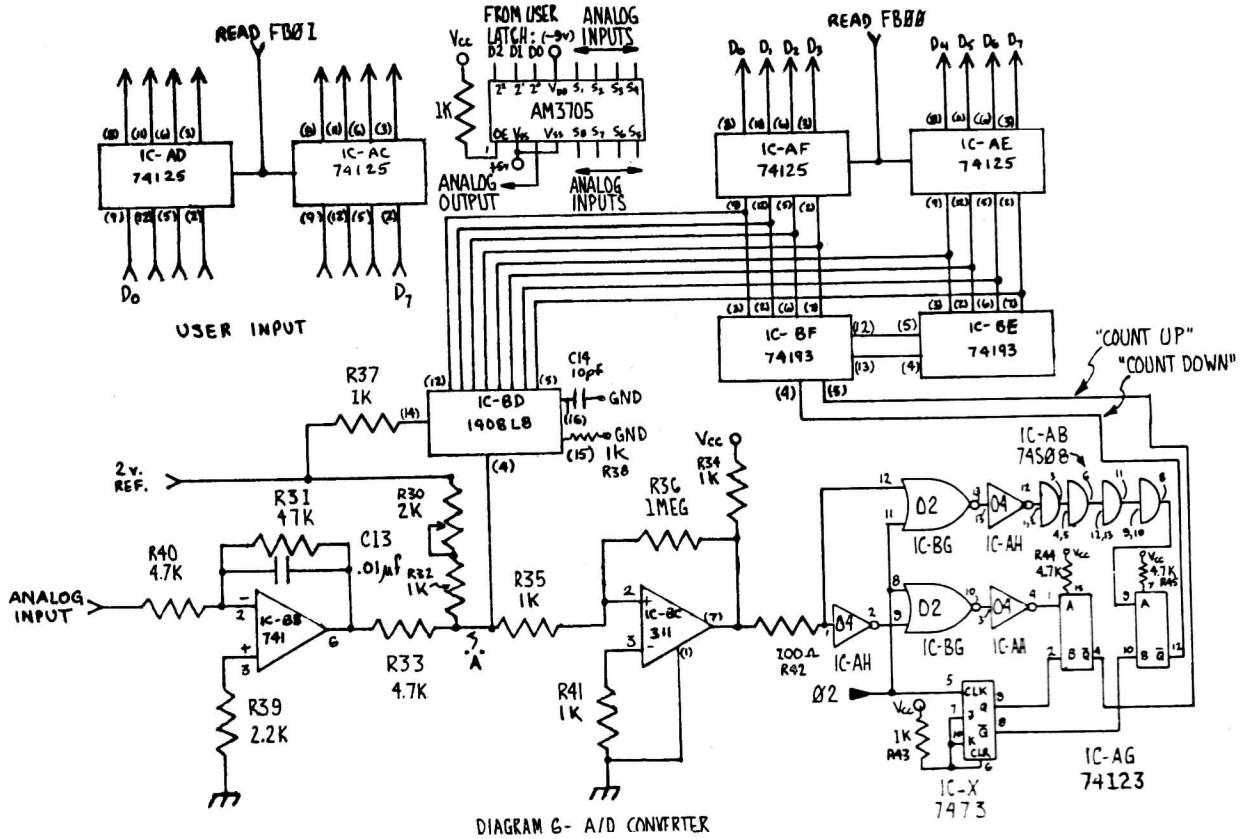


DIAGRAM 6- A/D CONVERTER

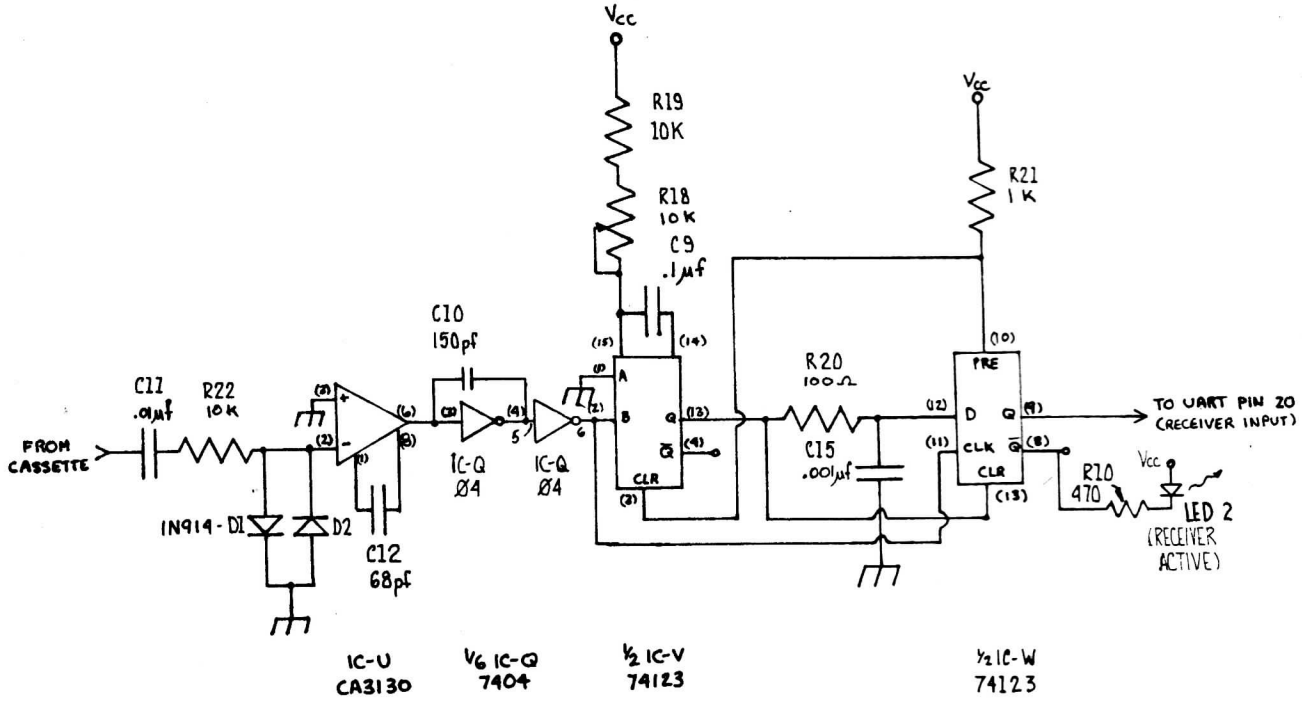
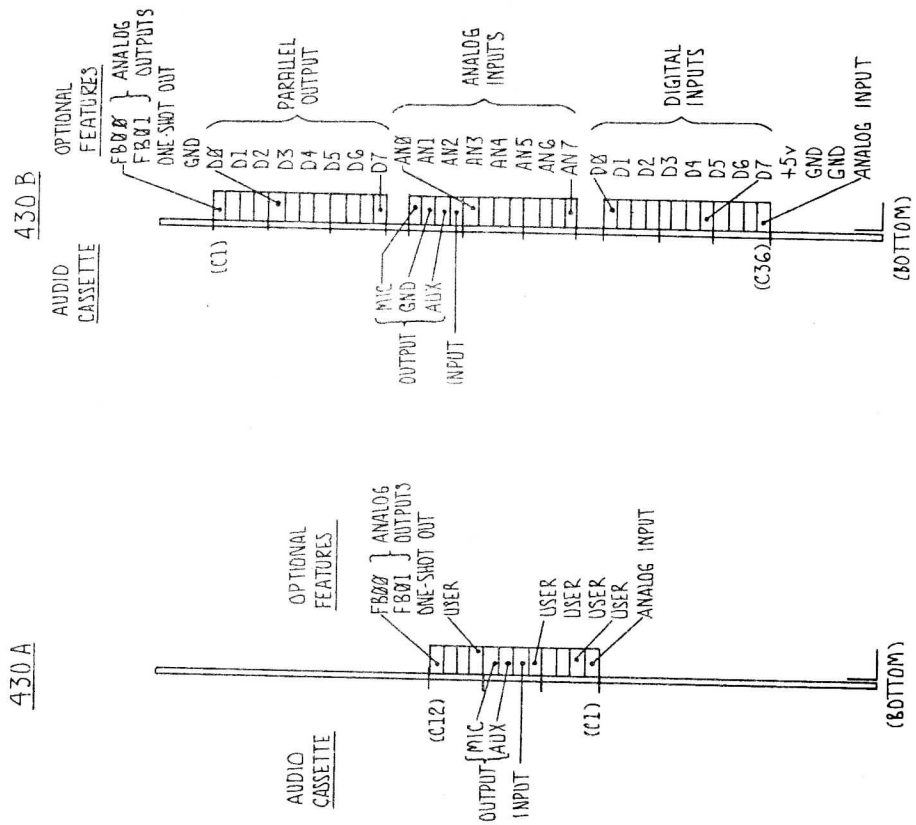


DIAGRAM 5- AUDIO CASSETTE RECEIVER

430 BOARD CONNECTIONS FOR AUDIO CASSETTE AND OPTIONAL A/D AND D/A CONVERTERS



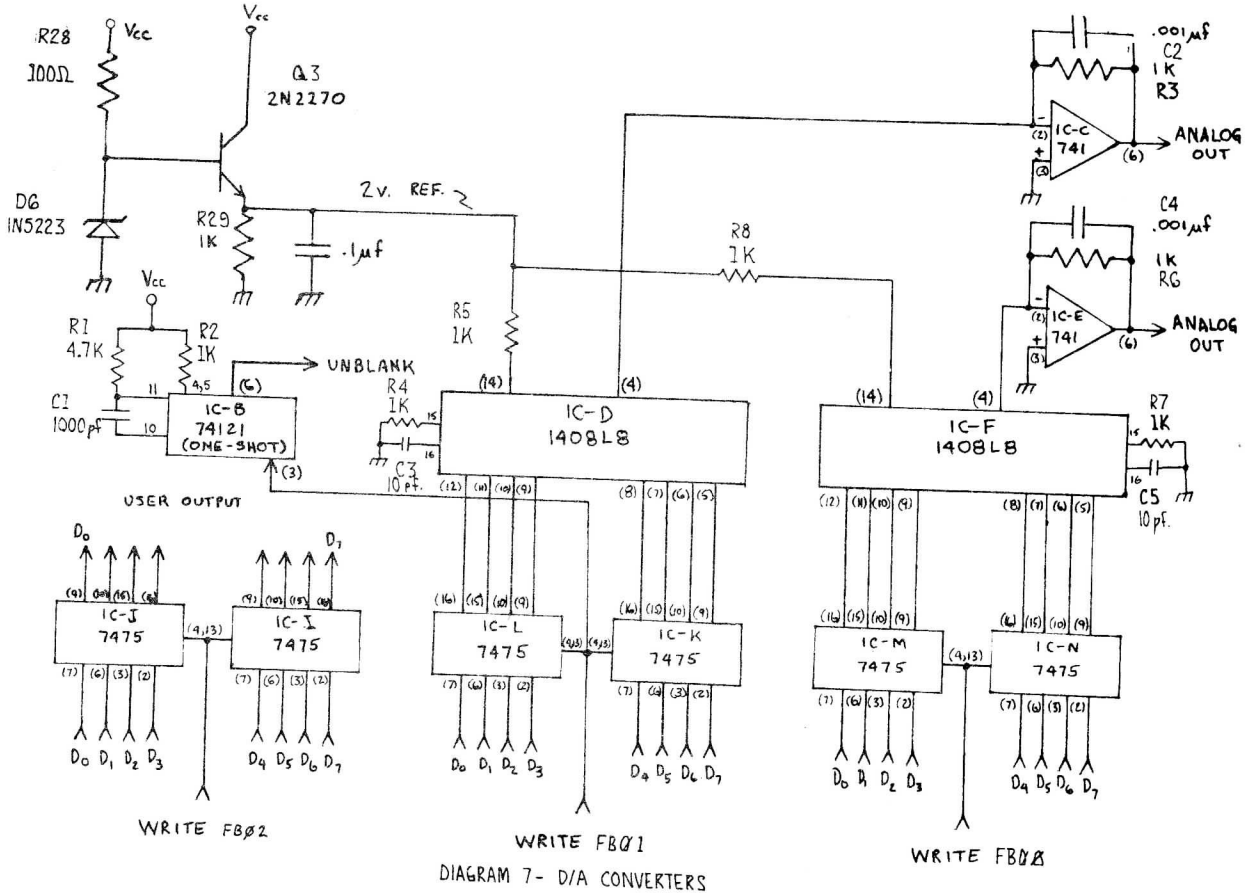


DIAGRAM 7- D/A CONVERTERS

440B Video Board

Description:

The OSI 440B Video Graphics Board is a versatile high performance computer to video (TV) interface. The 440 Board can be very economically populated as a terminal for a 500 or Challenger computer providing up to 32 by 32 characters on a screen and a keyboard input port. It can maximally be populated for 32 by 32 alphabetics, 128 by 128 graphics, and four color alphabetics. The 440 uses a dedicated memory which is accessed as conventional RAM memory by the computer. The result is that the 440 has ultra-high speed random access capability, allowing elaborate real-time animation!

Applications:

An alphabetics equipped 440 Board together with a 500 board is a complete computer and terminal. The ultra-high speed loading and random access features of the screen provide full animation capability in both alphabetics and graphics mode for elaborate video games and animation. Color can optionally enhance these features. In conjunction with a 430 Board's A/D converter, the graphics feature allows an OSI computer to act as an intelligent storage oscilloscope up to audio frequencies. The system operates particularly well with biological signals which are traditionally difficult to display. The graphics display can be used with a parallel input port as a logic analyzer since eight traces can easily be displayed on a conventional TV set!

Specifications:

Mechanical: 8" X 10" G-10 double-sided plated through hole board; 16-pin (IC type) keyboard connector. Optional 420 "slave" memory for graphics connects via three 16-pin ribbon cables.

Electrical: +5V at 800ma
-9V at 30ma

Output: 0 to 2V video into hi-Z termination. Composite video or separated sync (TTL level).
Vertical Frame Rate: 60.0Hz
Horizontal Frequency: 15,450Hz
Character Font: 5 X 7 characters upper-case ASCII
Format: 32 rows of 32 characters maximum. Unmodified TV sets typically display 24 rows of 24 columns of characters. 128 rows of 128 dots (graphics option) maximum

Keyboard Input: seven-bit parallel ASCII with continuous strobe or at least 50 usec. long-pulsed strobe. Strobe can be negative or positive going.

OSI MODEL 440 PARTS LIST

For Alphabetics Use Only

___ 1 - 440 Video Graphics Board
___ 2 - 7403
___ 2 - 7404
___ 3 - 7408
___ 5 - 7420
___ 2 - 74123 Texas Instruments or ITT units only.
___ 2 - 74125
___ 3 - 74157
___ 4 - 74163
___ 1 - 74165
___ 2 - 8T26
___ 1 - 2513N CM 2140 font recommended. Use ONLY Signetics Units.
___ 6 - 2102 type memories. "zero data hold time" 650ns. worst case for 1MHz operation, 350 ns. worst case for 2MHz operation.
___ 1 - 1N914

NOTE: Use only standard TTL since propagation delays are important

Resistors All ¼Watt 10% or Better

___ 4 - 220 ohm
___ 1 - 470 ohm
___ 7 - 1K
___ 1 - 2.2K
___ 2 - 4.7K
___ 1 - 10K
___ 2 - 5K pots
___ 1 - 10K pots

Capacitors 10V. Rating or Better 20% Tolerance

___ 1 - 6.8pf NPO (temperature stable)
___ 1 - 68pf NPO (temperature stable)
___ 1 - .001uf
___ 1 - .1uf stable (mylar or polycarbonate)
___ 1 - 25uf (optional)
___ 18- .1uf bypass capacitors

Graphics Parts Included in 446 Kit

___ 3 - 74157
___ 1 - 74165

Required Parts Not Supplied in 446 Kit

___ Sockets: at least one at keyboard connector
___ 4 - Female Molex Connectors
___ Jumper Wire
___ Solder

Required Parts for Graphics Not Supplied by OSI

___ 1 - 420B or 420C Memory Board
___ 16- 2102 Memories; specifications as above
___ 3 - Sockets (minimum)
___ 3 - 4" or longer 16 pin jumper cables
___ 1 - Female Molex Connector
___ Approximately 8 - Bypass Capacitors (.1uf)

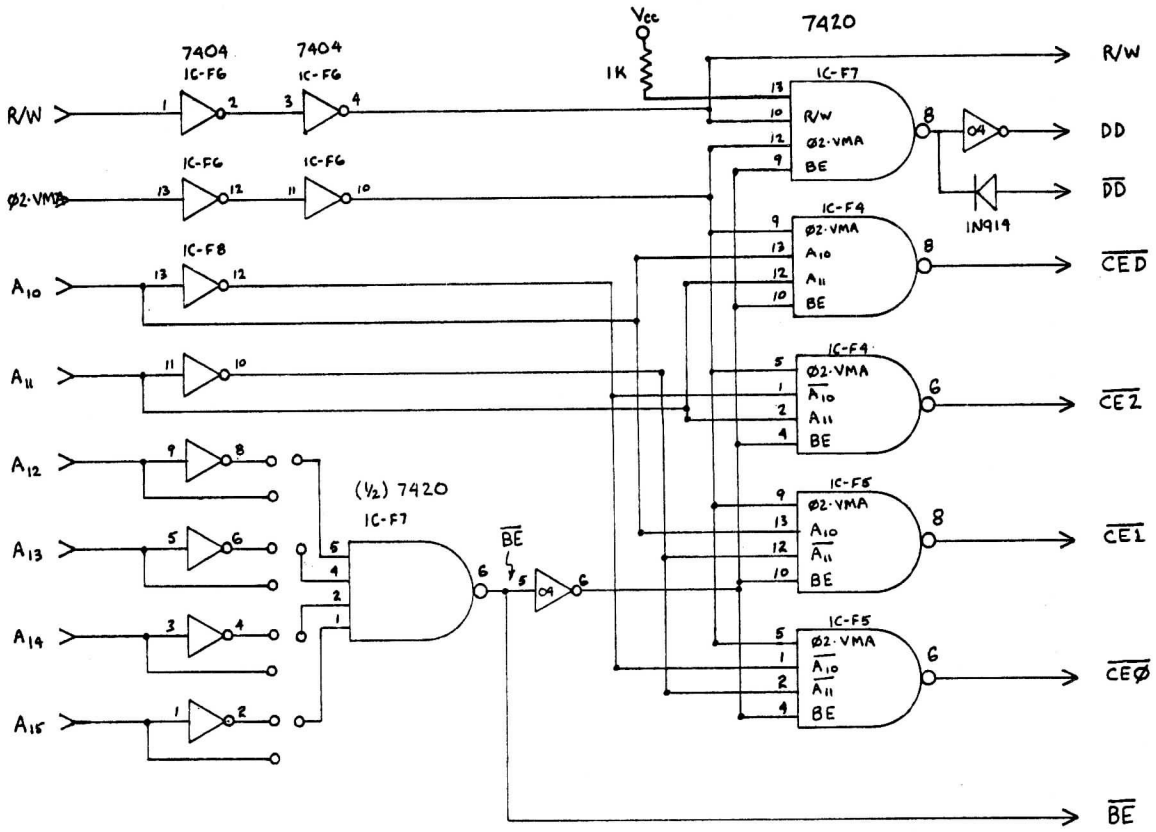


Diagram B. 440 Board Address Decoding

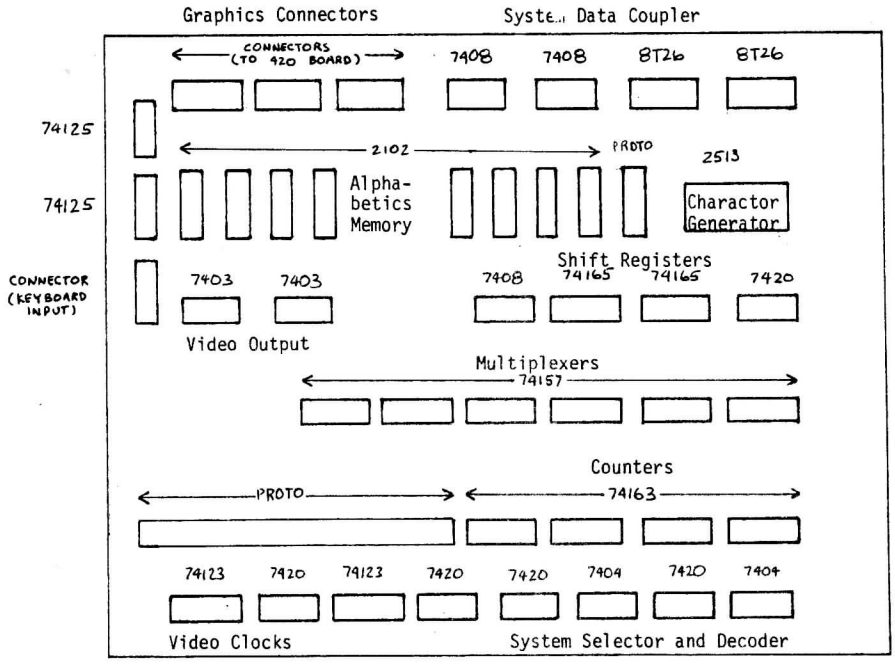


Diagram A. 440 Board Layout

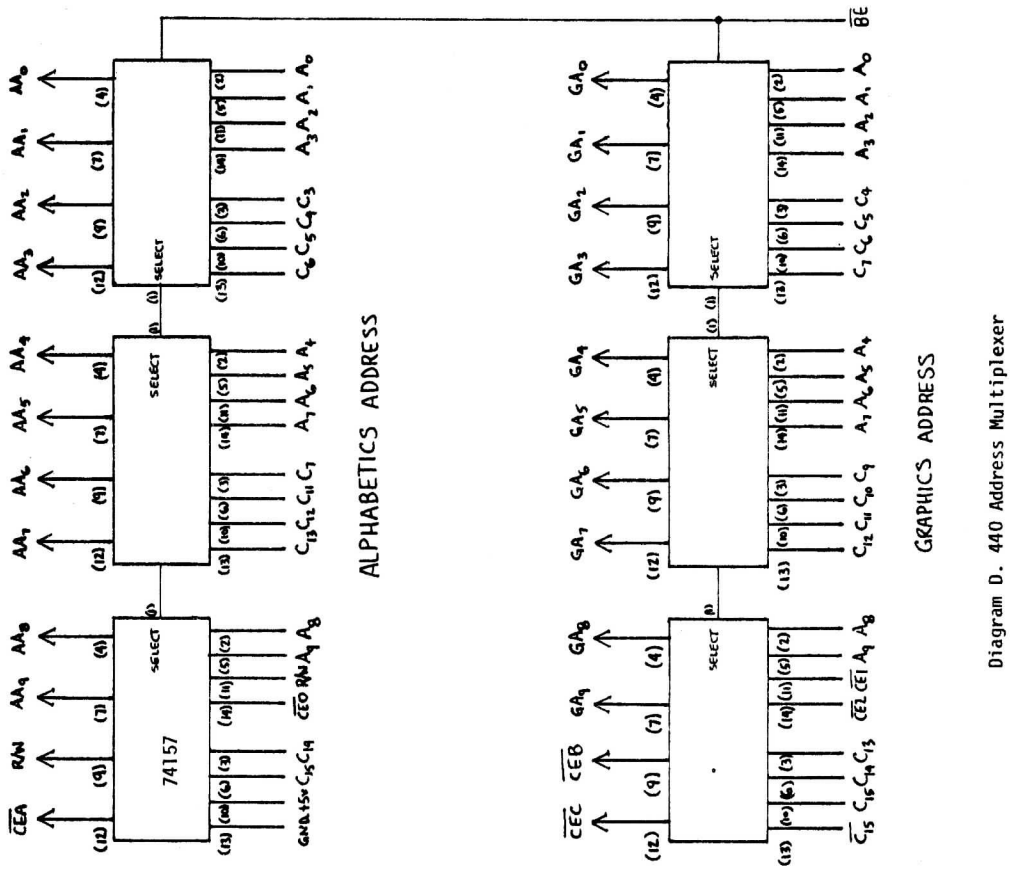


Diagram D. 440 Address Multiplexer

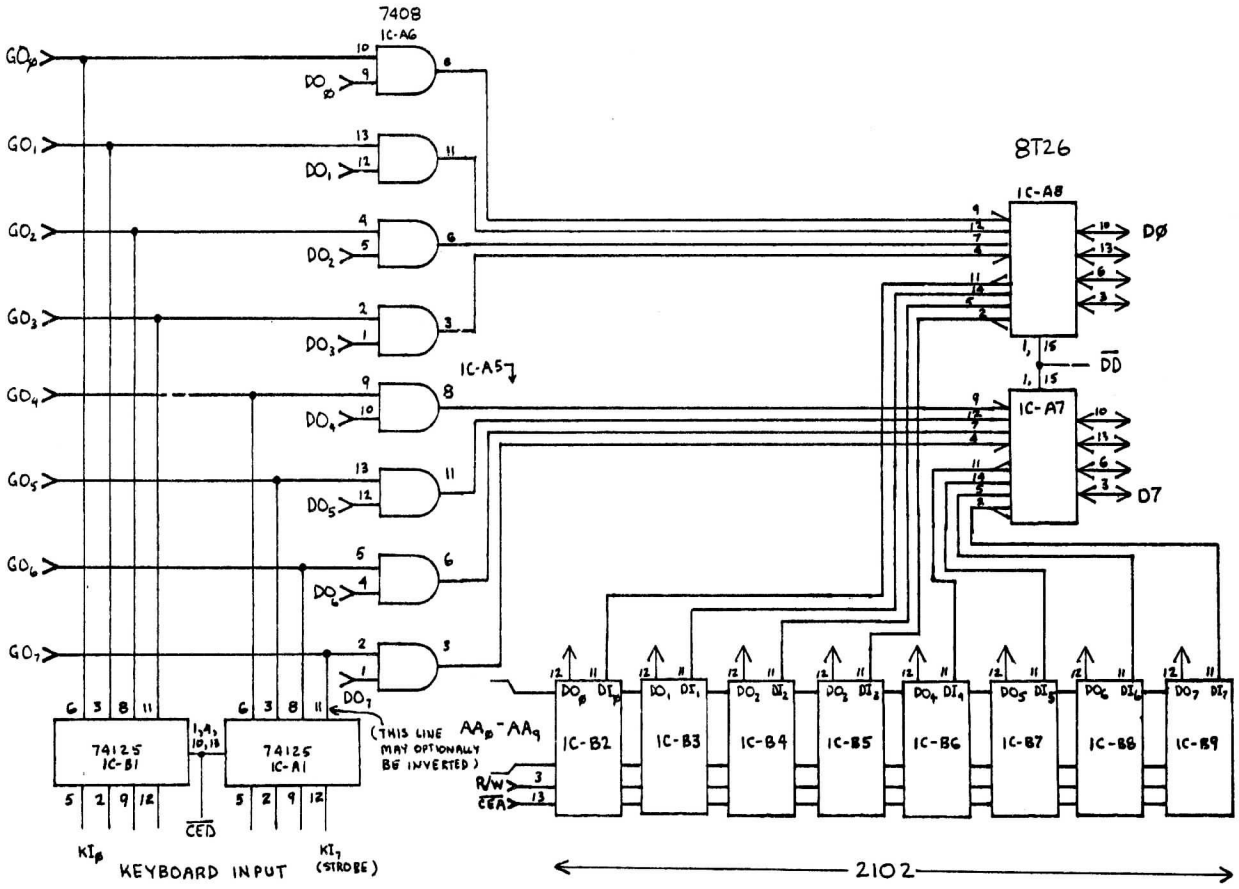
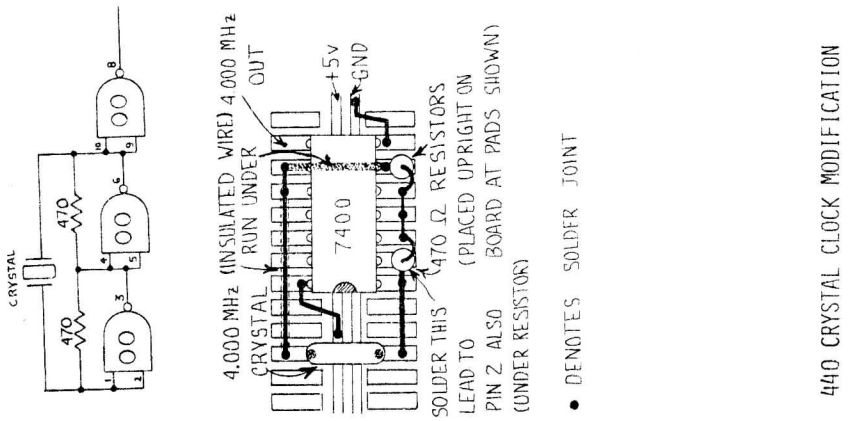


Diagram E. 440 Alphabetics memory, data multiplexer, and data buffers



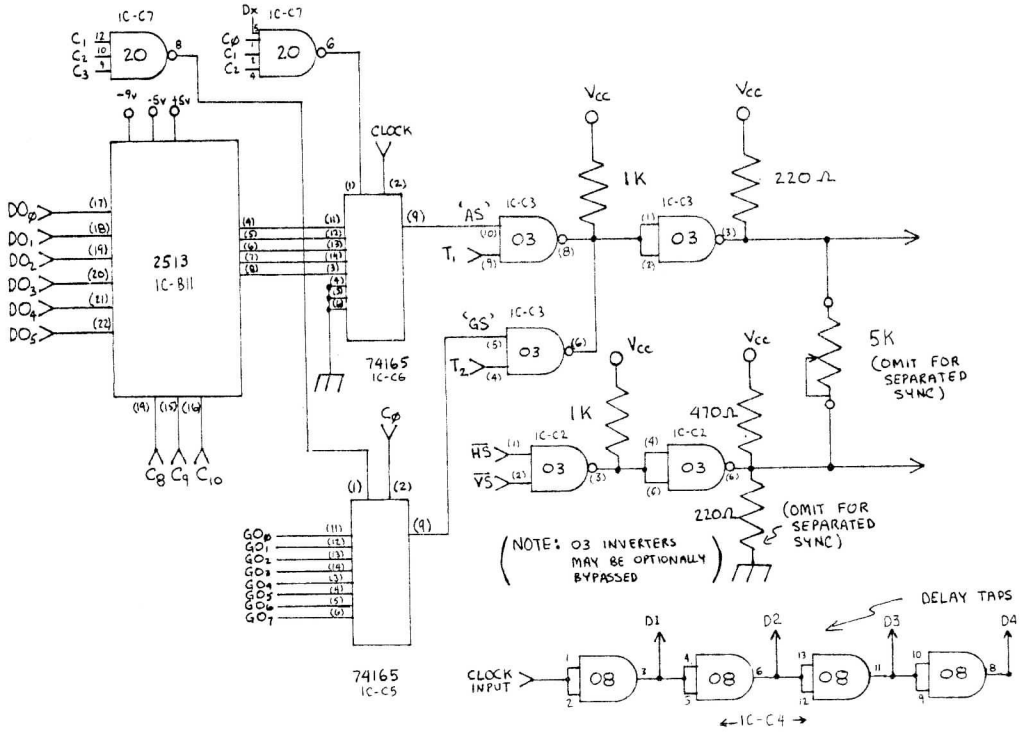
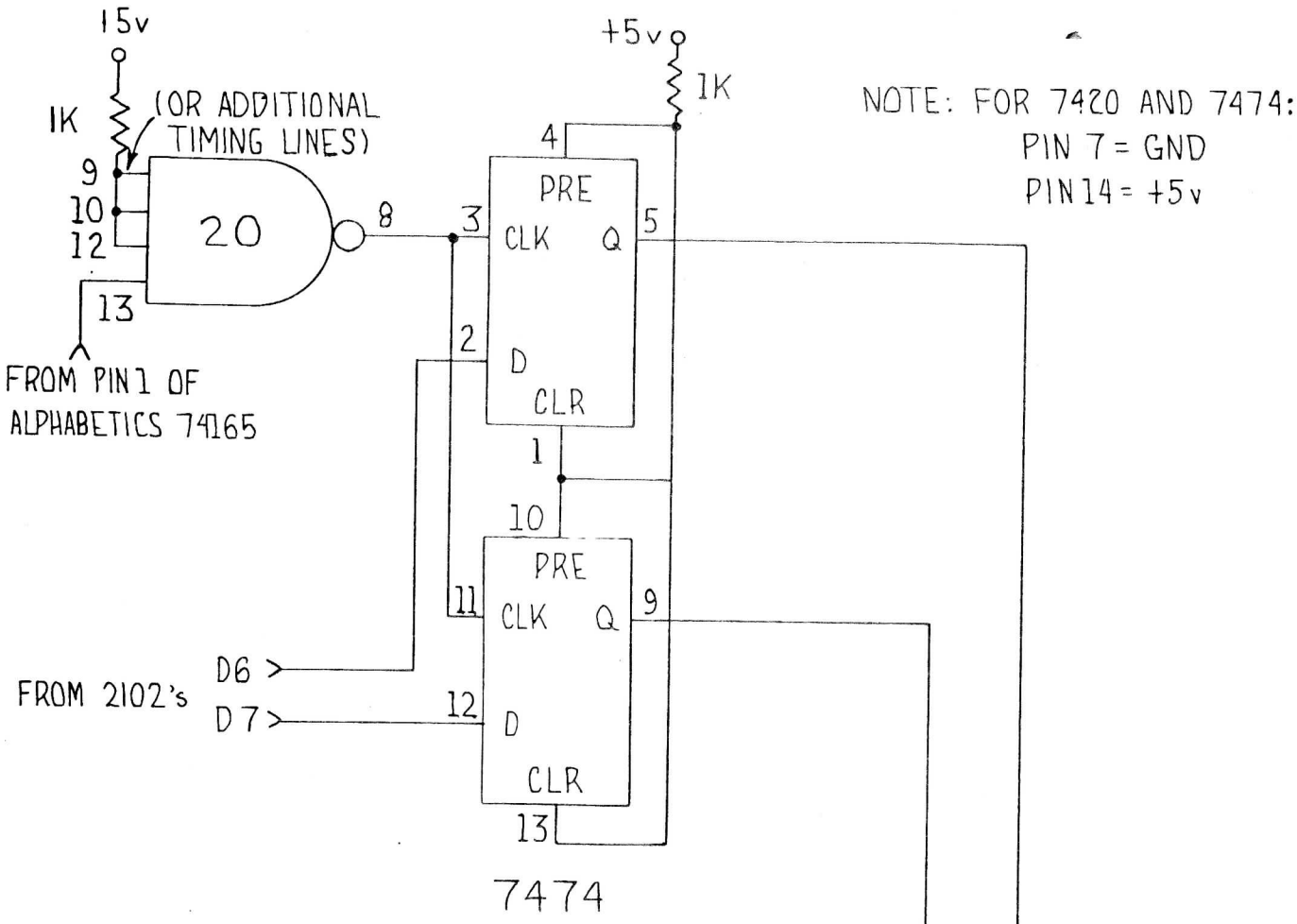
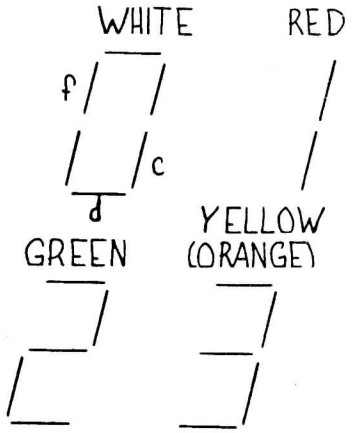
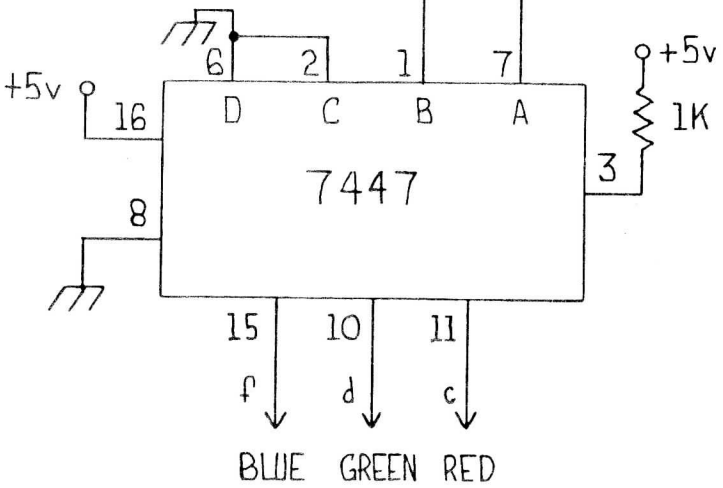


Diagram F. 440 Character generator shift register and video output





f = BLUE GUN
c = RED GUN
d = GREEN GUN



15 VOLT OPEN COLLECTOR OUTPUT
(ON = GROUND = GUN ON)

COLOR IMPLEMENTATION

450B 8K EPROM and Parallel I/O
455 4K EPROM and Parallel I/O

Description:

OSI 450 and 455 EPROM boards provide ROM storage and 16 lines of parallel I/O. The 455 Board accepts up to 4K by 8 of the popular 1702 or 3702 type 256 X 8 EPROM. The 450 Board accepts up to 8K by 8 of the 6834 (512 X 8) EPROMs and features an on-board programmer for 6834s.

Applications:

Both PROM boards are ideal for dedicated applications of the 400 system since they provide permanent storage and parallel I/O. The 455 Board can be used where a small program is needed and a 1702 programmer is available. The 450 Board can be used with much larger programs which can be loaded into PROM right on the board! The 6834 EPROM is one of the easiest to program and is the most cost effective EPROM available.

Specifications:

Mechanical: 8" X 10" G-10 double-sided plated through hole board
24 I/O connections

Electrical (Either Board): Maximum configuration--
+5V at 2Amps
-9V at 600ma

Parallel I/O: 6820 based parallel I/O with 16 I/O lines and four hand-shake lines.

455 Board: Up to 16 1702 type PROMs (4K by maximum). Occupies 4K of contiguous memory.

450 Board: Up to 16 6834 type PROMs (8K by 8 maximum). Occupies 8K of contiguous memory.

450 Board Programmer: Dedicated Programmer socket; requires -50V at 50ma maximum. Programming is accomplished with included programmer program written for 6502 based systems.

Parts List

PROM only

1	Model 450 Board
2	8T26
1	7400
2	7404
1	7420
1	7430
3	7475
1	74154
2	1K 1/4 watt (R10, R11)
2	IN914 (D3, D4)
28	.1uf bypass caps
1	25uf 24V electrolytic (C3)
1 to 16	S6834 PROMs

Programmer

1	74123
1	MC6820 PIA
1	100ohm (R3)
1	220 ohm (R5)
1	1K (R7)
4	4.7K (R1, R2, R8, R9)
1	18K (R6)
1	22K (R4)
1	1.0 uf mylar (C1)
1	25uf 25V electrolytic (C2)
2	IN4001 diode (D1, D2)
2	PNP transistors 2N398B or equiv. (Q1, Q2)
1	DPDT slide switch
1	24-pin socket (ZIF preffered)
1	4 pin Molex (KK-156) Power connections

Optional

PROM Sockets as Desired

4	Molex KK-156 Connectors (B1-B48)
2	Molex KK-156 Connectors (F1-F24) (PIA PORT only)

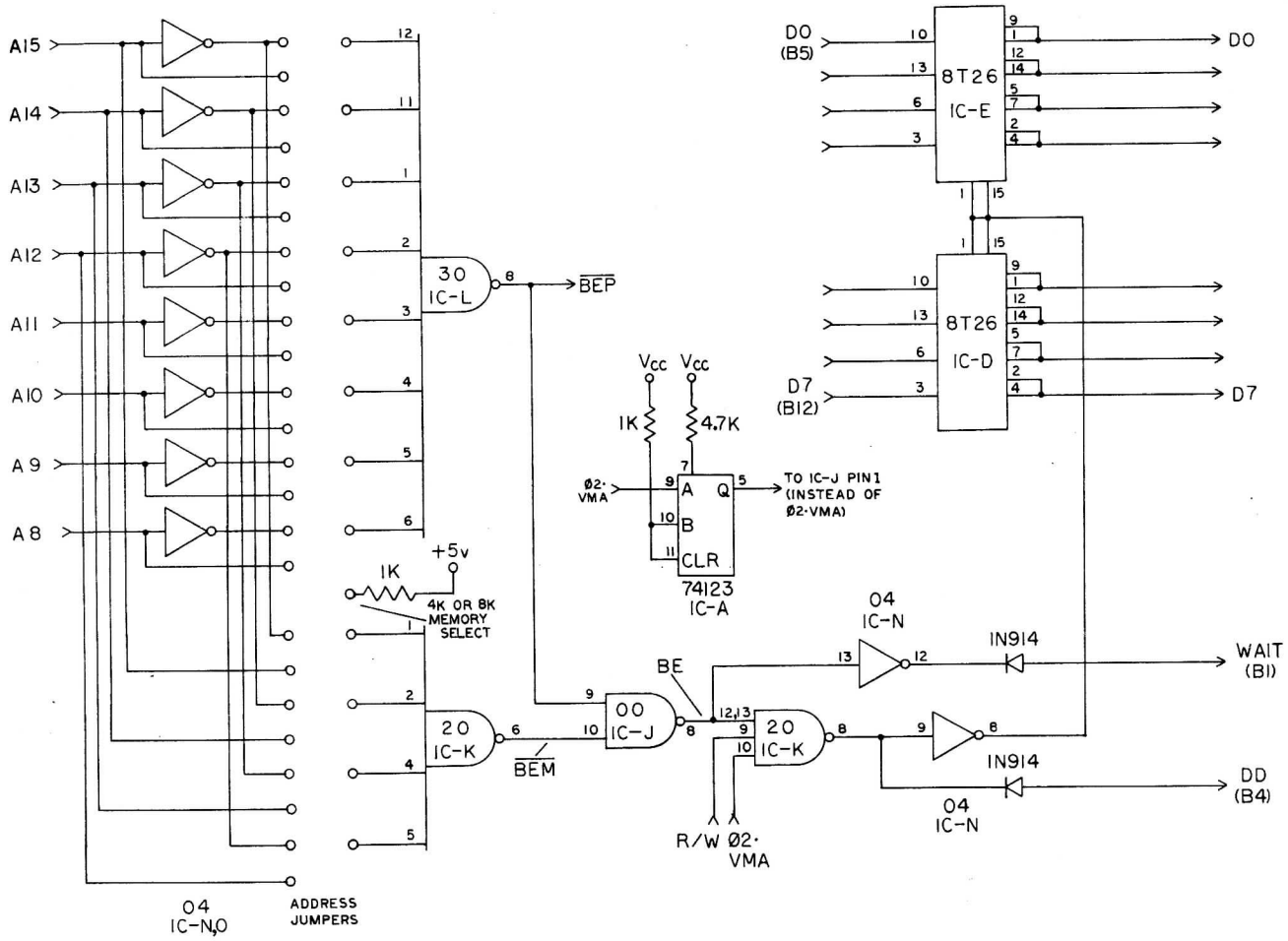


DIAGRAM 1- ADDRESS DECODING

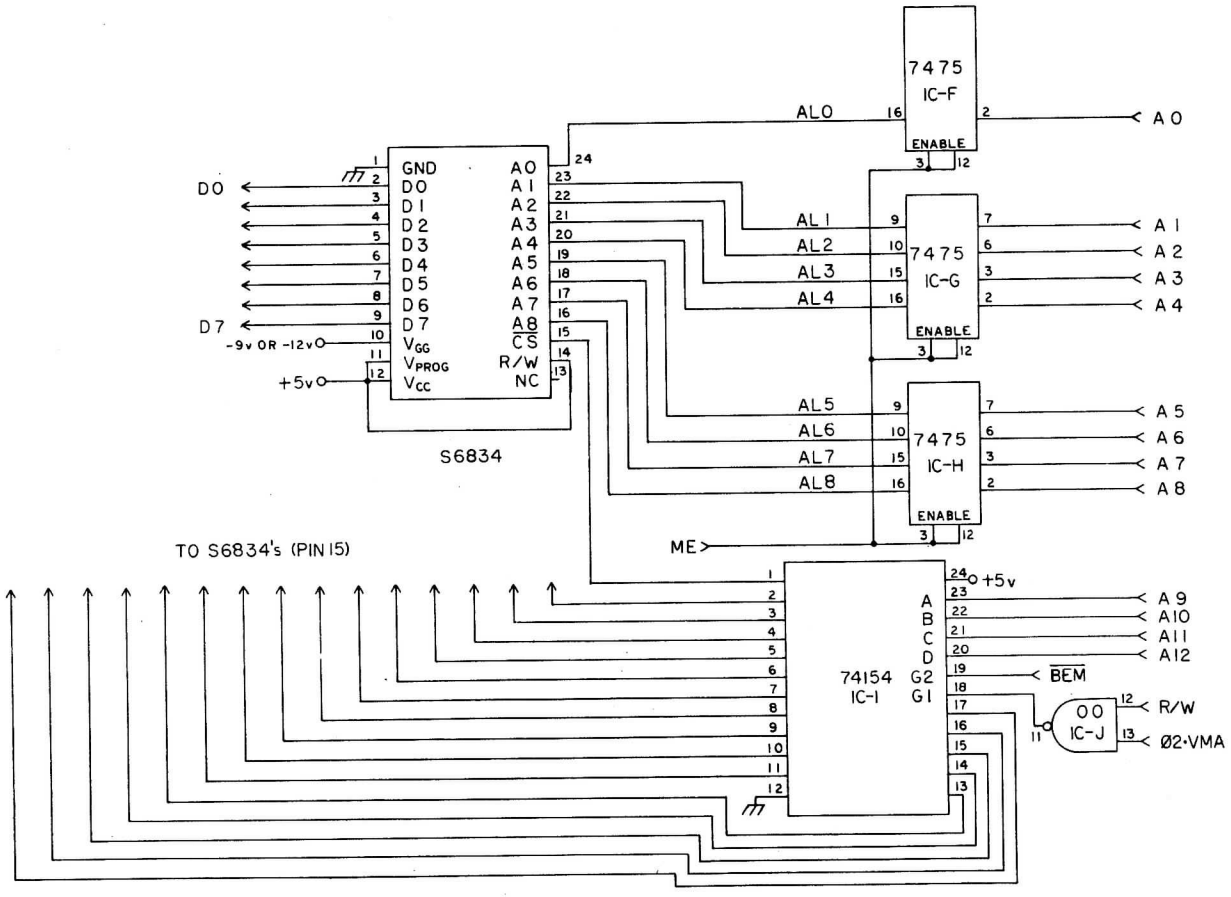
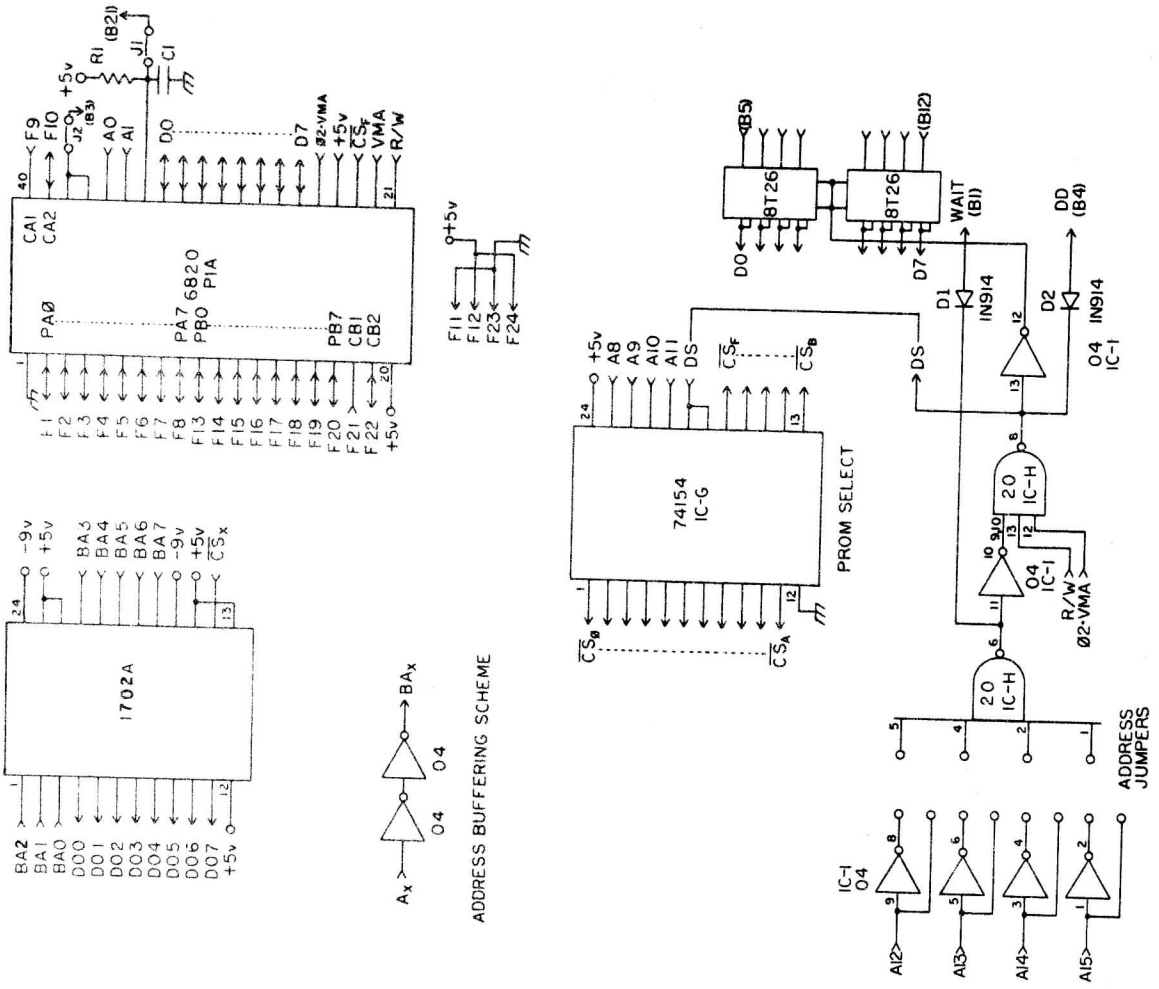
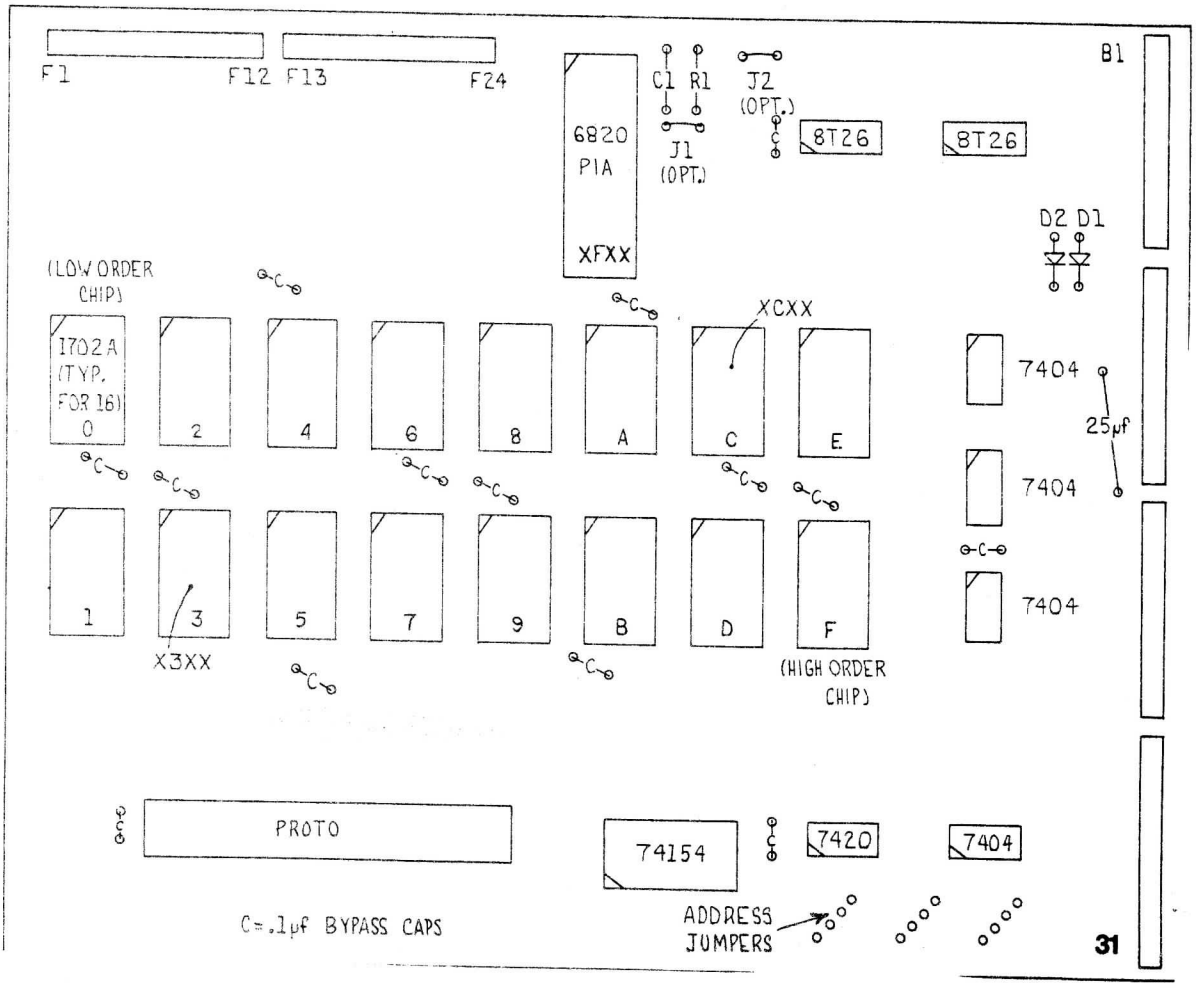


DIAGRAM 2- PROM IMPLEMENTATION


6820 PIA
74154 IC-G
PROM SELECT
1702A
ADDRESS BUFFERING SCHEME
8T26
IN914
IC-H
IC-I
ADDRESS JUMPERS


6820 PIA
XFXX
1702A (TYP. FOR 16)
(LOW ORDER CHIP)
(HIGH ORDER CHIP)
X3XX
XCXX
8T26
7404
25µf
PROTO
74154
7420
ADDRESS JUMPERS
C=.1µf BYPASS CAPS

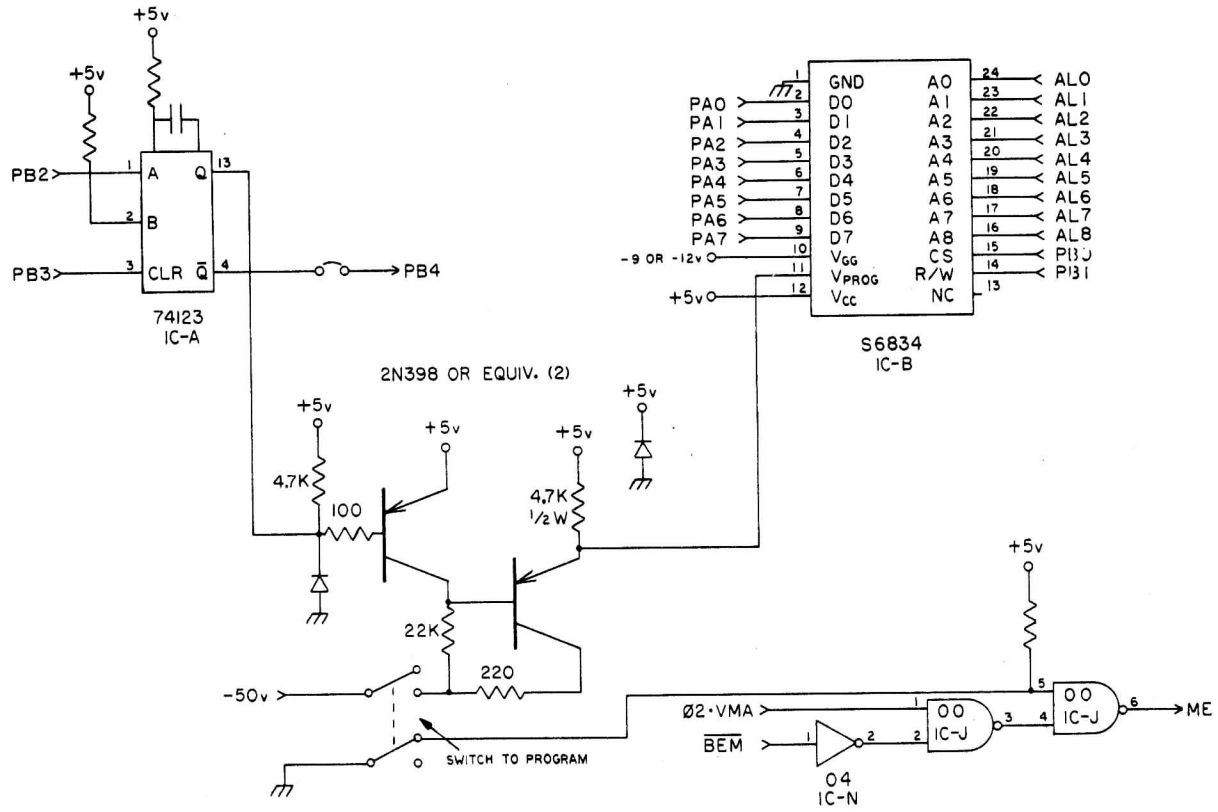


DIAGRAM 4- PROM PROGRAMMER

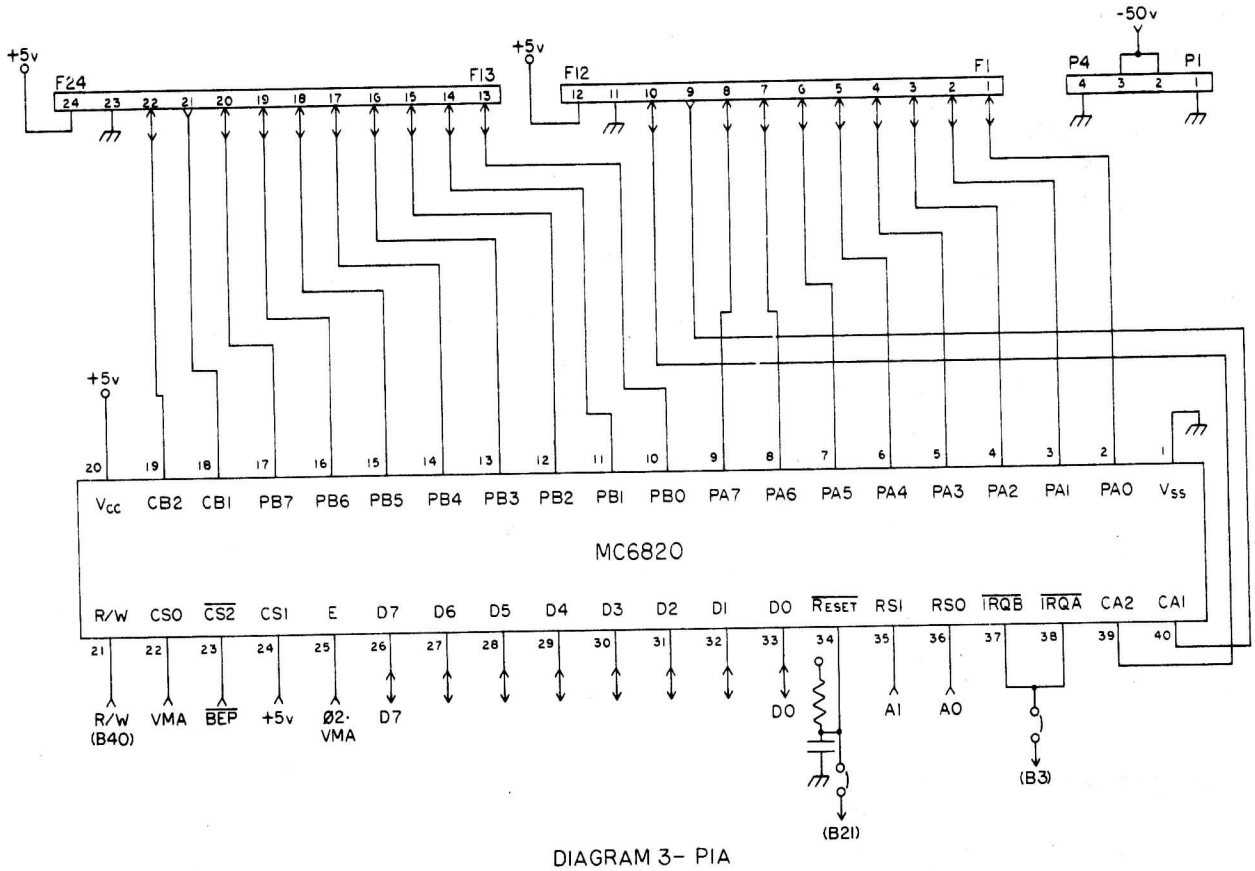
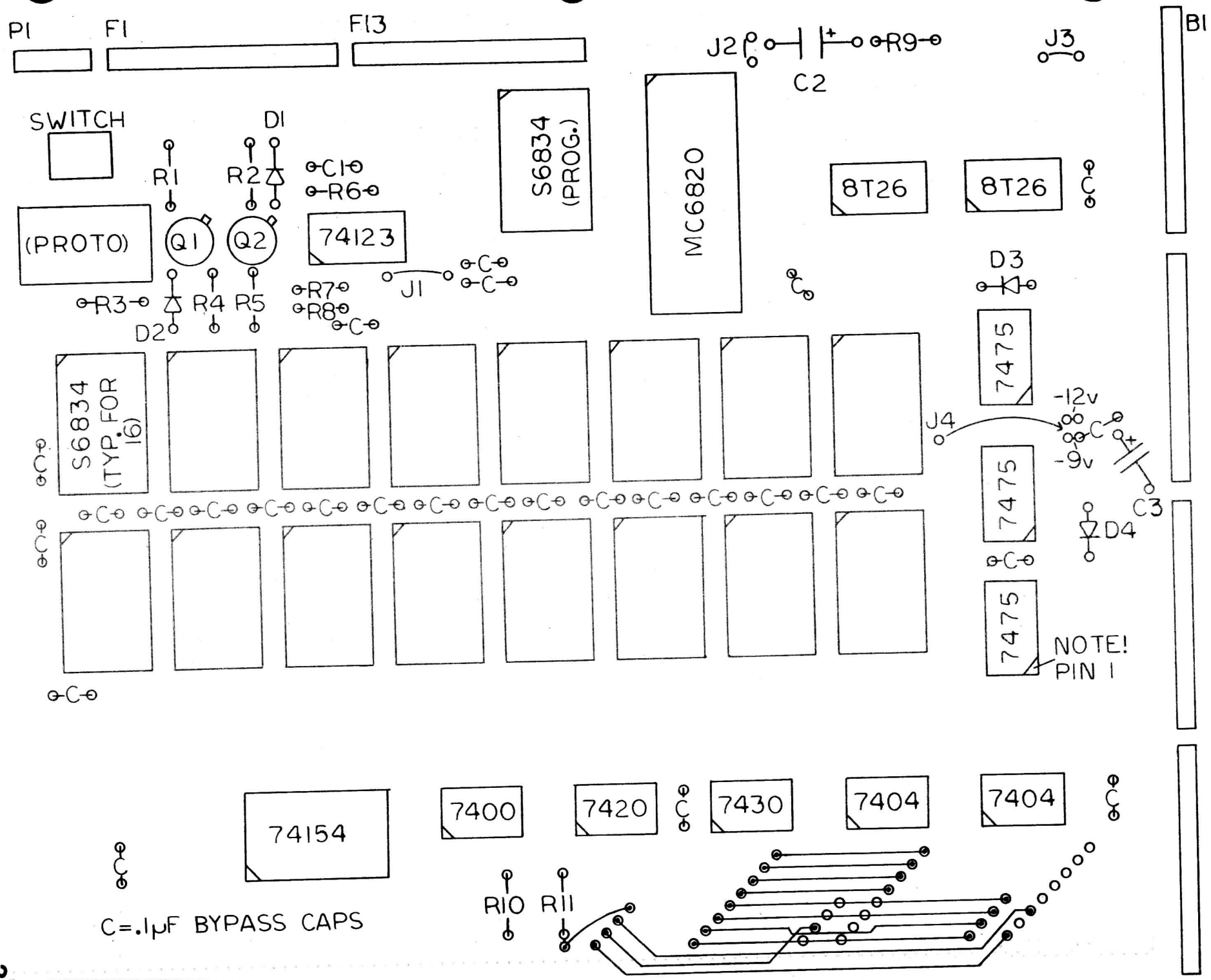


DIAGRAM 3- PIA


P1
F1
F13
J2
C2
R9
J3
B1
SWITCH
D1
R1
R2
C1
R6
S6834
(PROG.)
MC6820
8T26
8T26
(PROTO)
Q1
Q2
74123
D3
R3
R4
R5
R7
R8
J1
D2
7475
S6834
(TYP. FOR
16)
-12v
J4
-9v
C3
D4
7475
7475
NOTE!
PIN 1
74154
7400
7420
7430
7404
7404
R10
R11
C=.1μF BYPASS CAPS

475 Floppy Disk System

Description:

The 475 Floppy Disk Subsystem provides extremely fast random access mass storage for any Ohio Scientific Computer. The 475 Kit includes a General Systems International Model 110 Disk Drive (a full-sized floppy, not a mini!) a preassembled four-foot interconnecting harness, the 470 controller board (kit), and the OS-65D Disk Operating System on floppy diskette. Documentation includes the Model 110 Disk Drive Manuals and the OS-65D Operating System Documentation as well as 8K BASIC for Disk. Documentation does not include the Assembler or Extended Monitor documentation.

Applications:

The 475 or assembled Challenger disk drive is the recommended mass storage device for any Ohio Scientific computer. Programs are transferred on and off of the disk as fast as you can type the commands. For example, the load times for 8K BASIC on three types of media are given below:

8K BASIC Loading Times

Floppy Disk	1.3 Seconds
Audio Cassette	15 Minutes
Paper Tape	45 Minutes

Specifications:

Mechanical: The 470 PC Board is an 8" X 10" G-10 Double-Sided Plated Through Hole Board. The Cable is a 50-Pin Four-Foot-Long Cable Properly Terminated for GSI 110 Drive and 470 Interface Boards.

Electrical: 470 Board: +5V at 300ma and -9V at 100ma
GSI Model 110: +5V at 1.5 Amps and +24V at 1.7 Amps

System Requirements: 6500 Series Processor Running at 1.0 to 2.0 MHz. The Ohio Scientific 65F Floppy Disk Bootstrap PROM Option is Recommended for "Instant System Generation"

Format: The 475 supports soft and hard sector formats at single and dual densities. Standard OS-65D software configures the disk for single density soft sector format with 250K bytes of user workspace per diskette surface. OS-65D uses standard single-index hole diskettes.

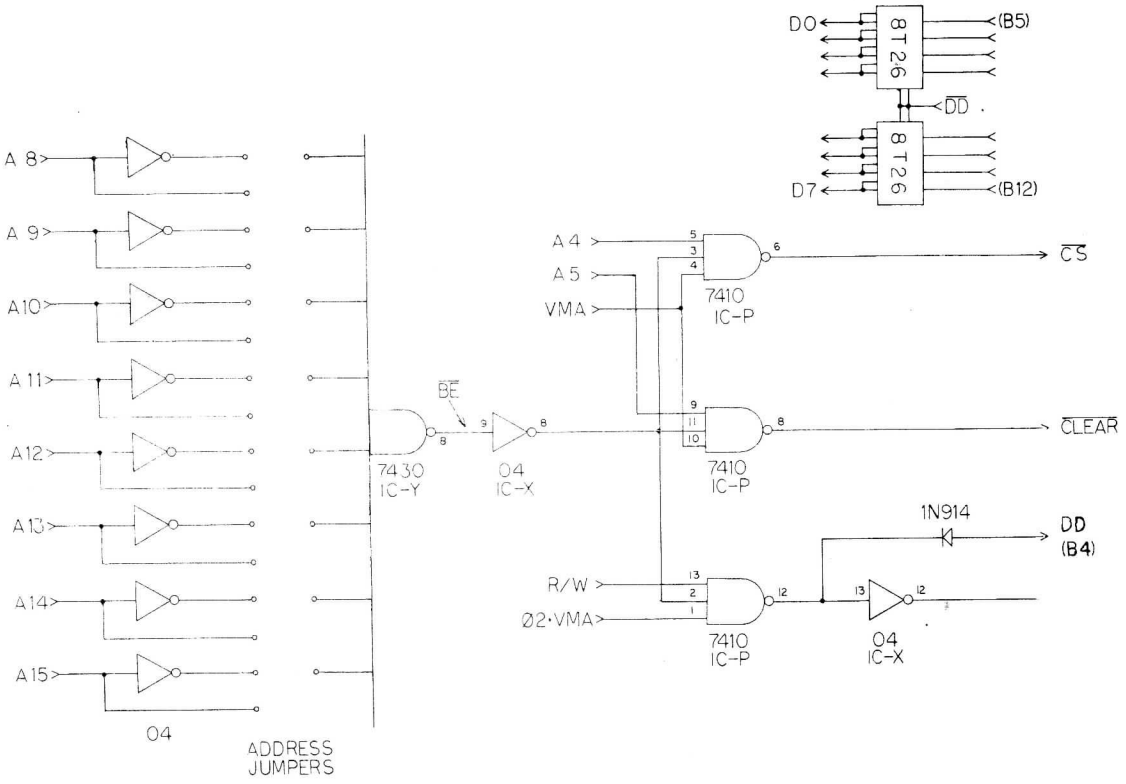


DIAGRAM 1

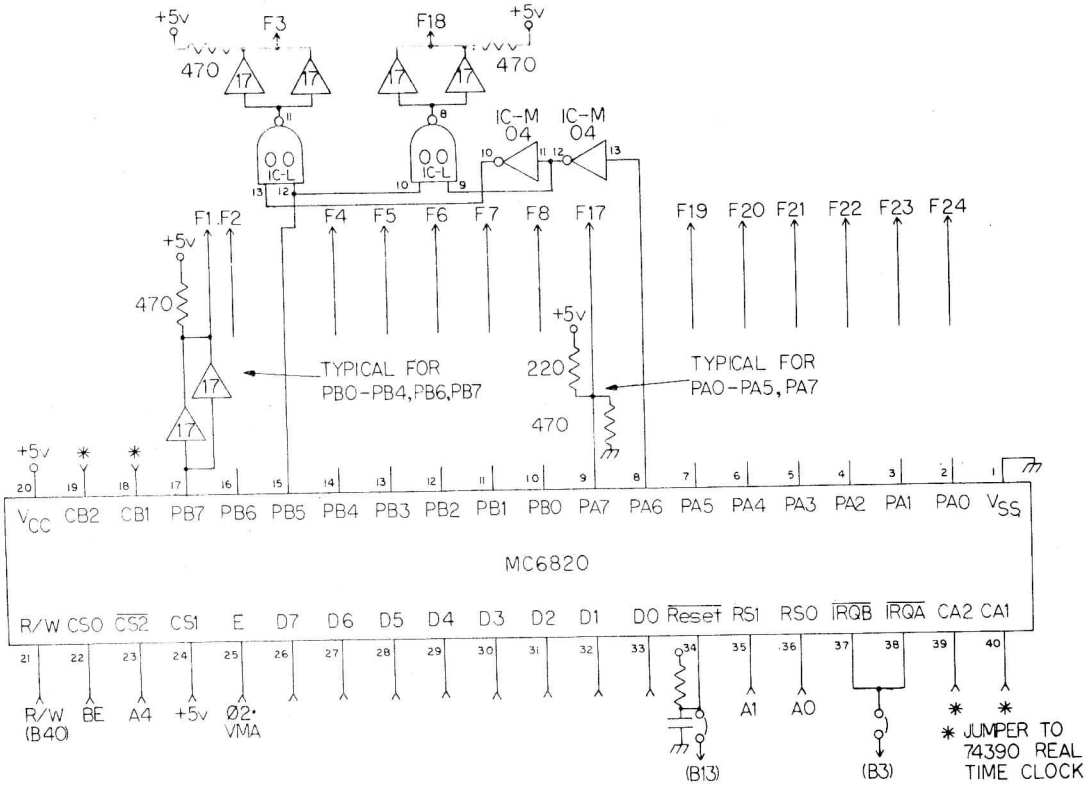


DIAGRAM 2- PIA

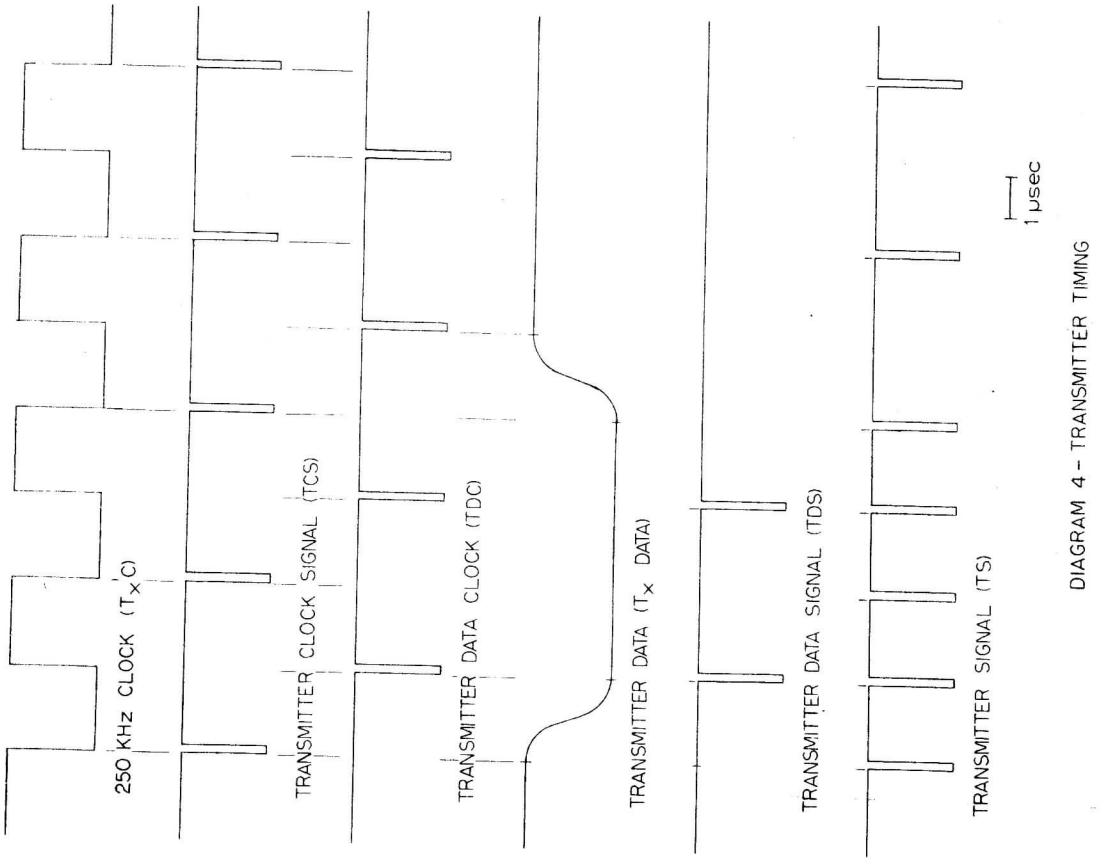


DIAGRAM 4 - TRANSMITTER TIMING

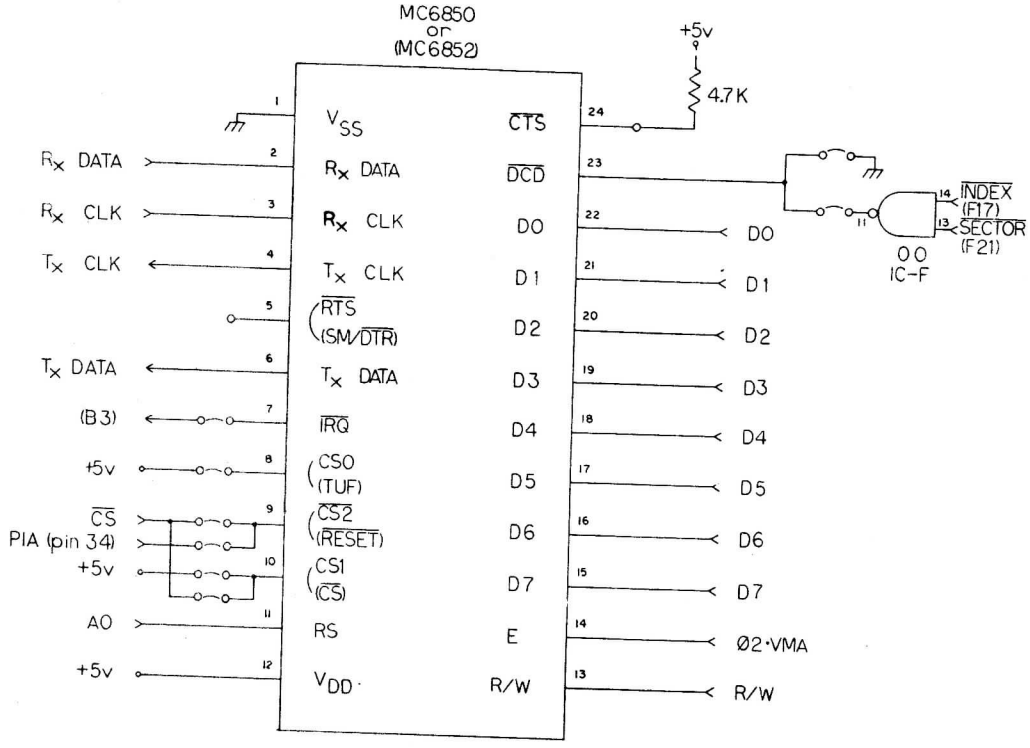


DIAGRAM 3- ACIA/SSDA

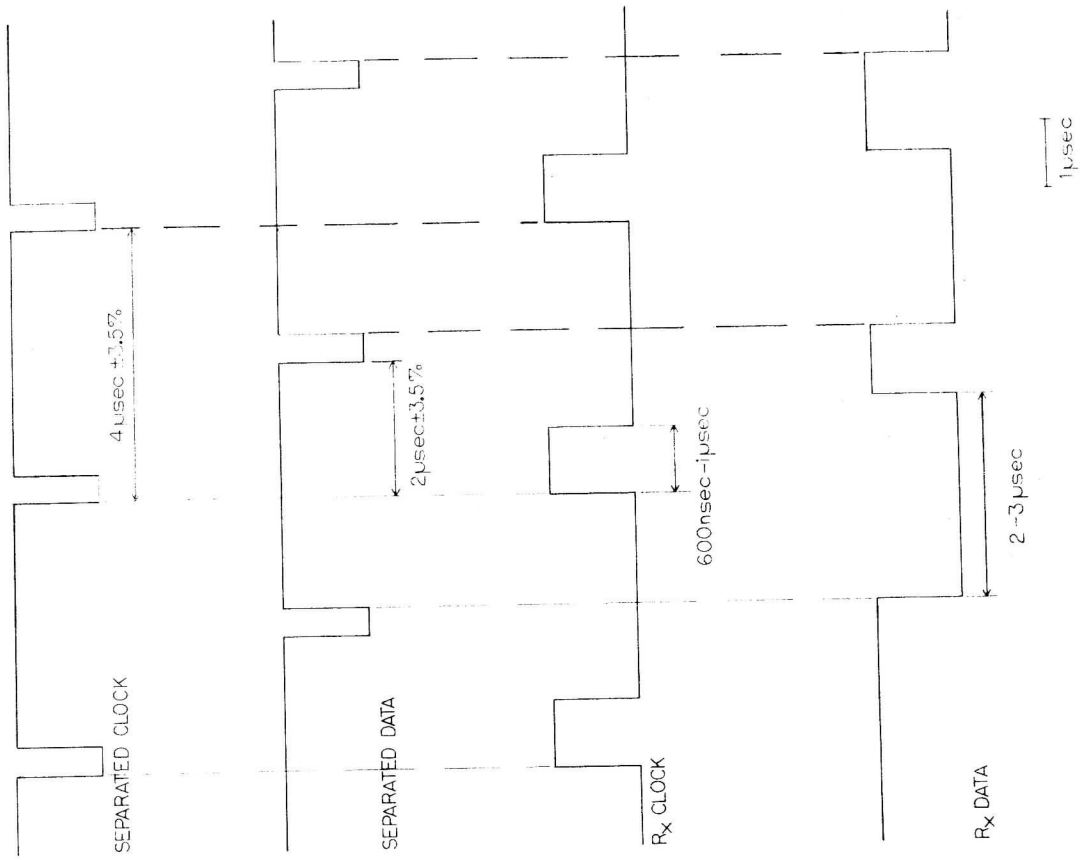


DIAGRAM 6- RECEIVER TIMING

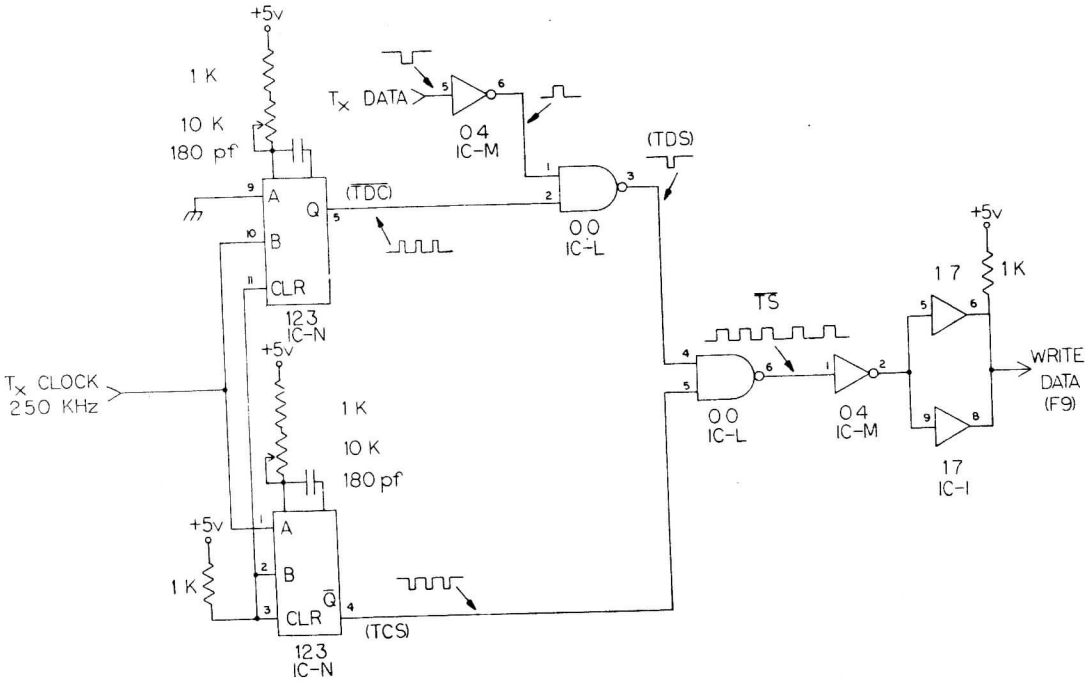


DIAGRAM 5- TRANSMIT CIRCUIT

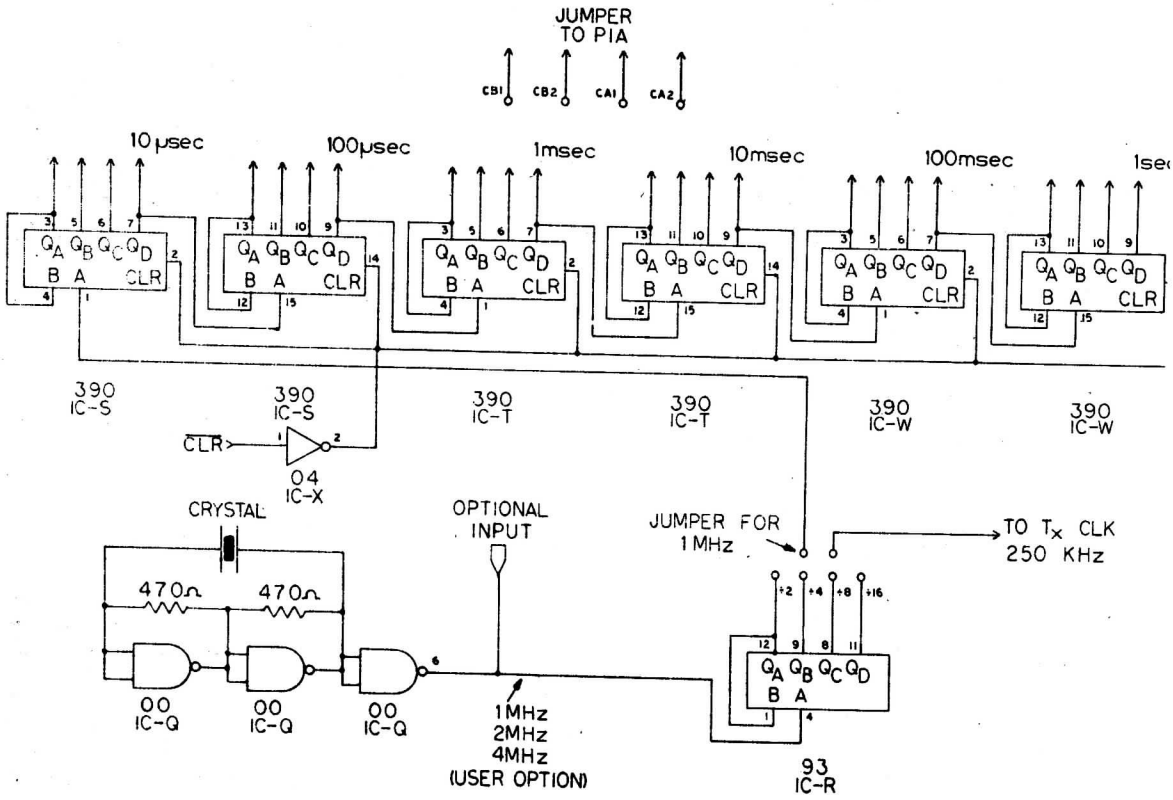


DIAGRAM 8 - OSCILLATOR/REAL TIME CLOCK

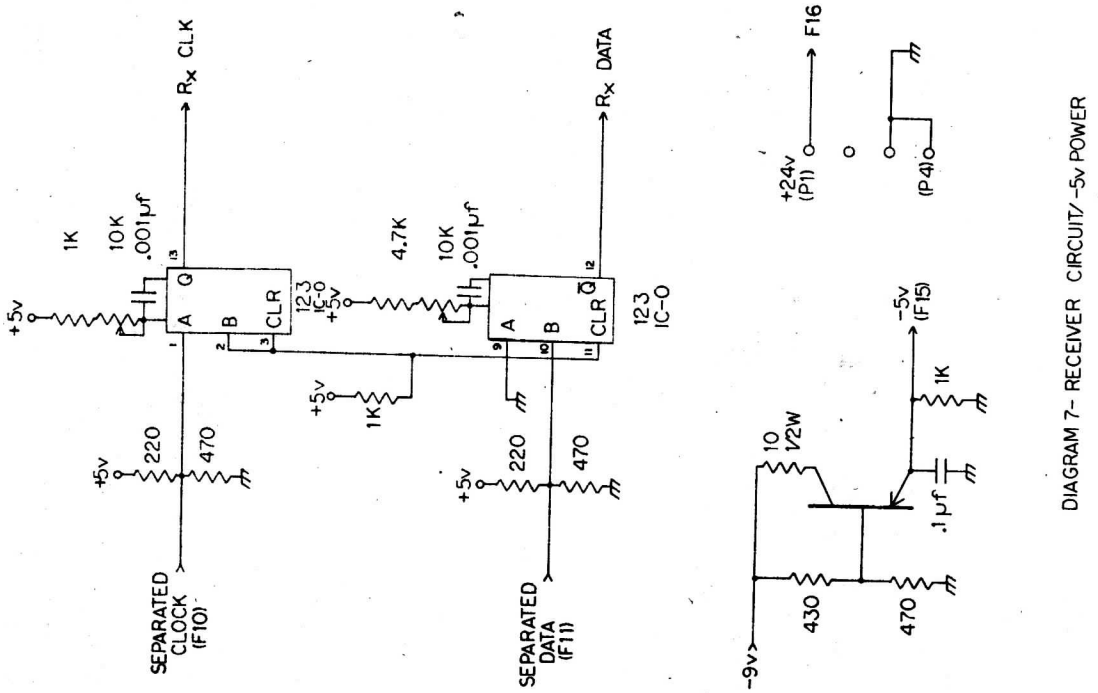


DIAGRAM 7 - RECEIVER CIRCUIT/-5v POWER

Table 1. Floppy Disk Connections

470 Board	PIA Assignment	Signal Name	GSI 105
F_1	PB7	Head Load	V
F_2	PB6	Low Current	7
F_3	PB5	Select Drive 1	14 on Drive 1
F_4	PB4	Fault Reset	D
F_5	PB3	Step	F
F_6	PB2	Step In	S
F_7	PB1	Erase Enable	J
F_8	PB0	Write Enable	H
F_9		Write Data	L
F_{10}		Separated Clock	W
F_{11}		Separated Data	U
F_{12}		Ground	A and 1
F_{13}		Ground	Z and 22
F_{14}		+5	M and 11
F_{15}		-5	20
F_{16}		+24	B and 2
F_{17}	PA7	Index	E
F_{18}	PA6	Select Drive 2	14 on Drive 2
F_{19}	PA5	Write Protect (optional)	R
F_{20}	PA4	Ready (Drive 2)	12 on Drive 2
F_{21}	PA3	Sector (optional)	21
F_{22}	PA2	Fault	K
F_{23}	PA1	Track 00	N
F_{24}	PA0	Ready (Drive 1)	12 on Drive 1

Twisted pair grounds should be terminated at the disk and the G connectors at the 470 board. Power connections can alternately be directly to the disk drives. When two drives are used, all lines except for Ready and Select are simply fed to both drives!

480 Backplane

Description:

The OSI 480 is a standard 8-slot backplane board for use on any OSI system. The board also has provisions for address and control line buffering which allows 480 boards to be connected together, yielding up to 250 slot in ultra-large OSI systems. These buffers and an on-board prototyping area can also accommodate the KIM-1. OSI APP Note #5 covers this subject in some detail.

Applications:

The 480 Board is used in any OSI system having more than one board. A second backplane or partial backplane (fewer than eight slots) is typically used with the 560Z Board.

Specifications:

Mechanical: 8" X 10" G-10 single sided plated board, four mounting holes, 8 slots spaced one inch apart and provisions for pull-up resistors. Additional buffering and backplane inter-connection connectors are at both ends.

495 Prototyping

Description:

The 495 is a system compatible prototyping board which can be used with point-to-point wiring or wire wrapping techniques. The board has provisions for 40 sixteen-pin packages and 8 forty-pin packages. It has the standard 48-pin bus connectors and +5 and ground distribution.

Applications:

Allows easy implementation of custom circuits in an OSI 500 or Challenger System.

Specifications:

Mechanical: 8" X 10" G-10 single sided plated board.

498 Card Extender

Description:

The 498 card edge extender is for extending a board out of the card cage for easy servicing. The extender has connectors along the top to service Challenger system boards and along the side to service some OSI 400 configurations.

Specifications:

8" X 10" G-10 double-sided plated through hole board.

Model 500

Description:

The state-of-the-art Model 500 Single Board Computer is fully compatible with the Ohio Scientific 48-pin bus and all Ohio Scientific Accessory Boards. The Model 500 is based on the 6502 microprocessor by MOS Technology. This chip is second sourced by Synertek and third sourced by Rockwell International. The Model 500 accepts 8 2K X 8 2616 Mask programmed ROMs (normally containing our 8K BASIC by Microsoft). 2704s, 2708s, 2716s, or similar parts can be used instead of the ROMs if the user has a custom application using his own software. Space is alsq provided for 4K of 2102-type RAM, an ACIA based serial interface which can be populated for RS-232 or 20ma current loop. Options include a PIA based parallel I/O port, 256K Memory Management (allows the system to address up to 256K memory), and up to three 1702-type PROMs.

Applications:

The 500 CPU Board can be used as a powerful small system. It is especially powerful because if has "instant 8K BASIC" and because of its 4K of on-board RAM memory. It can also be used as the basis of a larger Challenger type system. It is capable of supporting additional memory, our 430B Audio Cassette Interface, our 440B Video Graphics Board, our Floppy Disk Drive, and all other peripheral devices offered by Ohio Scientific. If a person already has an Ohio Scientific system, the 500 Board can be used to store 8K BASIC in ROM and as a 4K RAM board.

Specifications:

Mechanical: 8" X 10" G-10 Double-Sided Plated Through Hole Board

Electrical: +5 Volts at 2 Amps
-9 Volts at 500ma

Processors: Supports the 6502 or 6502A. Can be used as the controller for the 560Z which offers Z-80 and 6100.

PROM: Supports three 1702-type PROMs. Ohio Scientific offers 65A Serial PROM Monitor, 65V Video PROM Monitor, and Floppy Disk Bootstrap PROMs.

RAM: Can support up to 4K X 8 2102 type RAM

Firmware: 8K BASIC in ROM (User can supply own software in ROM)

Serial I/O: Serial Interface can be configured for RS-232 or 20ma. loop. 5 possible baud rates are jumper selectable.

Other Features: Buffering to drive up to 250 Ohio Scientific System Boards.
Memory Management for up to 256K Bytes of Memory.
PIA based parallel port also available.

OHIO SCIENTIFIC			product name/number 500/C2-0/C2-1/C2-8V/C2-8S/C2-4P	
date 8/77	revision A	page 41	status Production	sheet 1 of 1

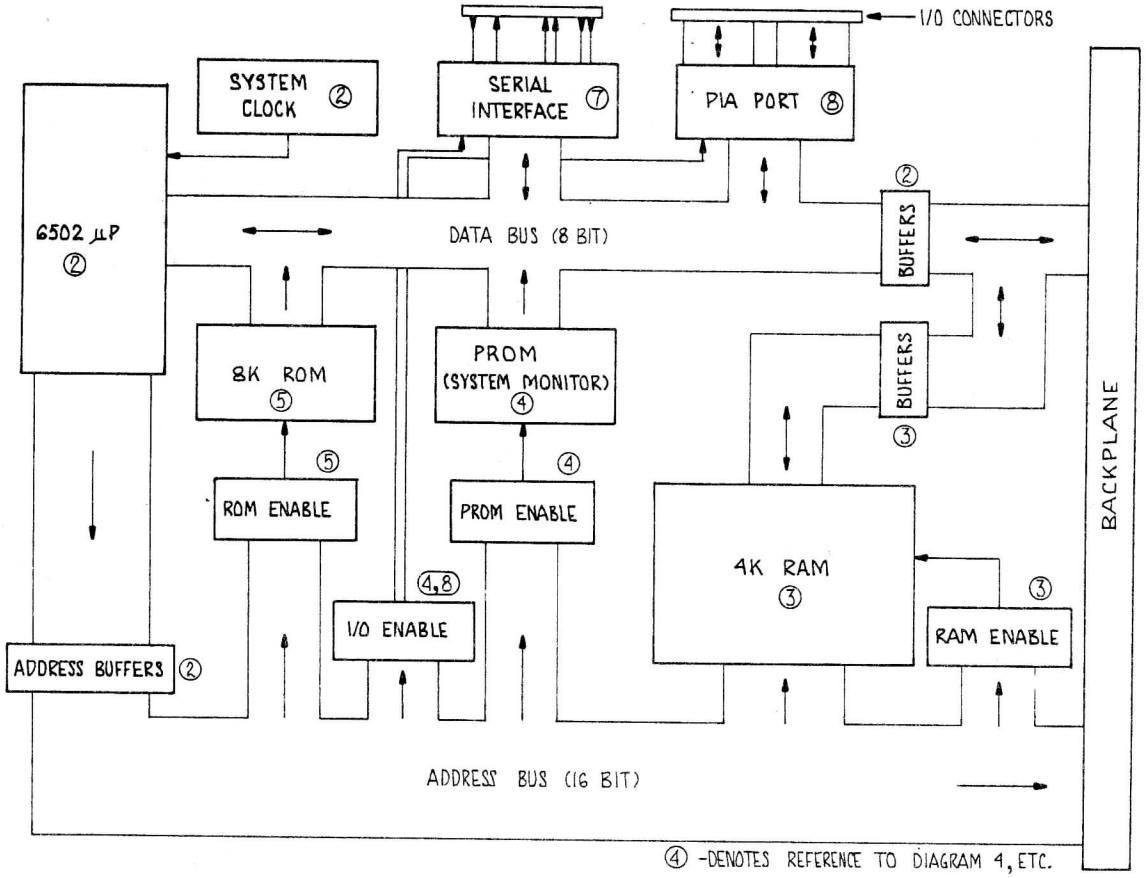


DIAGRAM 1 - SYSTEM OVERVIEW

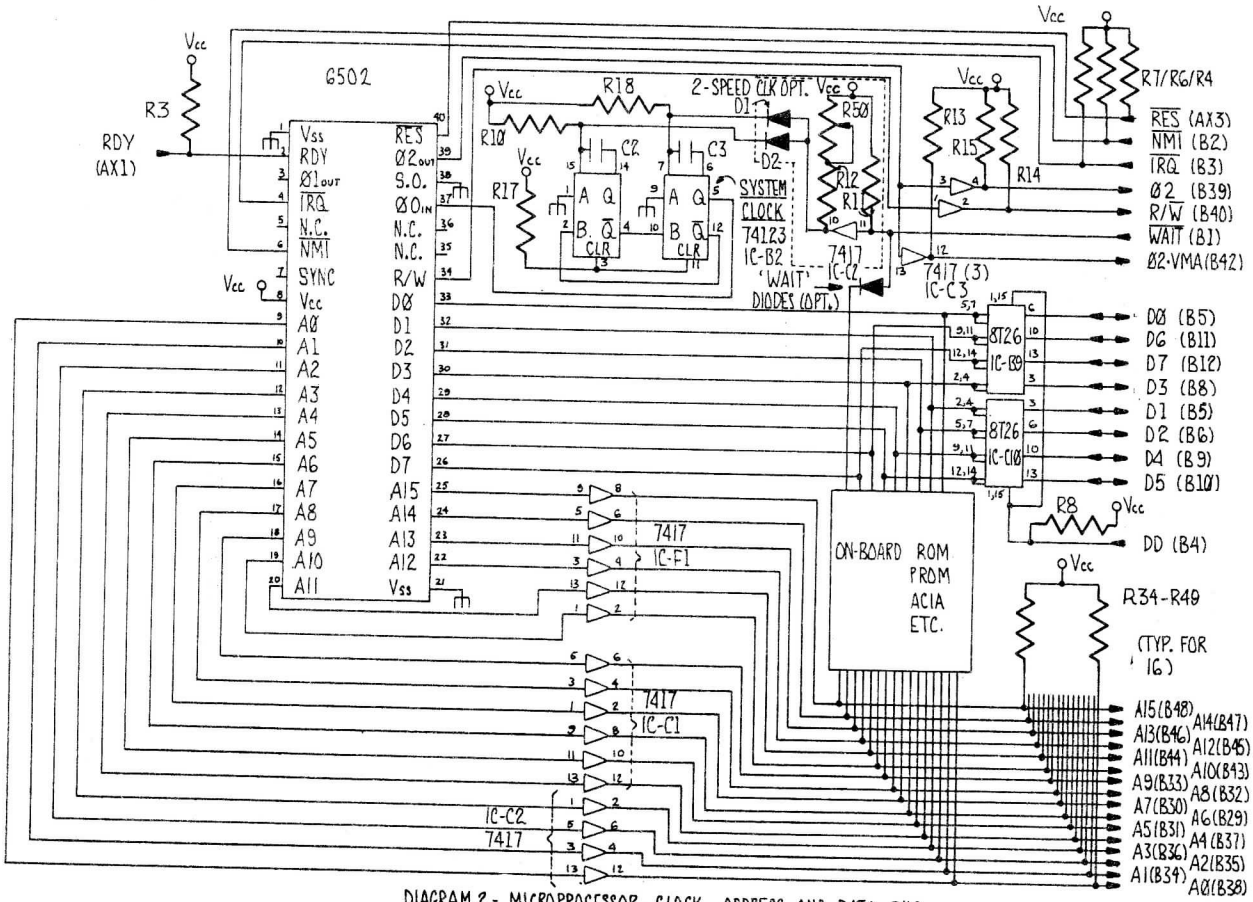


DIAGRAM 2 - MICROPROCESSOR, CLOCK, ADDRESS AND DATA BUS

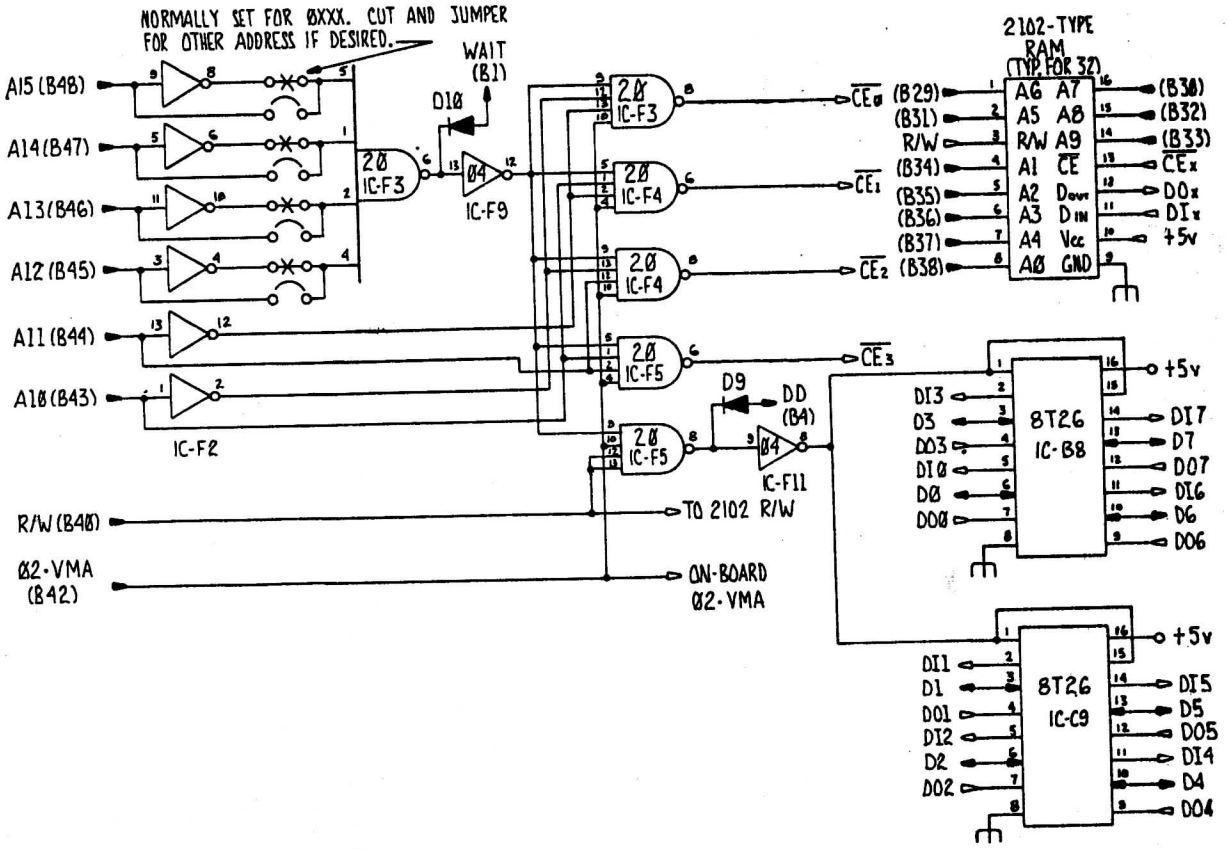


DIAGRAM 3- RAM IMPLEMENTATION

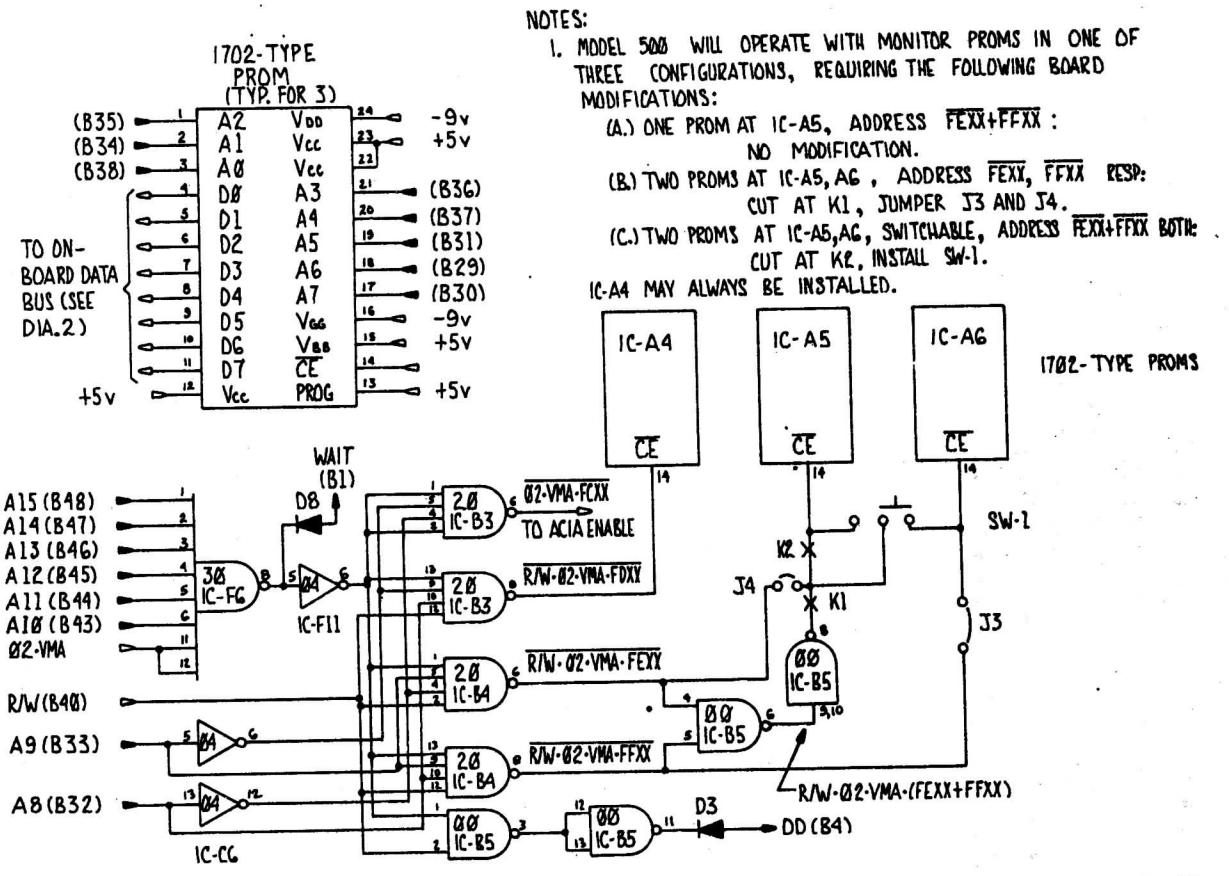
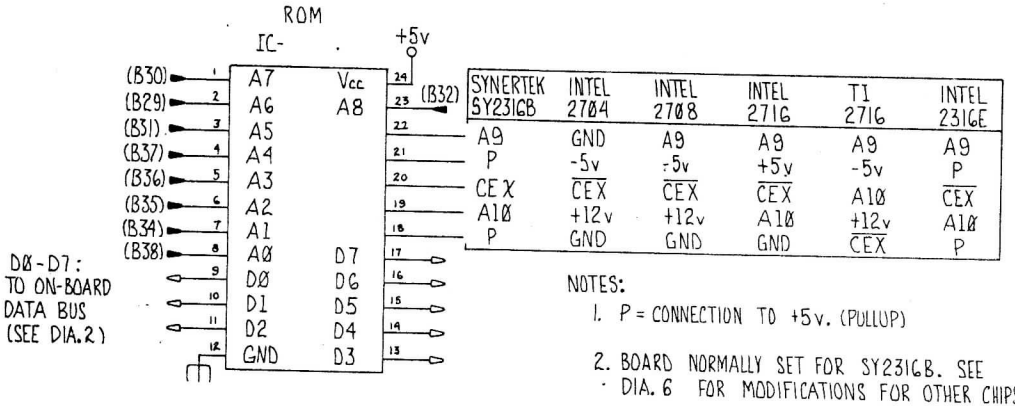


DIAGRAM 4- 1702-TYPE PROM IMPLEMENTATION



SYNERTEK SY2316B	INTEL 2704	INTEL 2708	INTEL 2716	TI 2716	INTEL 2316E
A9	GND	A9	A9	A9	A9
P	-5v	-5v	+5v	-5v	P
$\overline{CEX}$	$\overline{CEX}$	$\overline{CEX}$	$\overline{CEX}$	A10	$\overline{CEX}$
A10	+12v	+12v	A10	+12v	A10
P	GND	GND	GND	$\overline{CEX}$	P

NOTES:

1. P = CONNECTION TO +5v. (PULLUP)
2. BOARD NORMALLY SET FOR SY2316B. SEE DIA. 6 FOR MODIFICATIONS FOR OTHER CHIPS.

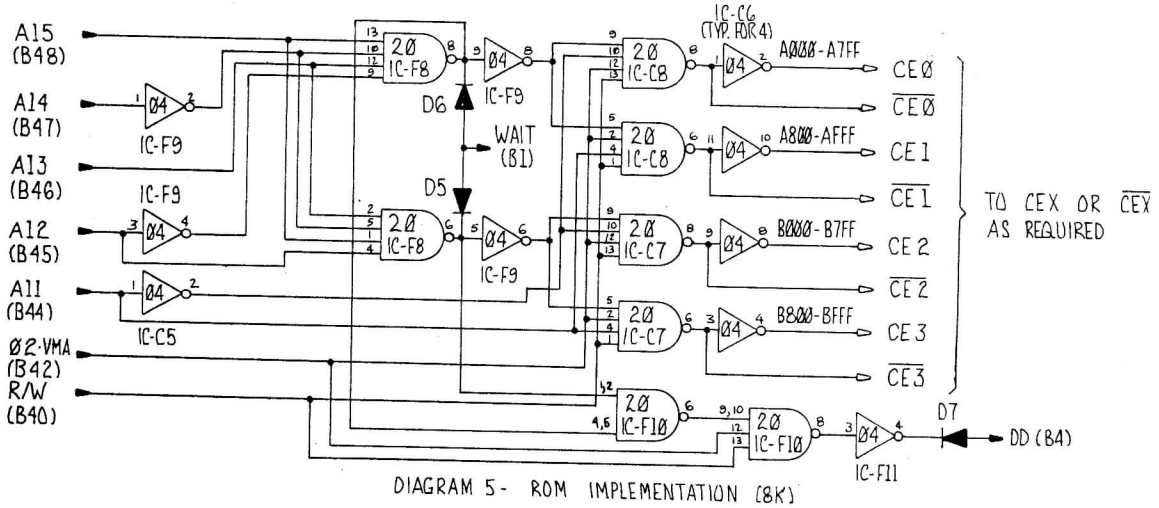
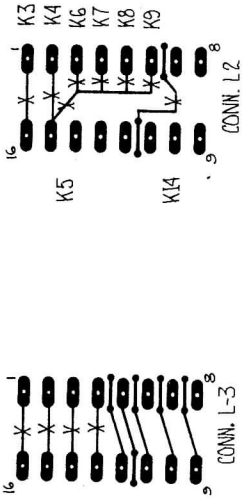


DIAGRAM 5- ROM IMPLEMENTATION (8K)

SYNERTEK SY2316B	INTEL 2704	INTEL 2708	INTEL 2716	TI 2716	INTEL 2316E
CUT	CUT	CUT	CUT	CUT	CUT
NONE REQ'D.	K-3 K-4 K-5 K-10 K-11 K-12 K-13 K-14	K-3 K-4 K-5 K-10 K-11 K-12 K-13	K-5 K-10 K-11 K-12 K-13	K-3 K-4 K-6 K-7 K-8 K-9 K-10 K-11 K-12 K-13	K-10 K-11 K-12 K-13
JUMPER	JUMPER	JUMPER	JUMPER	JUMPER	JUMPER
NONE REQ'D.	L2 p.7-p.6 p.8-p.1 p.9-p.2 L3 p.8-p.7 p.9-p.4 p.10-p.3 p.11-p.2 p.12-p.1	L2 p.7-p.6 p.8-p.1 p.9-p.2 L3 p.9-p.4 p.10-p.3 p.11-p.2 p.12-p.1	L2 p.7-p.6 L3 p.5-p.1 p.5-p.2 p.5-p.3 p.5-p.4	L2 p.8-p.1 p.9-p.2 p.11-p.6 p.12-p.5 p.13-p.4 p.14-p.3 L3 p.5-p.1 p.5-p.2 p.5-p.3 p.5-p.4	L3 p.9-p.4 p.10-p.3 p.11-p.2 p.12-p.1

NOTE: L3 p.9-p.4 means jumper pin 9 to pin 4 of connector L3, etc.



(ABOVE) CONNECTORS L2 AND L3 SHOWING CUT POINTS. VIEW FROM REAR OF BOARD.

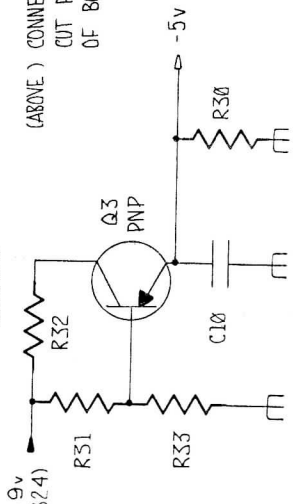


DIAGRAM 6- ROM JUMPER CONFIGURATION AND -5v POWER

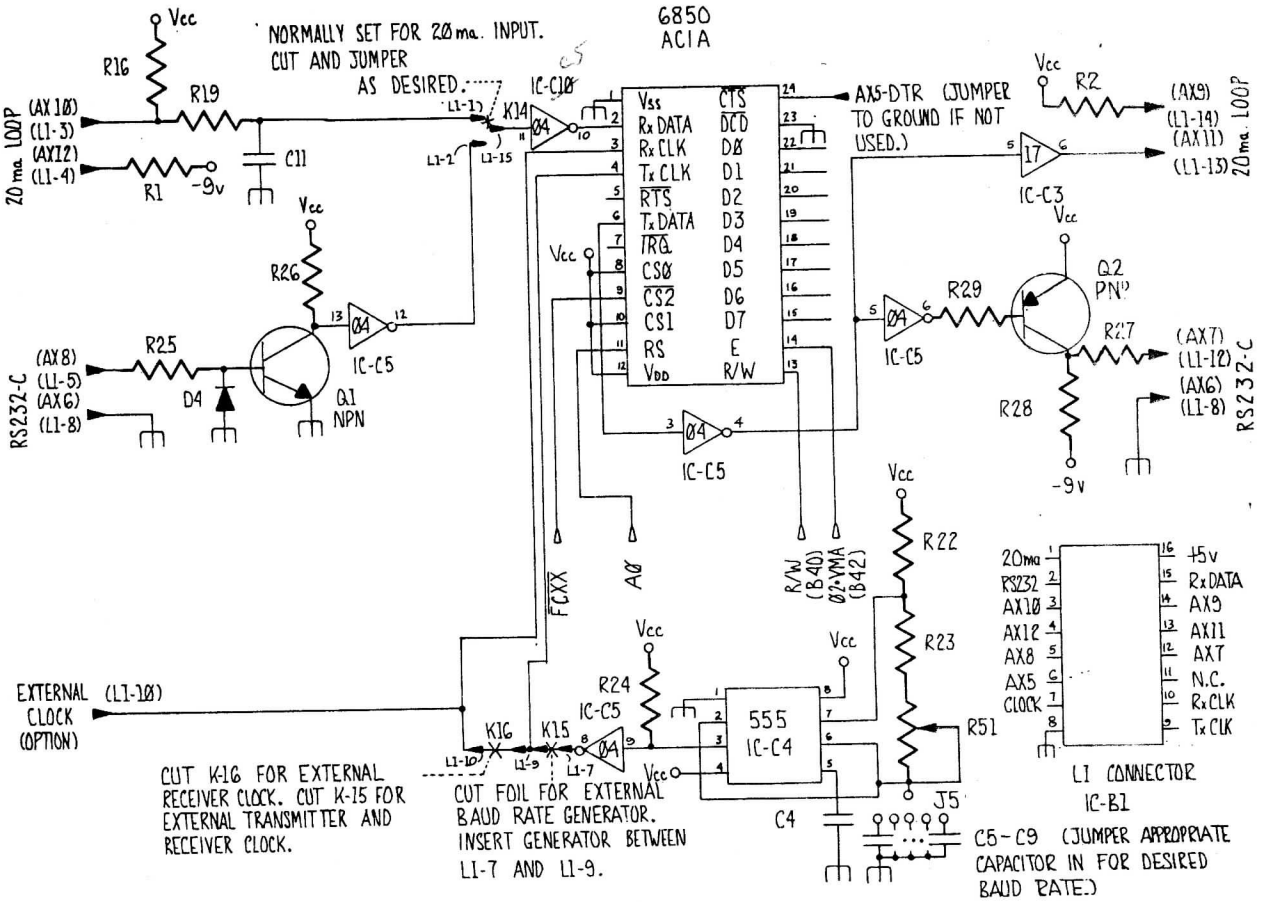
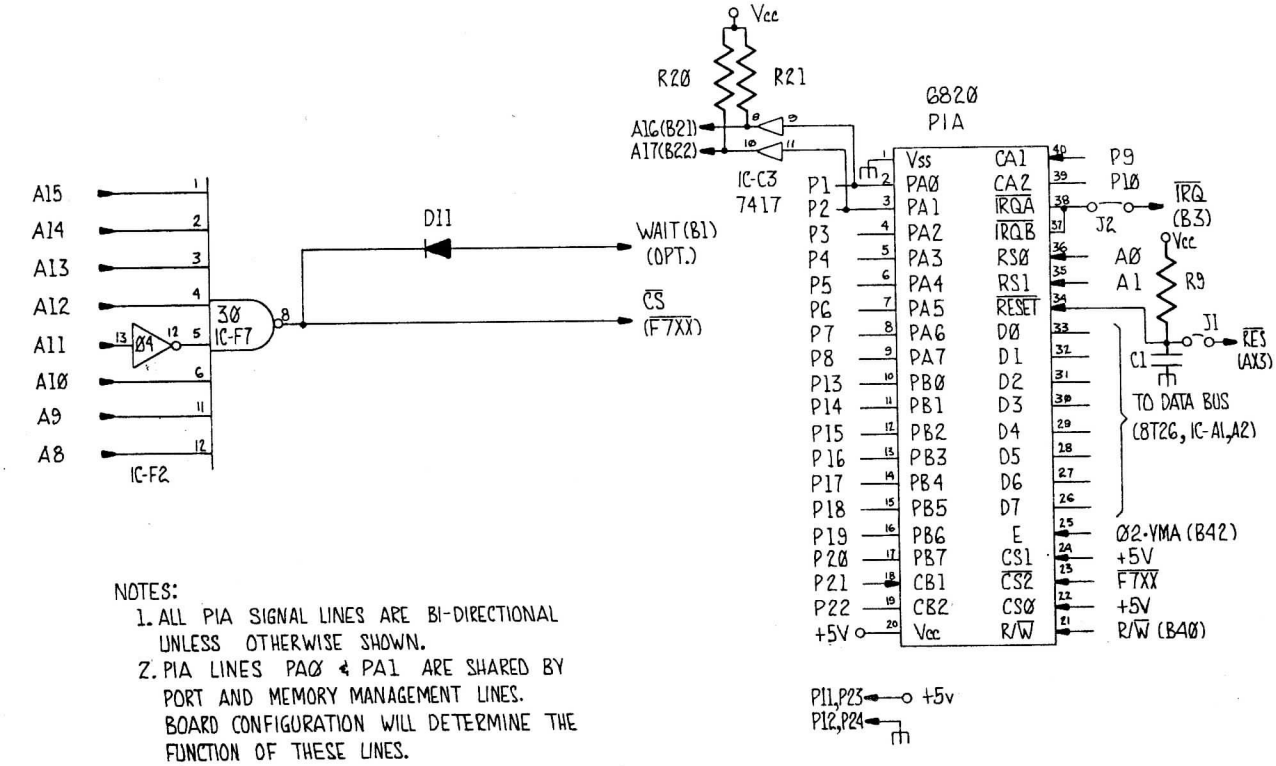


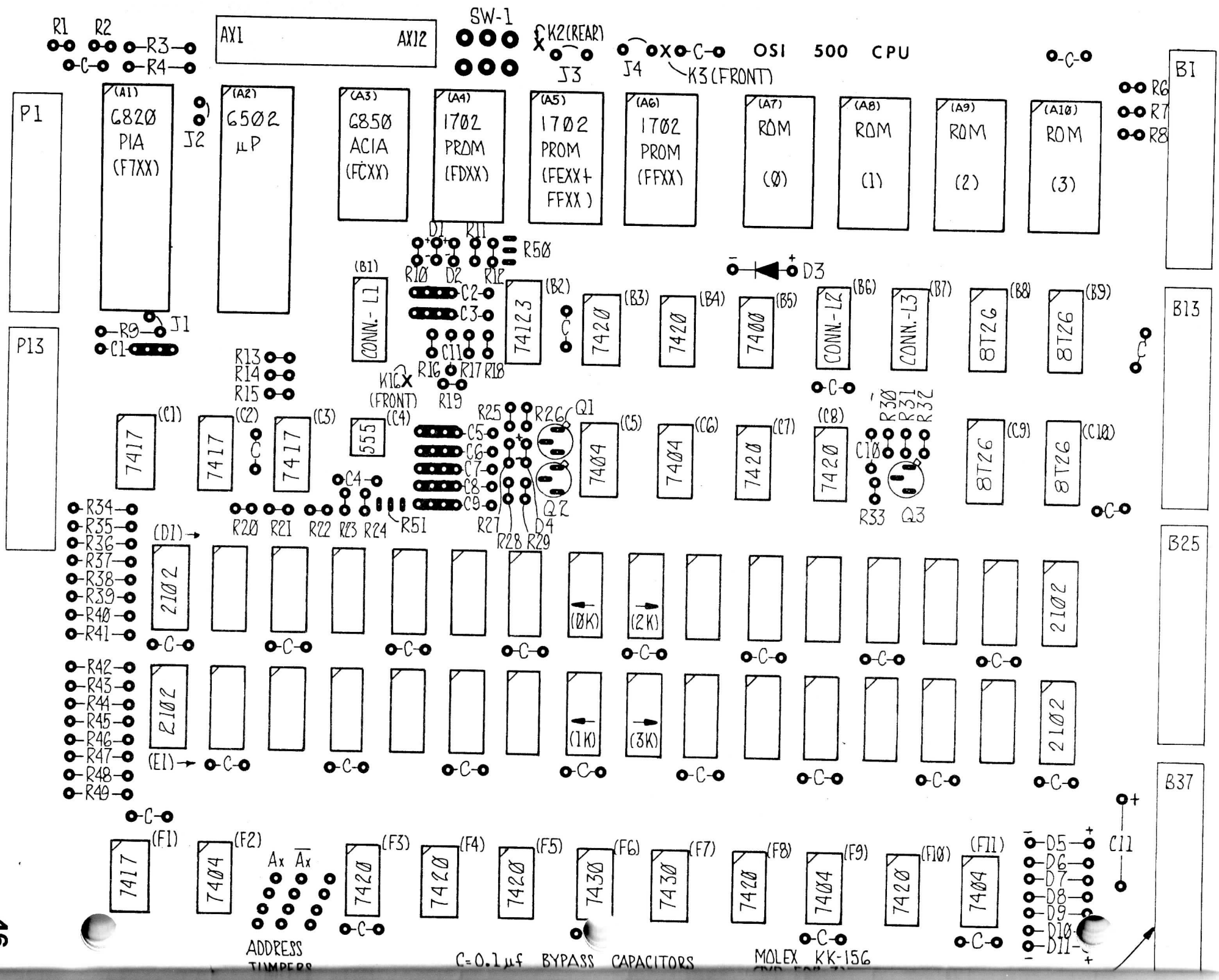
DIAGRAM 7- SERIAL INTERFACE

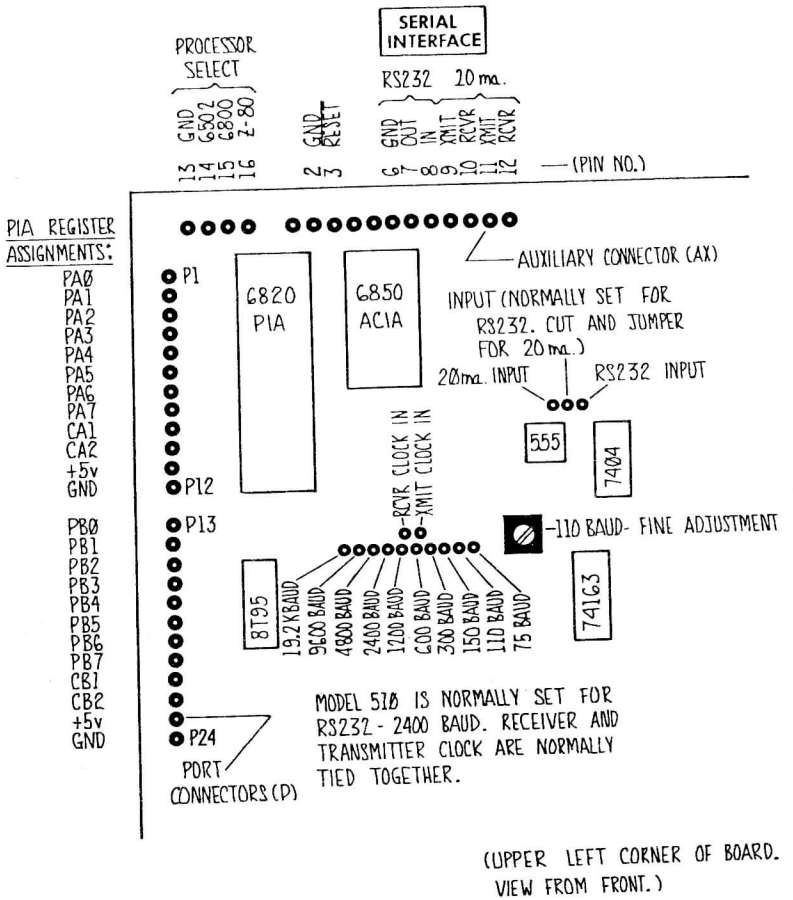


NOTES:

1. ALL PIA SIGNAL LINES ARE BI-DIRECTIONAL UNLESS OTHERWISE SHOWN.
2. PIA LINES PA0 & PA1 ARE SHARED BY PORT AND MEMORY MANAGEMENT LINES. BOARD CONFIGURATION WILL DETERMINE THE FUNCTION OF THESE LINES.

DIAGRAM 8- PIA PORT


OSI 500 CPU
P1
P13
B1
B13
B25
B37
AX1
AX12
SW-1
K2(REAR)
J3
J4
K3(FRONT)
K1(FRONT)
J1
J2
(A1) 6820 PIA (F7XX)
(A2) 6502 µP
(A3) 6850 ACIA (FCXX)
(A4) 1702 PROM (FDXX)
(A5) 1702 PROM (FEXX+ FFXX)
(A6) 1702 PROM (FFXX)
(A7) ROM (0)
(A8) ROM (1)
(A9) ROM (2)
(A10) ROM (3)
CONN.-L1
CONN.-L2
CONN.-L3
74123
555
2102
(0K)
(1K)
(2K)
(3K)
ADDRESS JUMPERS
C=0.1µf BYPASS CAPACITORS
MOLEX KK-156



(UPPER LEFT CORNER OF BOARD. VIEW FROM FRONT.)

MODEL 510 I/O CONNECTIONS

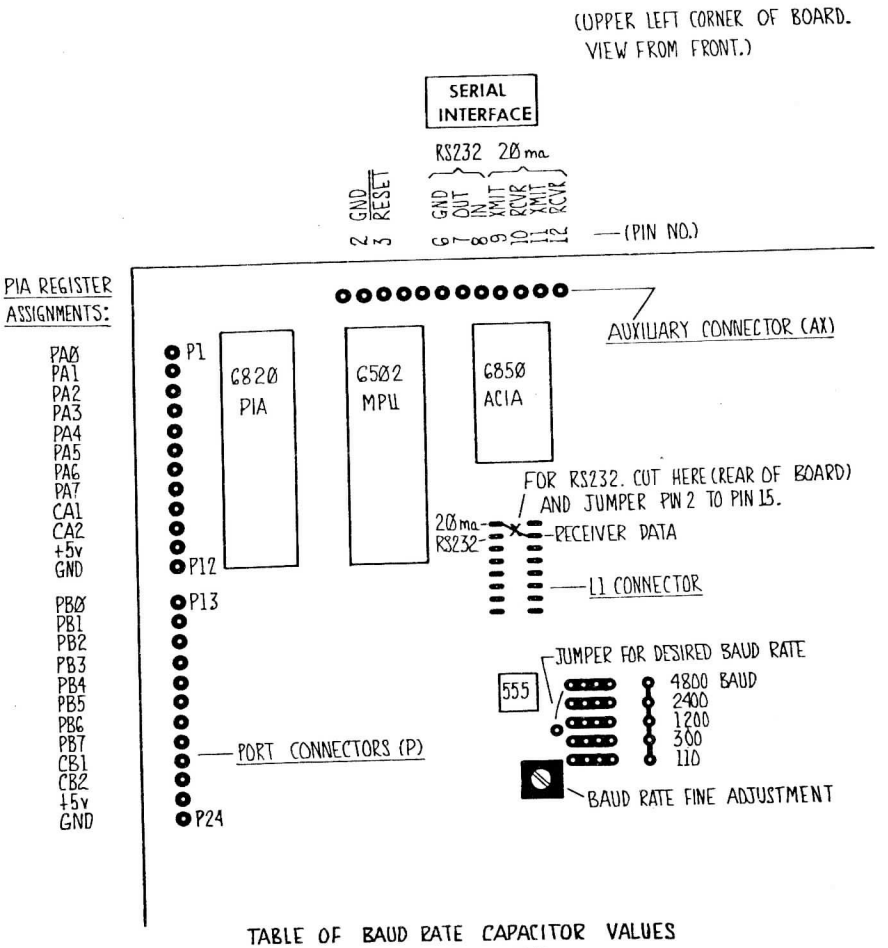


TABLE OF BAUD RATE CAPACITOR VALUES

	MIN	MID-RANGE	MAX
4800 BAUD	.001 µf	.002 µf	.0027 µf
2400	.0022	.0033	.0056
1200	.0045	.0068	.0110
300	.0179	.027	.0446
110	.0489	.082	.1216

MID-RANGE CAPACITANCE VALUES ARE RECOMMENDED, HOWEVER ANY VALUE BETWEEN MIN AND MAX MAY BE SUBSTITUTED. ALL VALUES ARE IN µf.

MODEL 500 I/O CONNECTIONS

510 CPU Board

Description:

The Model 510 CPU Board is the most technically advanced CPU Board available today for small computers. It is always supplied with three processors; 6502A, 6800, and Z-80. One processor is run at a time; an optional software switch is available to permit the user to change processors under software control. When the user switches processors, memory contents are preserved. The board can also be provided with "megabyte memory pager" allowing up to 1 megabyte of memory to be addressed. The CPU board can be configured to handle up to 16 users on a single system. Other features of the board include a serial interface with crystal controlled baud rate generator capable of operating from 110 to 19,200 baud. Up to three PROM Monitors can be provided for the 6502 and one for the 6800. The 510 Board is automatically configured for disk use.

Applications:

The Model 510 allows the user to have three processors for about $200 more than one processor. This is ideal for industrial development applications where an engineer wishes to compare three different processors. It is also ideal for small business systems as it allows up to 16 users. The three processors insure the businessman that his machine won't become obsolete when a new software package comes along--simply because he chose the wrong processor. These same reasons make the 510 ideal for educational as well as home use. Since the 510 is fully compatible with all of Ohio Scientific's peripherals (it is also used as the heart of the Challenger III systems), and since it is fully expandable, it is the ideal CPU for almost all applications. It allows the user to have the flexibility of owning three powerful computer systems at slightly over the cost of owning one!

Specifications:

Mechanical: 8" X 10" G-10 Epoxy Double-Sided Plated Through Hole Boards

Electrical: +5V at 2amps
-9V at 500ma

Processors: Comes standard with 6502A, 6800, and Z-80

PROM: Supports up to three 1702 type PROMs for the 6502, and one PROM for the 6800

Serial I/O: One Serial Interface can be configured for RS-232 or 20ma loop. Crystal controlled baud rate can be set from 110 baud to 19,200 baud

Parallel I/O: Offers one PIA based parallel port (optional)

Other Features: Allows one-megabyte memory management
Allows up to 16 users on a system
Comes configured for disk operation
Software Switch Option enables user to change from processor to processor under software control. When processors are changed (even if change is manual) memory is preserved.

OHIO SCIENTIFIC			product name/number 510/C3-8/C3-0	
date 8/77	revision A	page 48	status Production	sheet 1 of 1

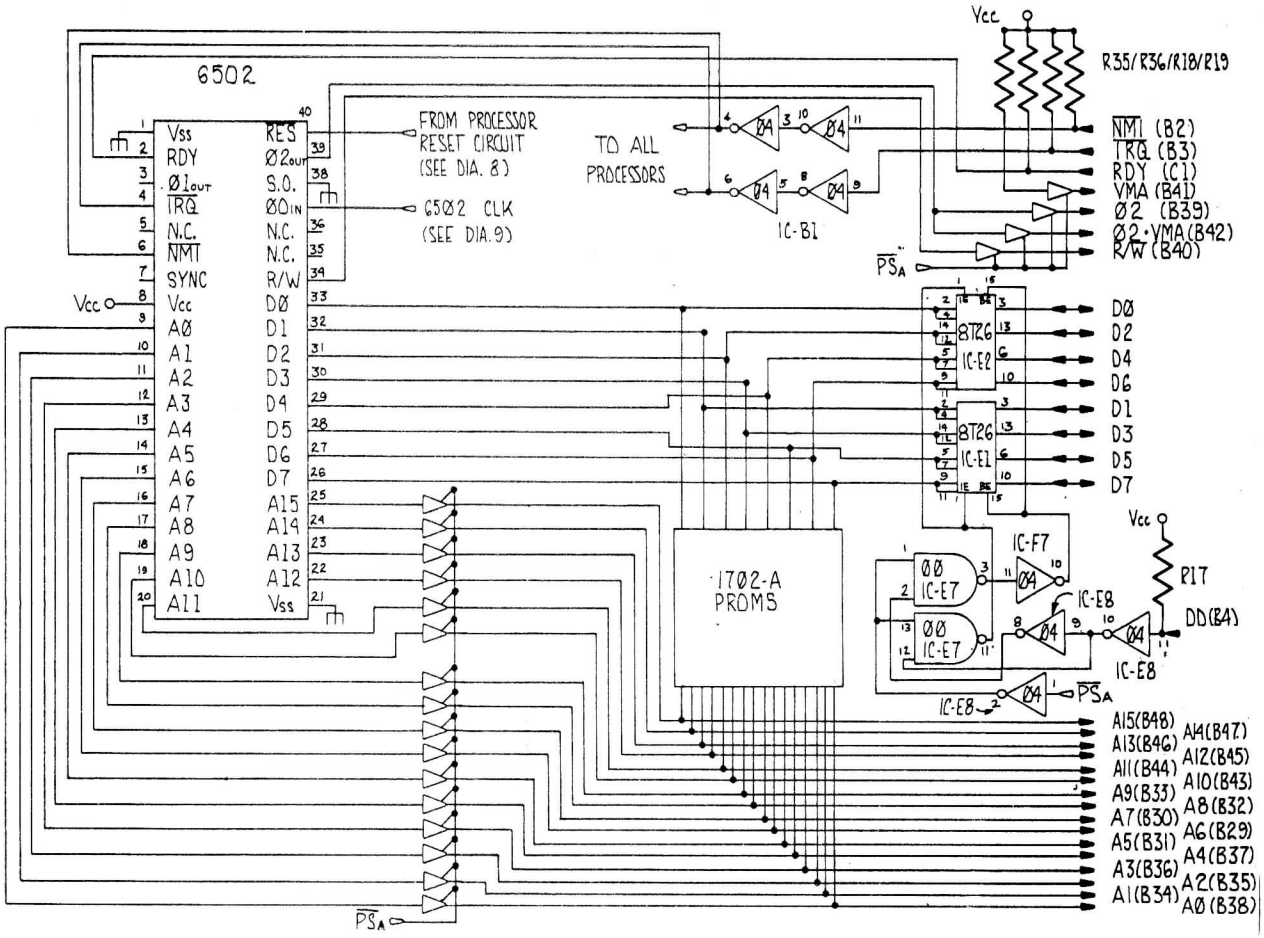


DIAGRAM 2- 6502 CIRCUITRY

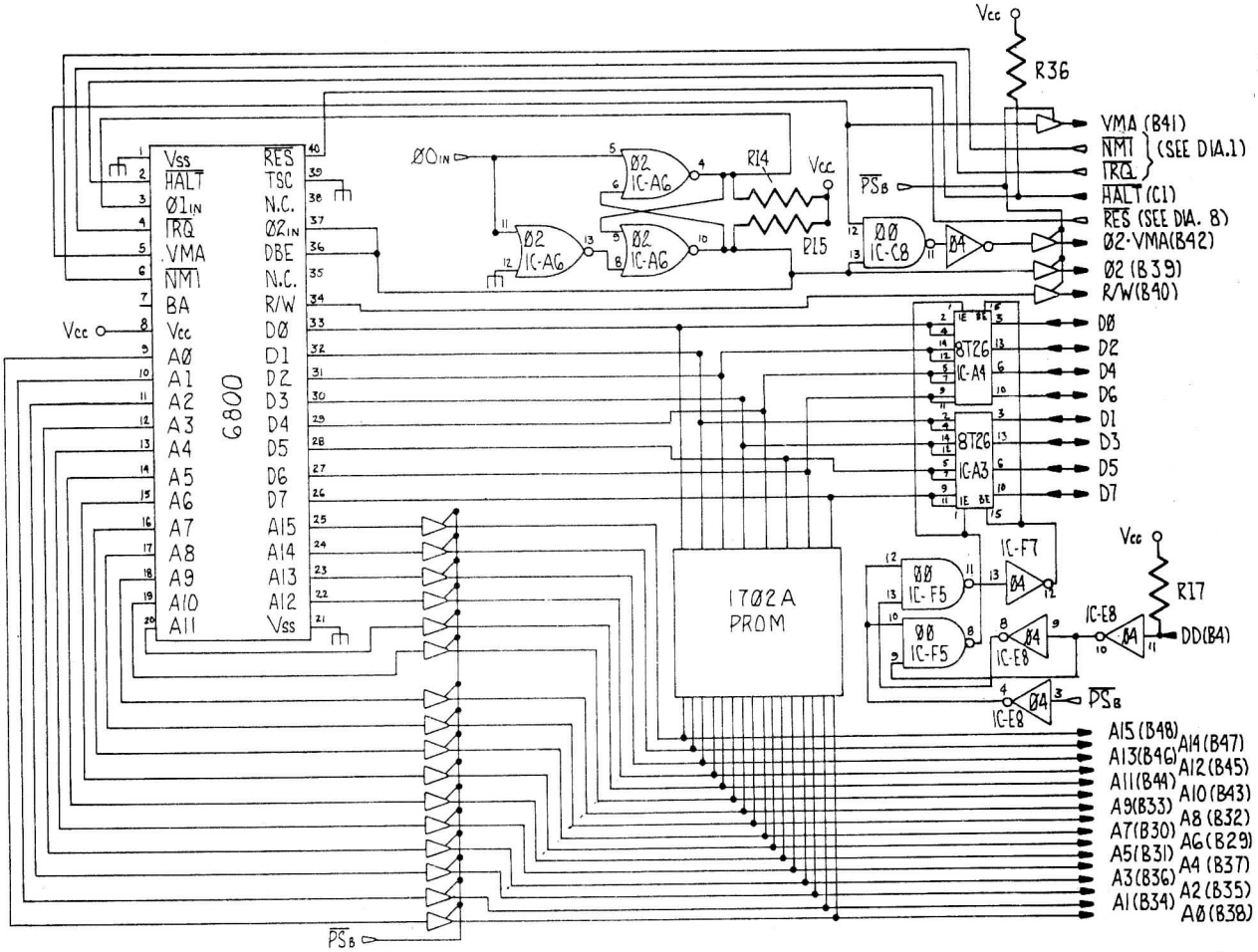


DIAGRAM 3- 6800 AND CIRCUITRY

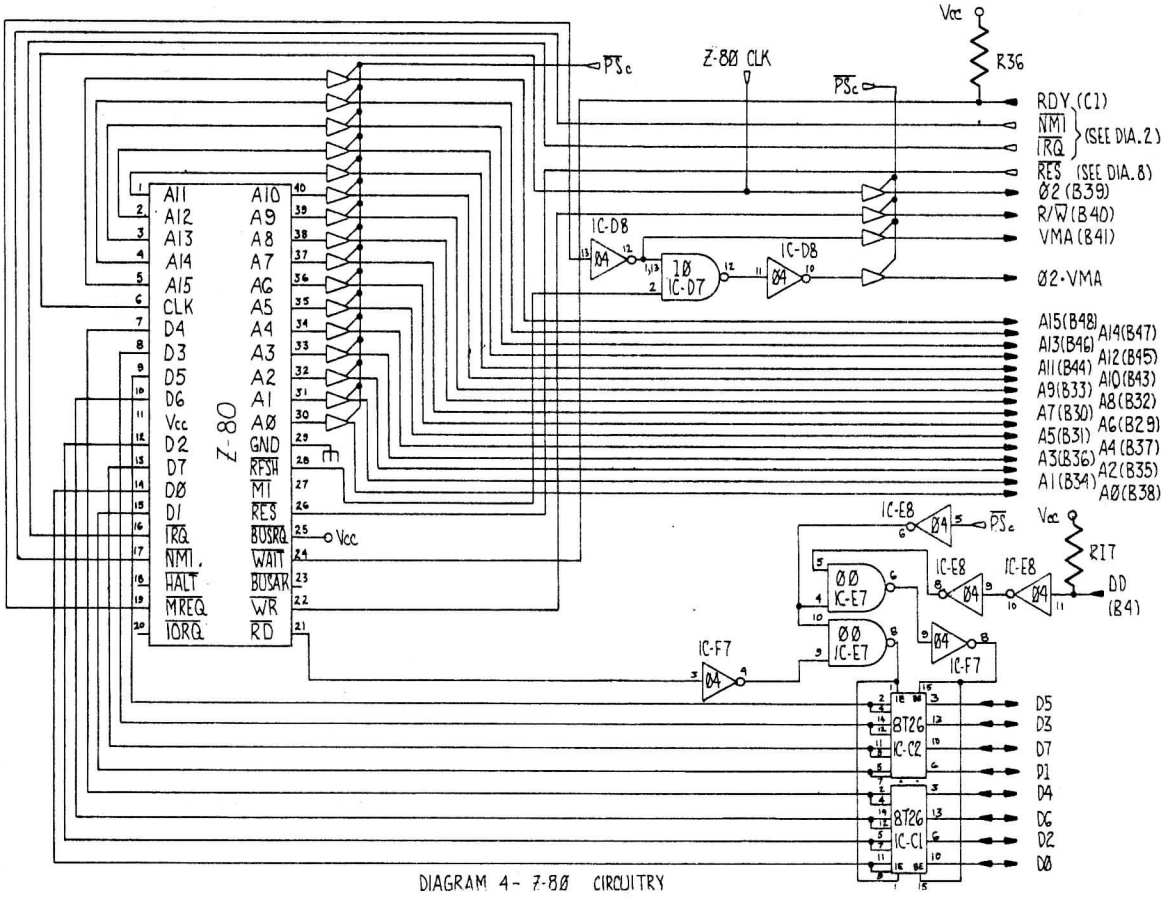


DIAGRAM 4- Z-80 CIRCUITRY

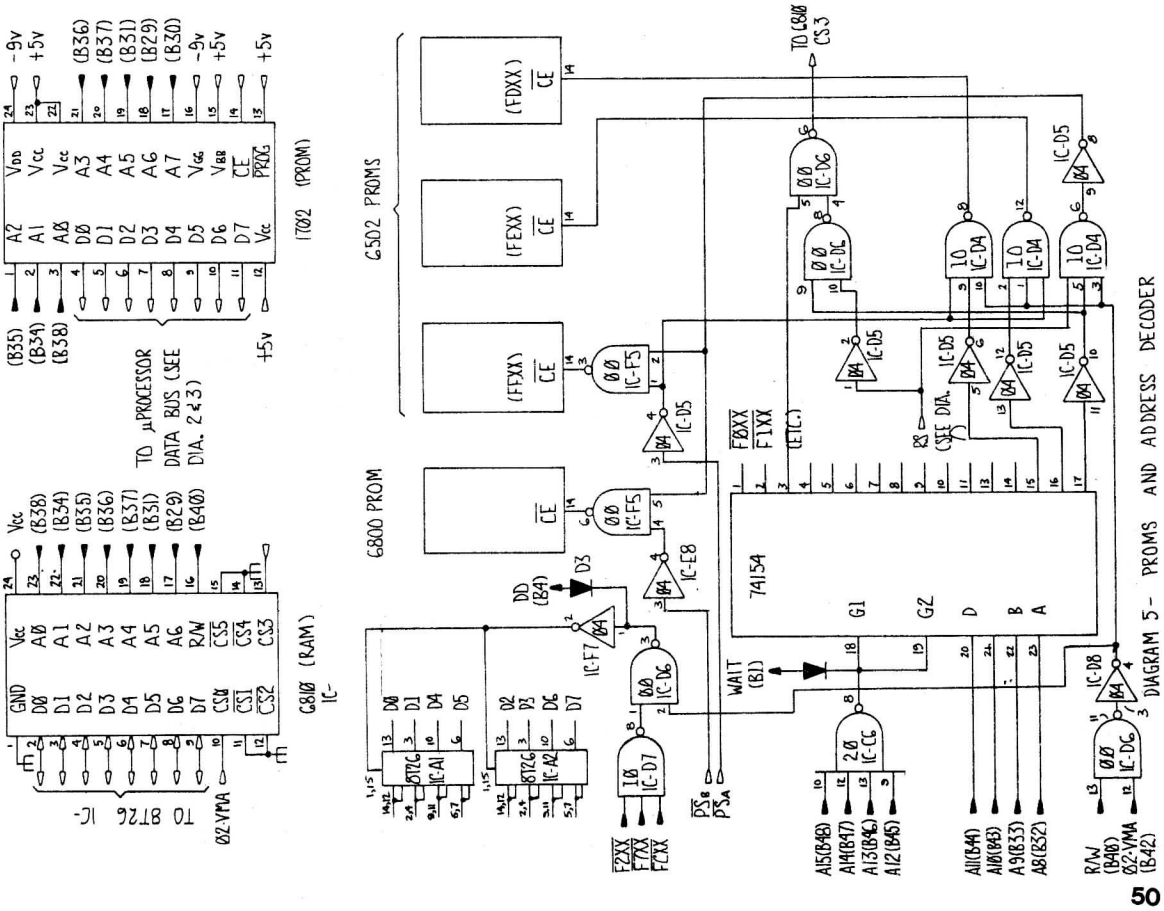


DIAGRAM 5- PROMS AND ADDRESS DECODER

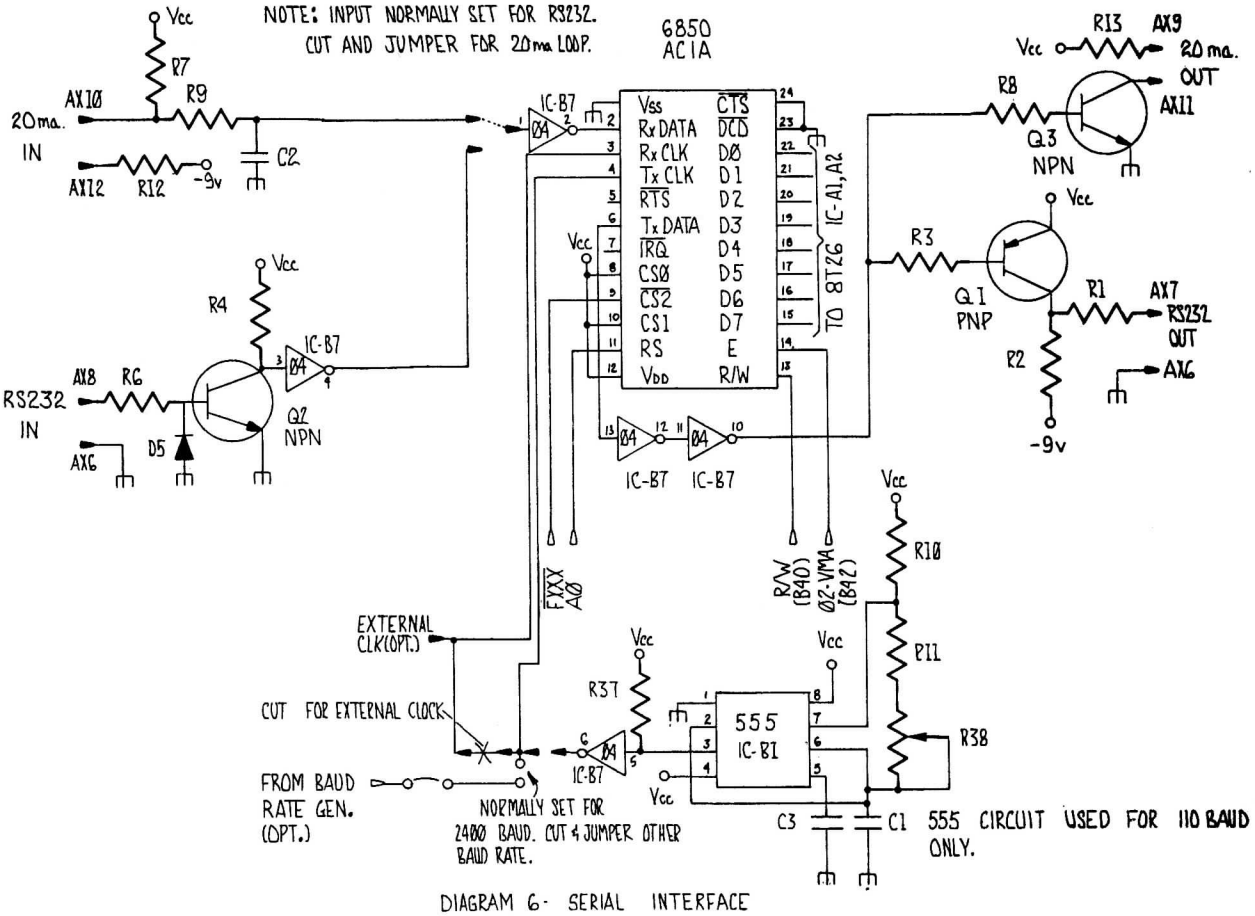
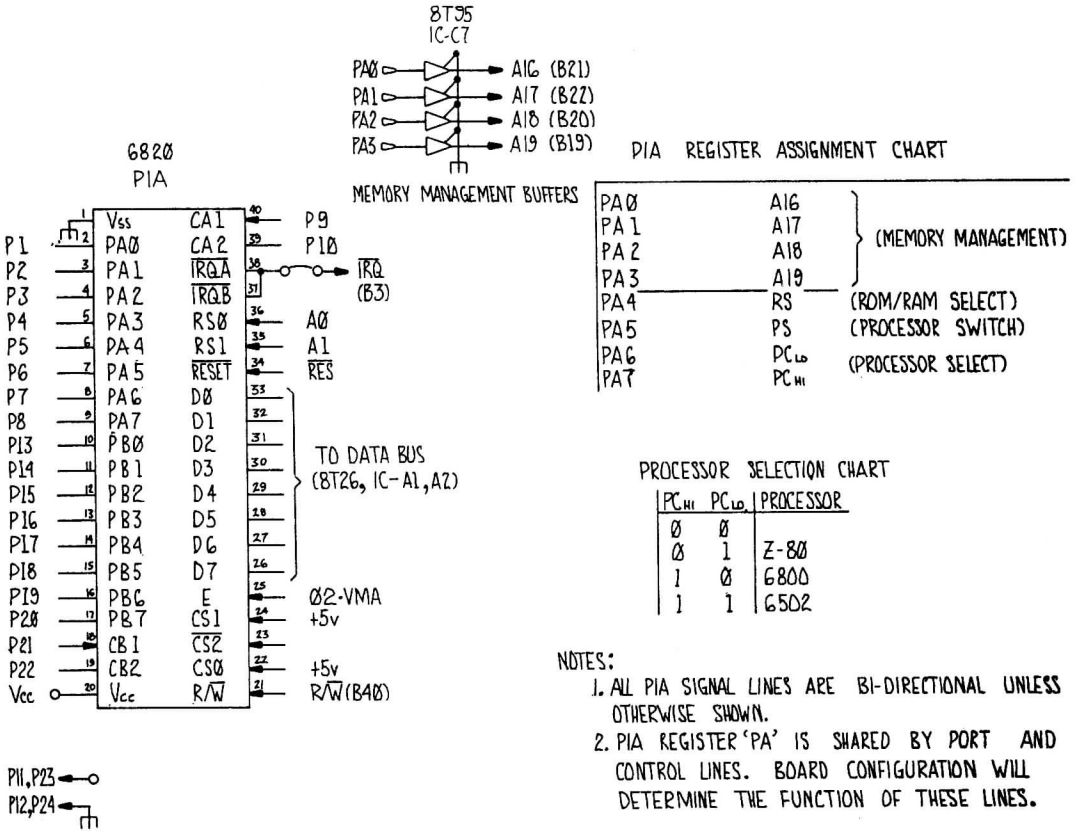


DIAGRAM 6- SERIAL INTERFACE



PIA REGISTER ASSIGNMENT CHART

PA0	A16	(MEMORY MANAGEMENT)
PA1	A17	
PA2	A18	
PA3	A19	
PA4	RS	(ROM/RAM SELECT)
PA5	PS	(PROCESSOR SWITCH)
PA6	PC_{LO}	(PROCESSOR SELECT)
PA7	PC_{HI}	

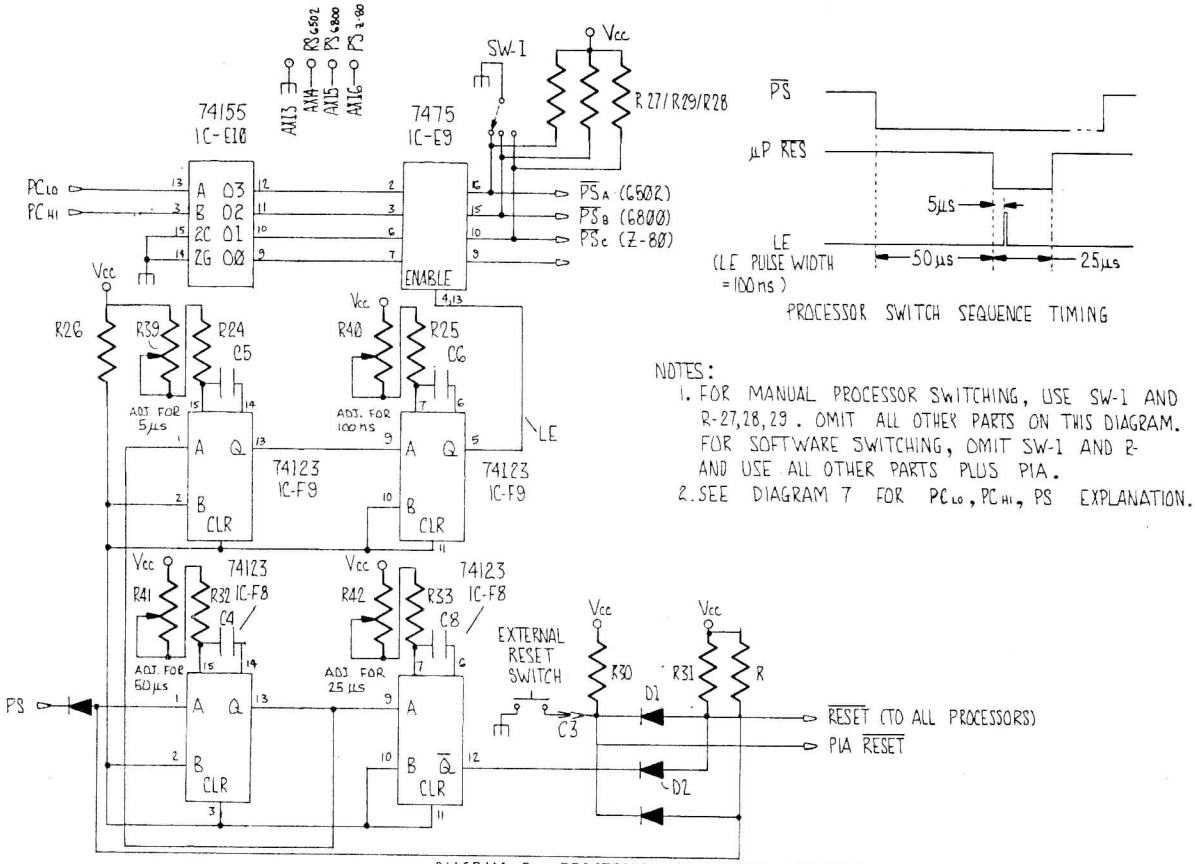
PROCESSOR SELECTION CHART

PC_{HI}	PC_{LO}	PROCESSOR
0	0	
0	1	Z-80
1	0	6800
1	1	6502

NOTES:

1. ALL PIA SIGNAL LINES ARE BI-DIRECTIONAL UNLESS OTHERWISE SHOWN.
2. PIA REGISTER 'PA' IS SHARED BY PORT AND CONTROL LINES. BOARD CONFIGURATION WILL DETERMINE THE FUNCTION OF THESE LINES.

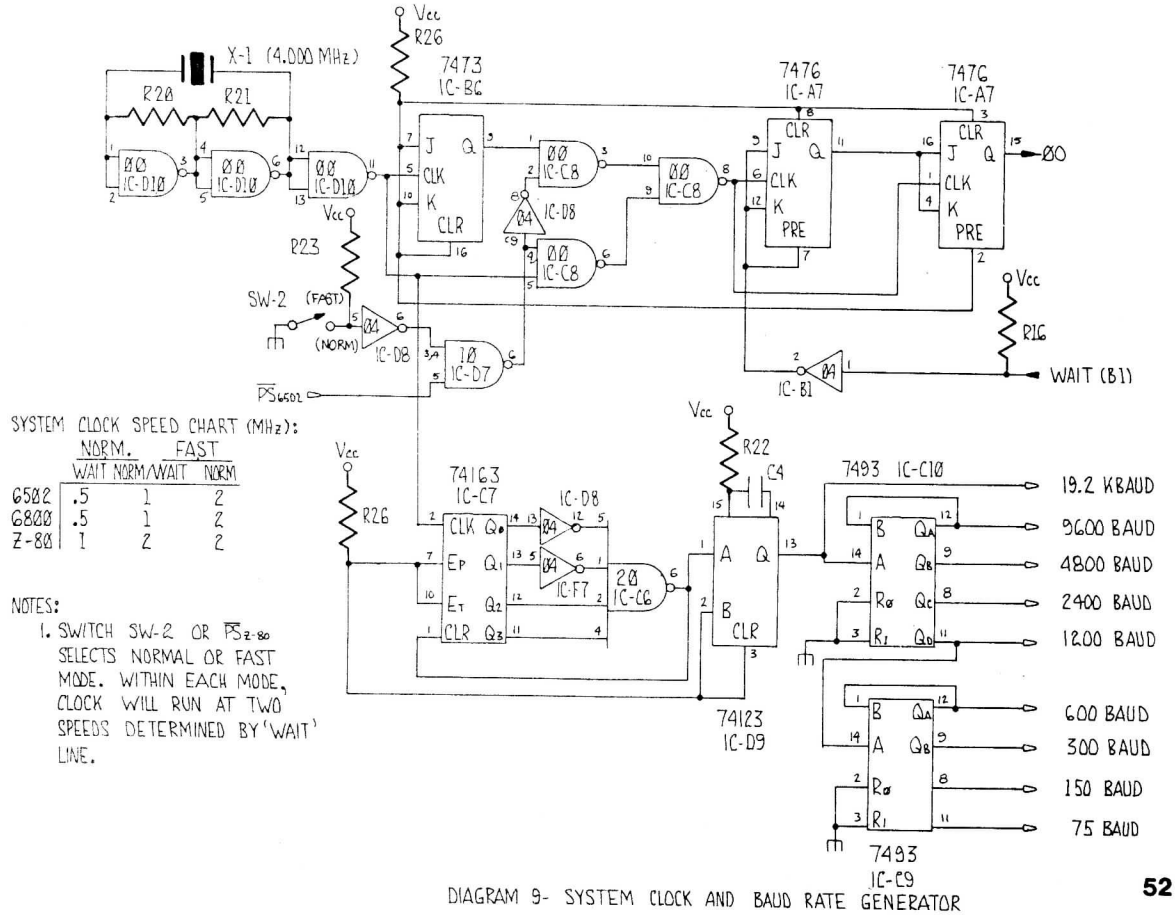
DIAGRAM 7- PIA IMPLEMENTATION



PROCESSOR SWITCH SEQUENCE TIMING

NOTES:
1. FOR MANUAL PROCESSOR SWITCHING, USE SW-1 AND R-27,28,29. OMIT ALL OTHER PARTS ON THIS DIAGRAM. FOR SOFTWARE SWITCHING, OMIT SW-1 AND R- AND USE ALL OTHER PARTS PLUS PIA.
2. SEE DIAGRAM 7 FOR PC_{LO}, PC_{HI}, PS EXPLANATION.

DIAGRAM 8- PROCESSOR SWITCHING CIRCUITRY



SYSTEM CLOCK SPEED CHART (MHz):

	NORM.		FAST	
	WAIT	NORM	WAIT	NORM
6502	.5	1	2	
6800	.5	1	2	
Z-80	1	2	2	

NOTES:
1. SWITCH SW-2 OR $\overline{PS}_{Z\text{-}80}$ SELECTS NORMAL OR FAST MODE. WITHIN EACH MODE, CLOCK WILL RUN AT TWO SPEEDS DETERMINED BY 'WAIT' LINE.

DIAGRAM 9- SYSTEM CLOCK AND BAUD RATE GENERATOR

Model 520
16K Static RAM

Description:

Model 520 16K RAM Board uses 4K x 8 EMM 4200 static RAM memories. These memories are ultra-low power, power-strobe chips. That is, they only draw appreciable amounts of power when they are being accessed. The Model 520 Memory Board requires power for both 12 Volt, 5 Volt, and -9 Volt supplies so that it cannot be used in 500-1 and Challenger IIP. The Model 520 Memory Board typically operates at a maximum of 1.5MHz with the 6502A or 6800 or approximately 3MHz with the Z-80.

Applications:

Main memory in medium to large scale computer systems (32 to 48K or more memory).

Specifications:

Available only as fully assembled, fully burned in memory board configured for 16K x 8 address strapable for any 16K partition within a 256K memory space. (18 address bits).

Electrical: Depend on access rate of the memory board but can be considered negligible in a stand-by condition.

Model 525
16K Dual Port RAM

Description:

The Model 525 16K Dual Port RAM Board utilizes 4K, 8K, or 16K of the popular 2114 static RAMs. The Model 525 can be configured for single or dual port operation. The second memory port allows memory transfers without processor paralyzing DMA.

Applications:

This board is a must in systems using the new 74 Megabyte disk, but, also has important applications in shared memory, multiprocessing, and high resolution video graphics where it is desirable to do memory transfers without interfering with processor performance.

Specifications:

Mechanical: 8" X 10" G-10 Dougle-Sided Plated Through Hole Board

Electrical: Power consumption is dependent upon the power type and speed type of the 2114 memories.

Other Features: Can be populated at 4K, 8K, or 16K with single or dual ports.

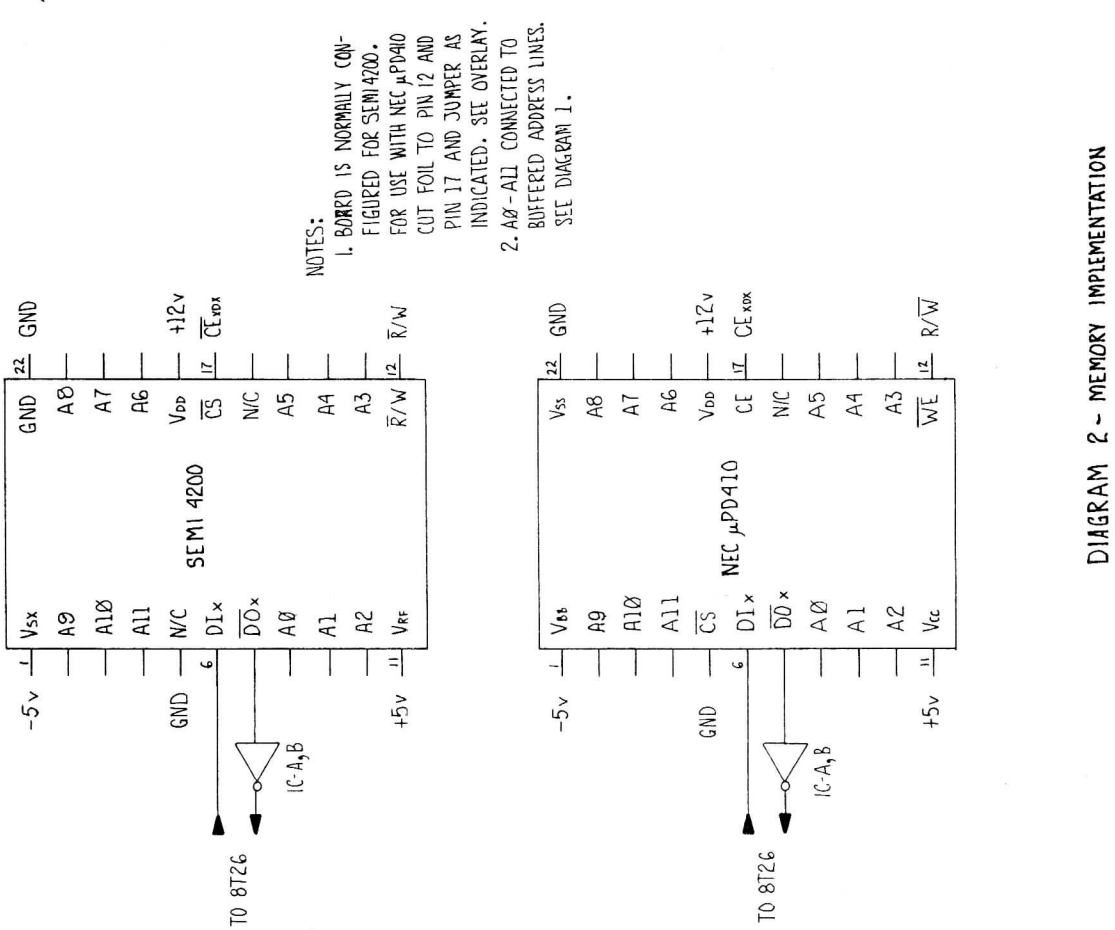


DIAGRAM 2 - MEMORY IMPLEMENTATION

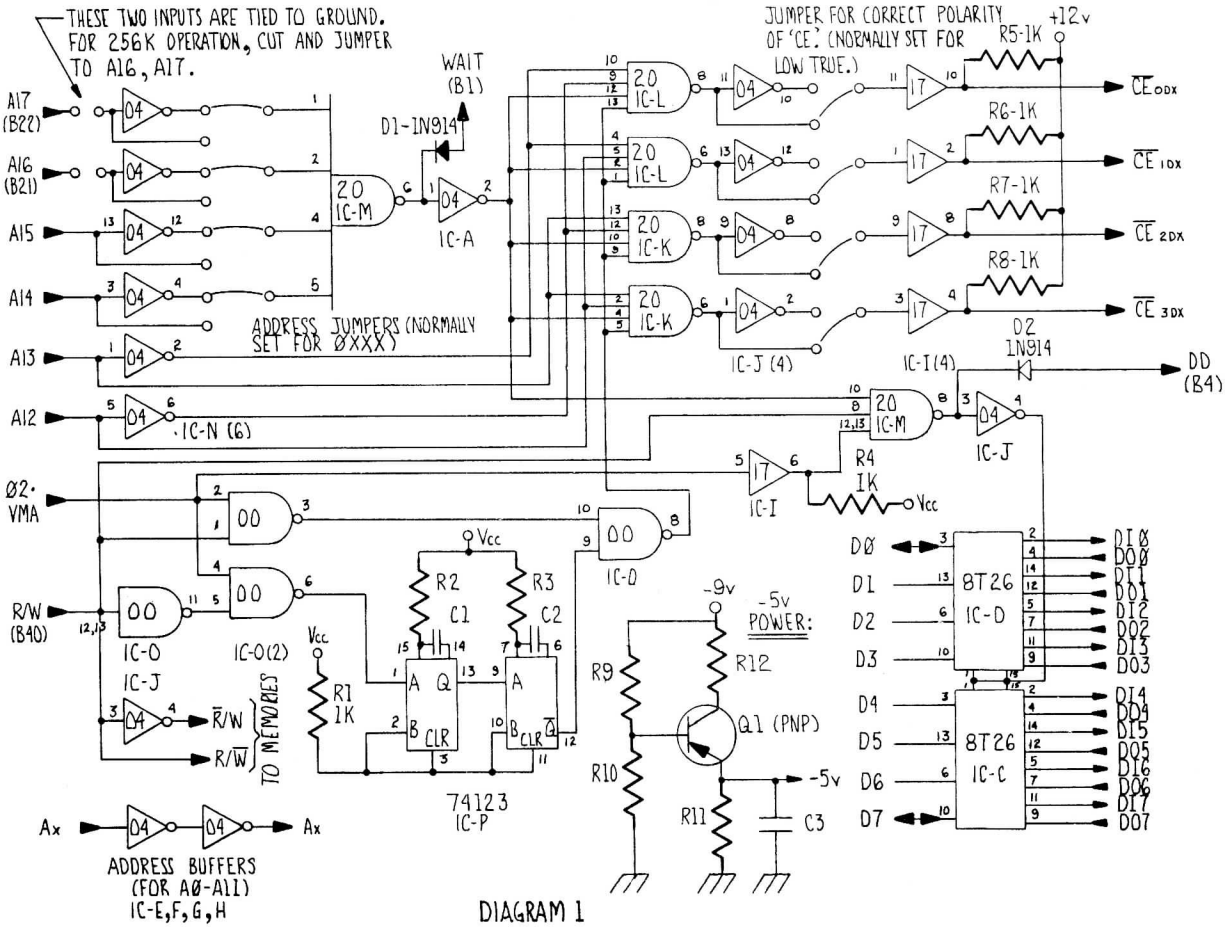
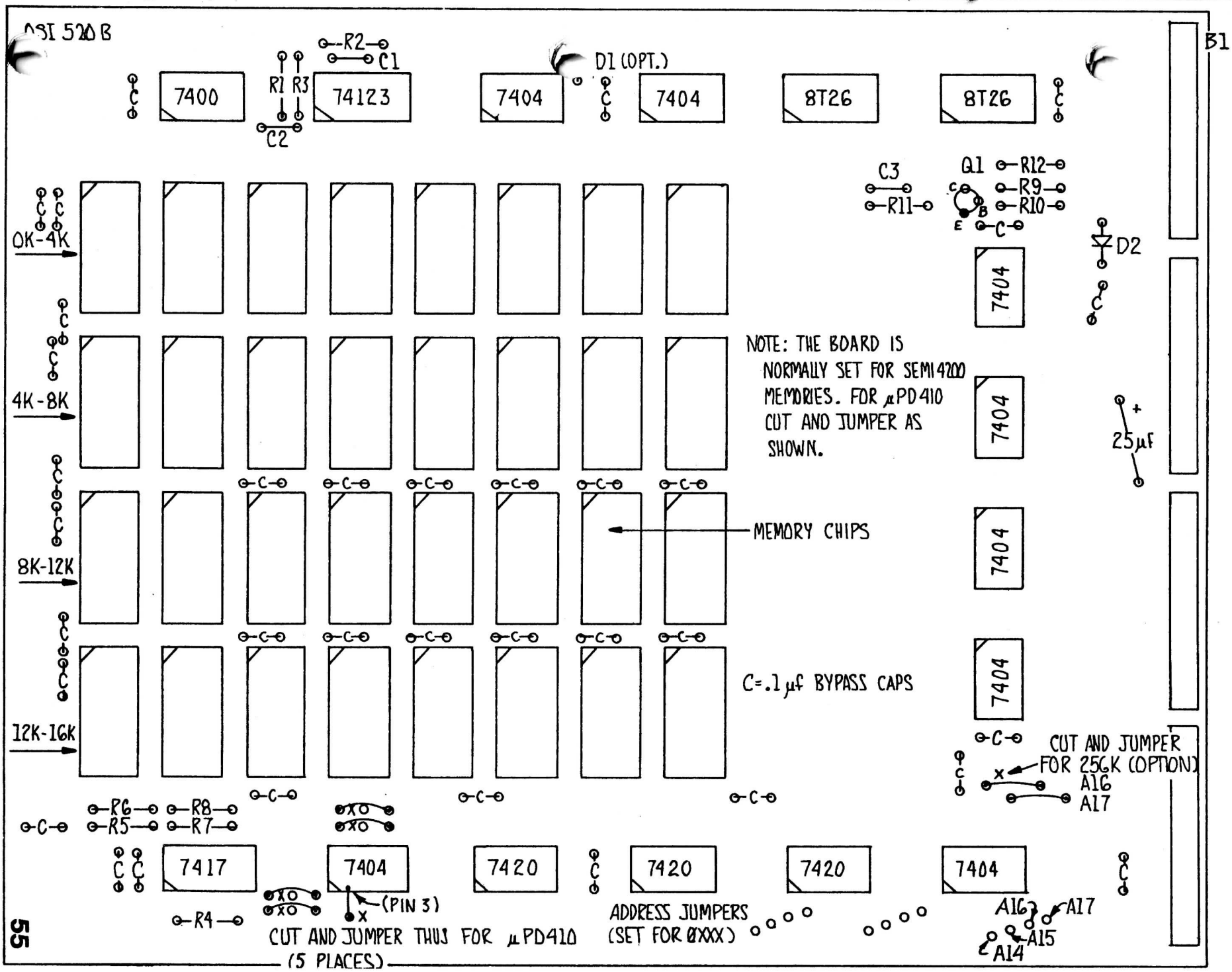


DIAGRAM 1


OSI 520 B
J1
7400
R1 R3
R2
C1
C2
74123
7404
D1 (OPT.)
7404
8T26
8T26
C3
R11
Q1
R12
R9
R10
D2
7404
0K-4K
4K-8K
8K-12K
12K-16K
NOTE: THE BOARD IS NORMALLY SET FOR SEMI 4200 MEMORIES. FOR μPD410 CUT AND JUMPER AS SHOWN.
25μf
MEMORY CHIPS
7404
7404
C=.1μf BYPASS CAPS
7404
CUT AND JUMPER FOR 256K (OPTION)
A16
A17
R6
R5
R8
R7
7417
7404
7420
7420
7420
7404
(PIN 3)
R4
CUT AND JUMPER THUS FOR μPD410 (5 PLACES)
ADDRESS JUMPERS (SET FOR 0XXX)
A16
A17
A15
A14
55

560Z CPU Expander Board

Description:

The 560Z CPU Expander is a "computer lab on a board." The 560Z supports Z-80 (8080 up-grade) and IM-6100 (PDP-8 compatible) microprocessors plus three-way bus switches and run/single step circuitry. The 560Z runs under the command of a 6502-based Ohio Scientific 400, 500, or 510 System.

Applications:

The 560Z can run standard PDP-8 and 8080 programs on an Ohio Scientific computer. It also has tremendous value as an educational aid in teaching about microprocessors since the host 6502 can single step the other two processors and read the status of each of their signal lines! The 560Z is a powerful research tool for investigations in multiprocessing and other computer architecture. The 560Z has provisions for a third microprocessor so new microprocessors can be evaluated under a complete operating system soon after their introduction.
Note: The 560Z is not for beginners. It is recommended that the potential 560Z user become intimately familiar with the 6502 system before attempting to utilize the 560Z.

Specifications:

Mechanical: 8" X 10" G-10 Double-Sided Plated Through Hole Board. 48-Pin System Bus on One Edge, 48 Pin Sub-Bus on Other Edge.

Electrical: +5V at 600ma

Supports: Z-80 and/or 6100 Microprocessors Plus Provisions for a Third Processor.

Hardware Requirements: System Bus Side: 400, 500 or 510 CPU with 6502 Processor and at Least 4K X 8 RAM
Sub Bus Side: 4K X 8 RAM for Z-80 Only, 4K X 12 RAM for 6100 Only or 6100 and Z-80

Mounting: The 560Z's Sub-Bus can support a full 65K of memory and I/O, but, it only occupies 4,512 bytes of the 6502 memory space via a sliding "port-hole." A 560Z and one dedicated memory can be mounted in slot 1 of the Challenger. If additional memory is required, an additional case will be required.

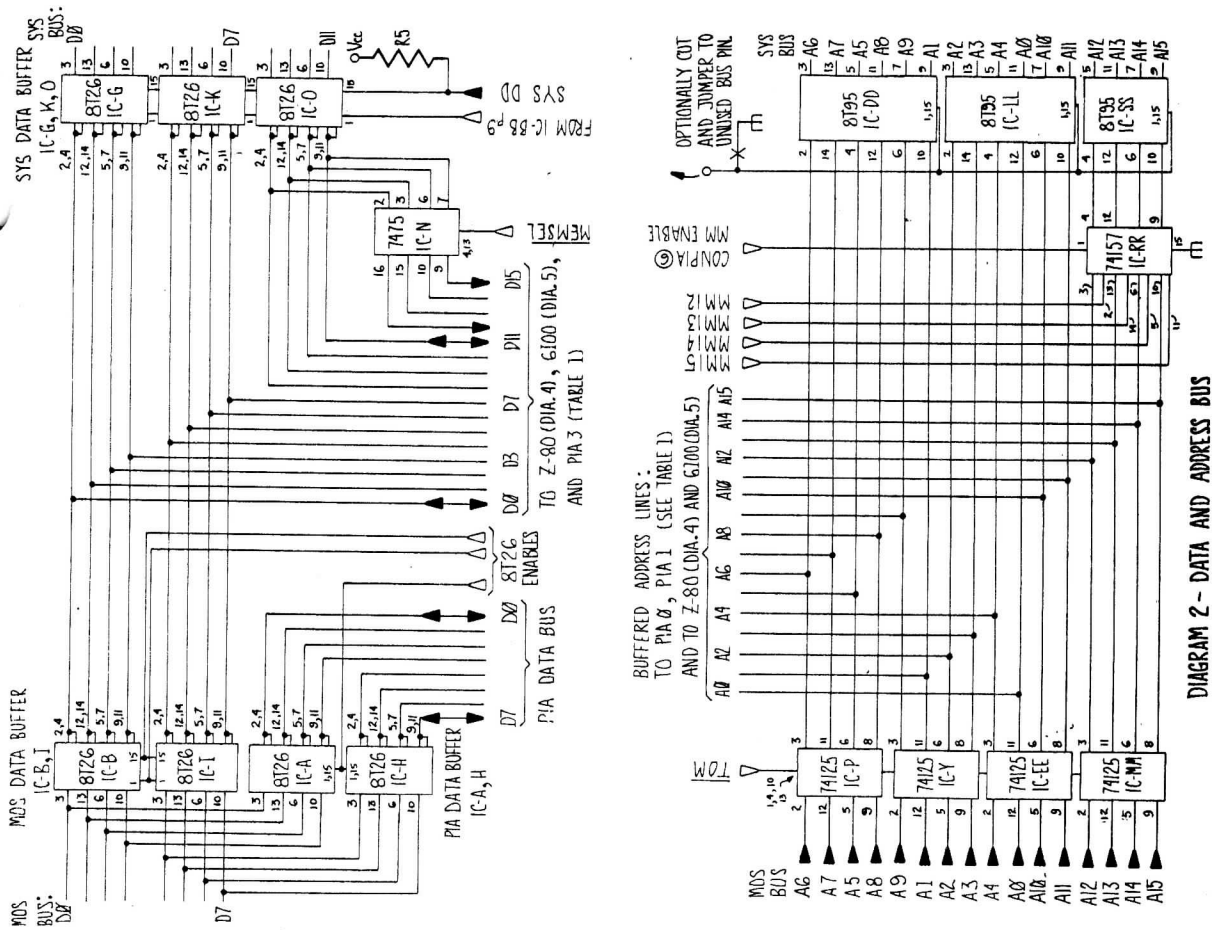
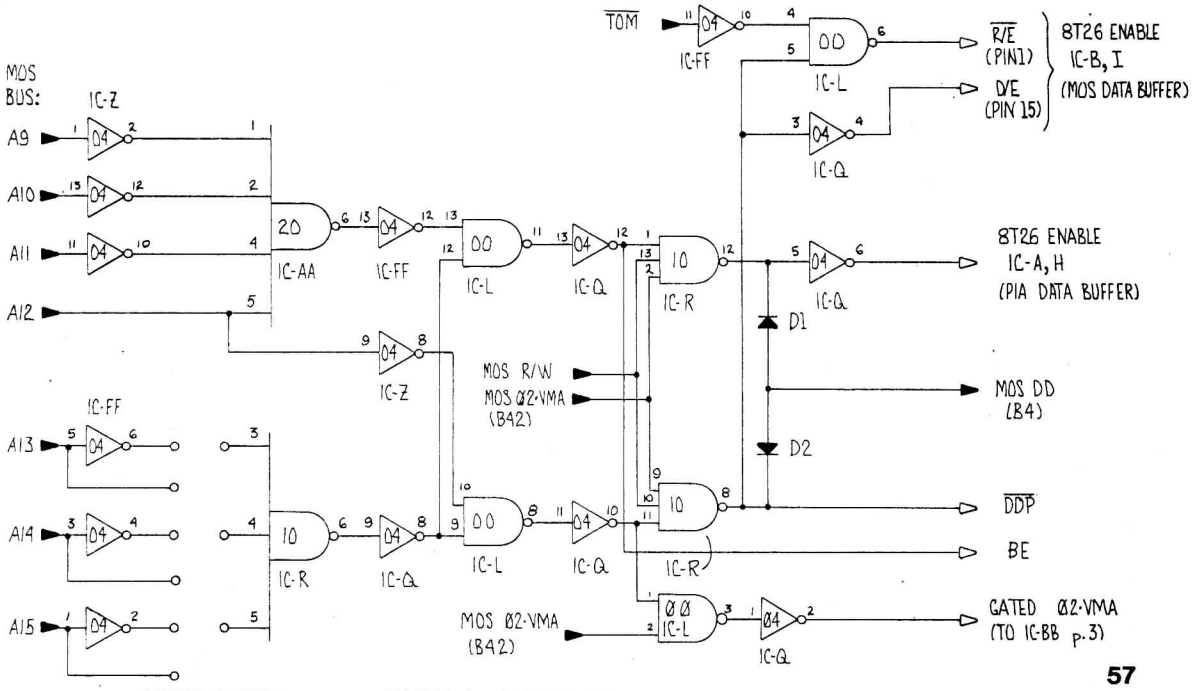


DIAGRAM 2 - DATA AND ADDRESS BUS



ADDRESS JUMPERS

DIAGRAM 1 - ADDRESS DECODE AND ENABLE CIRCUITRY

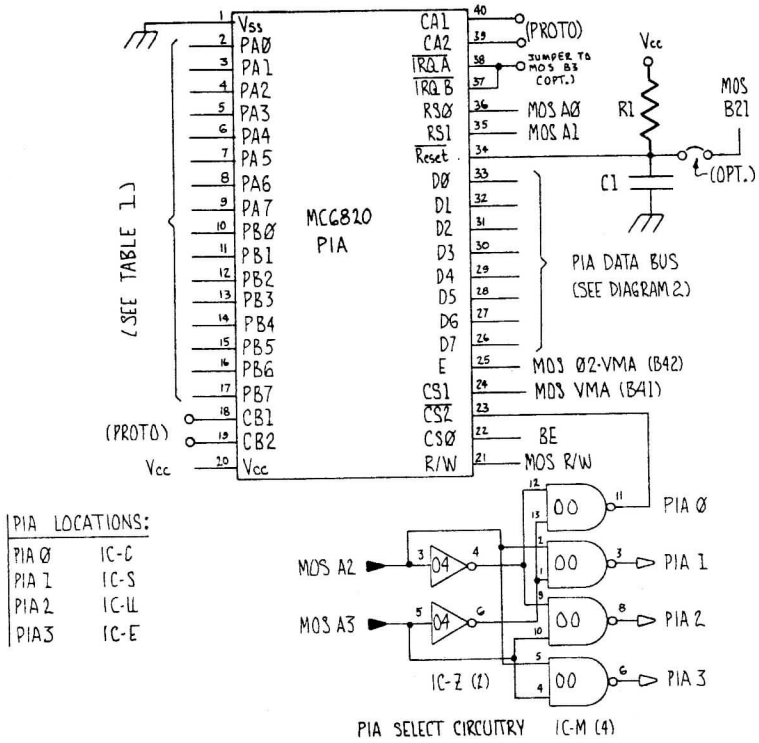


DIAGRAM 3 - PIA IMPLEMENTATION

	PIAØ IC-C	PIA1 IC-S	PIA2 IC-U	PIA3 IC-E
PAØ	AØ	A8	$\overline{WR}$ p.22	DA8
PA1	A1	A9	$\overline{MREQ}$ p.19	DA9
PA2	A2	A10	DATAF p.40	DA1Ø
PA3	A3	A11	$\overline{CPSEL}$ p.38	DA11
PA4	A4	A12	$\overline{MEMSEL}$ p.37	DA12
PA5	A5	A13	IFETCH p.36	DA13
PA6	A6	A14	$\overline{RESET}$ p.7	DA14
PA7	A7	A15	$\overline{SKP}$ p.35	DA15
PBØ	Z-80 $\overline{RFSH}$ p.10	DØ	$\overline{INTREQ}$	*PROCESSOR SELECT
PB1	Z-80 $\overline{INT}$ p.11	D1	$\overline{C_2}$	*PROCESSOR SELECT
PB2	Z-80 $\overline{IORQ}$ p.12	D2	$\overline{C_1}$	CLOCK MODE SELECT (RUN/$\overline{STEP}$)
PB3	MM STROBE	D3	$\overline{CØ}$	6100 $\overline{RUN/HALT}$
PB4	MM12	D4	LXMAR	STEP
PB5	MM13	D5	$\overline{SWSEL}$	$\overline{M_1}$ p.27
PB6	MM14	D6	XTC	$\overline{RESET}$ p.26
PB7	MM15	D7	$\overline{DEVSEL}$	$\overline{BUSAK}$ p.23

*See Selection Table, Diagram 6.

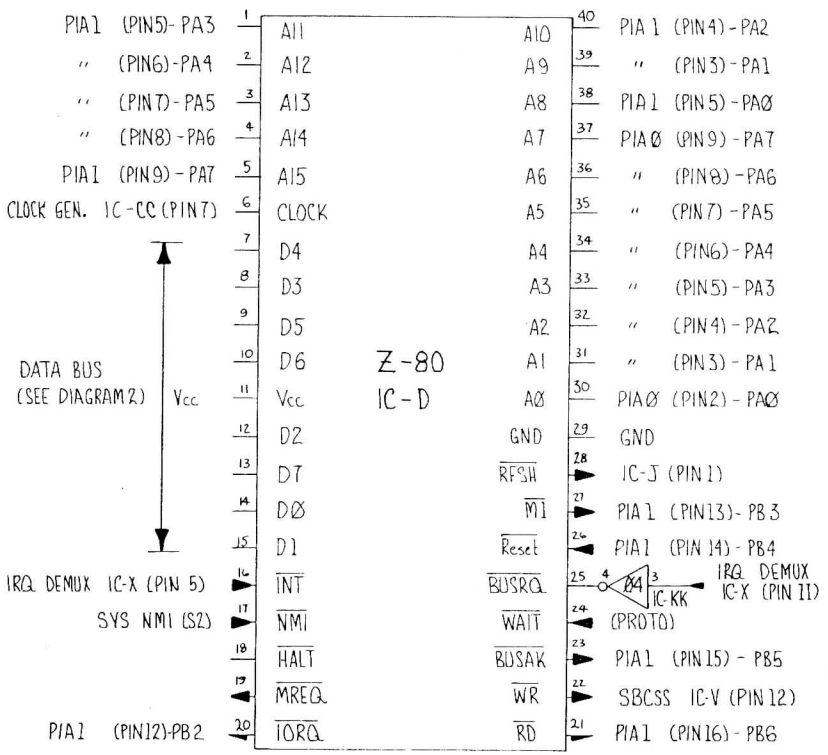
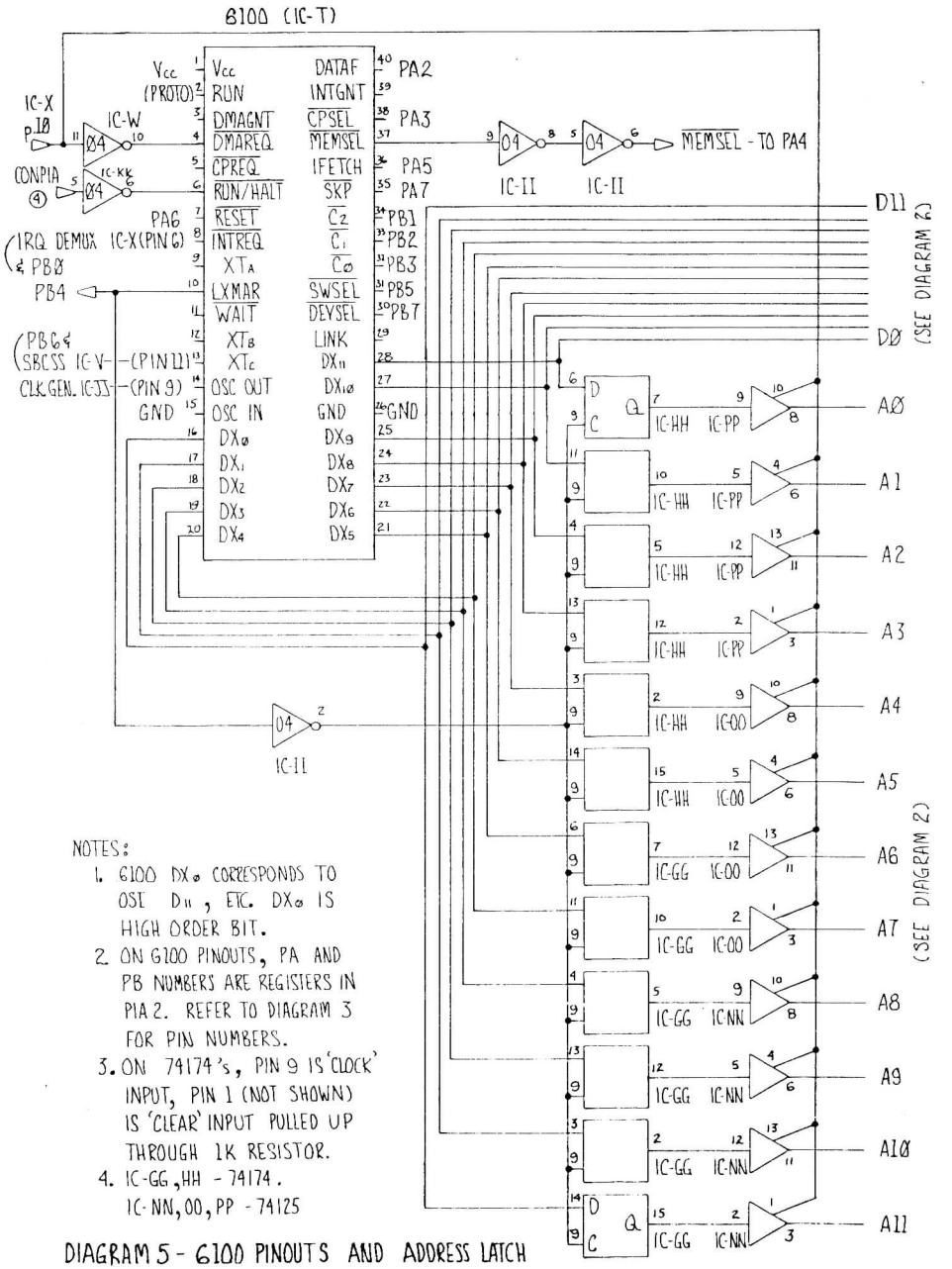


DIAGRAM 4- Z-80 PINOUTS



NOTES:
1. 6100 DXØ CORRESPONDS TO OSI D11, ETC. DXØ IS HIGH ORDER BIT.
2. ON 6100 PINOUTS, PA AND PB NUMBERS ARE REGISTERS IN PIA 2. REFER TO DIAGRAM 3 FOR PIN NUMBERS.
3. ON 74174's, PIN 9 IS 'CLOCK' INPUT, PIN 1 (NOT SHOWN) IS 'CLEAR' INPUT PULLED UP THROUGH 1K RESISTOR.
4. IC-GG, HH - 74174. IC-NN, OO, PP - 74125

DIAGRAM 5- 6100 PINOUTS AND ADDRESS LATCH

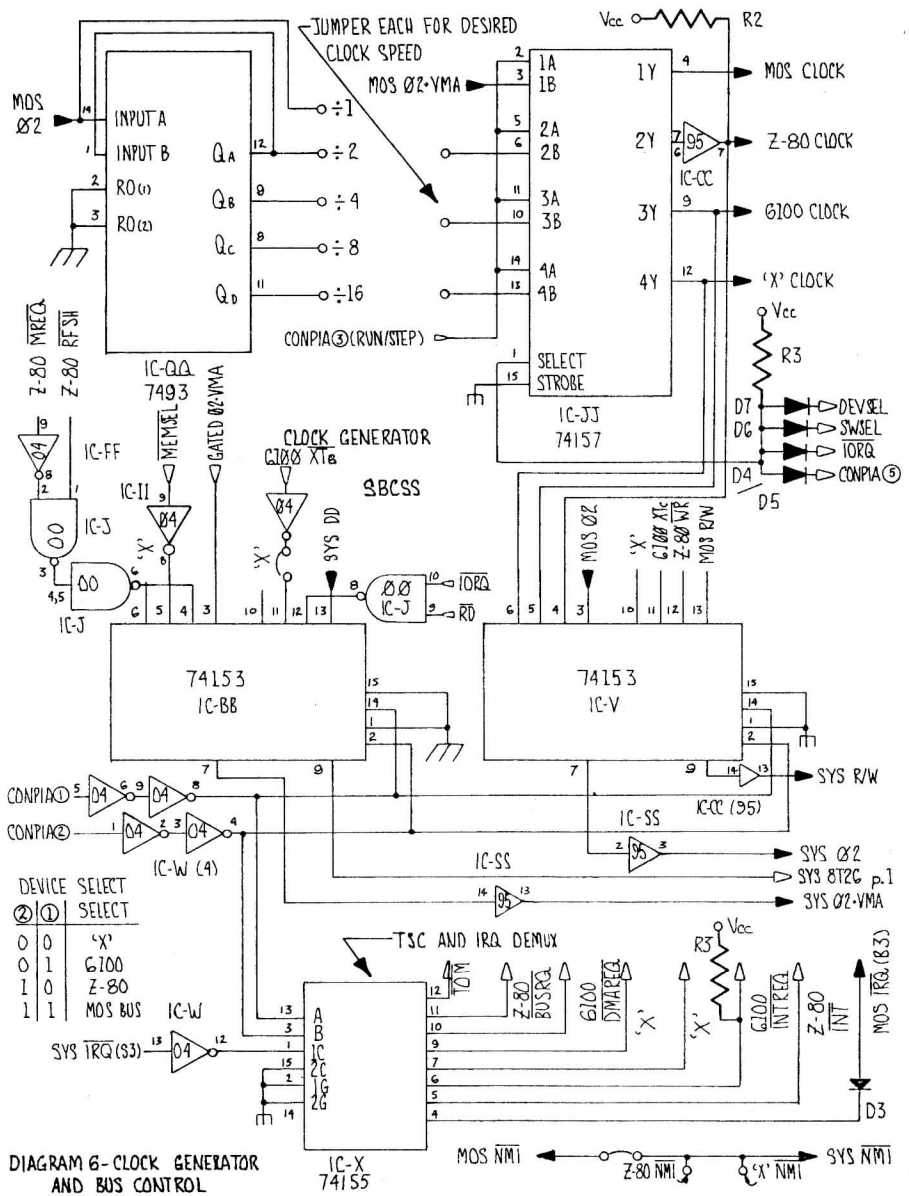
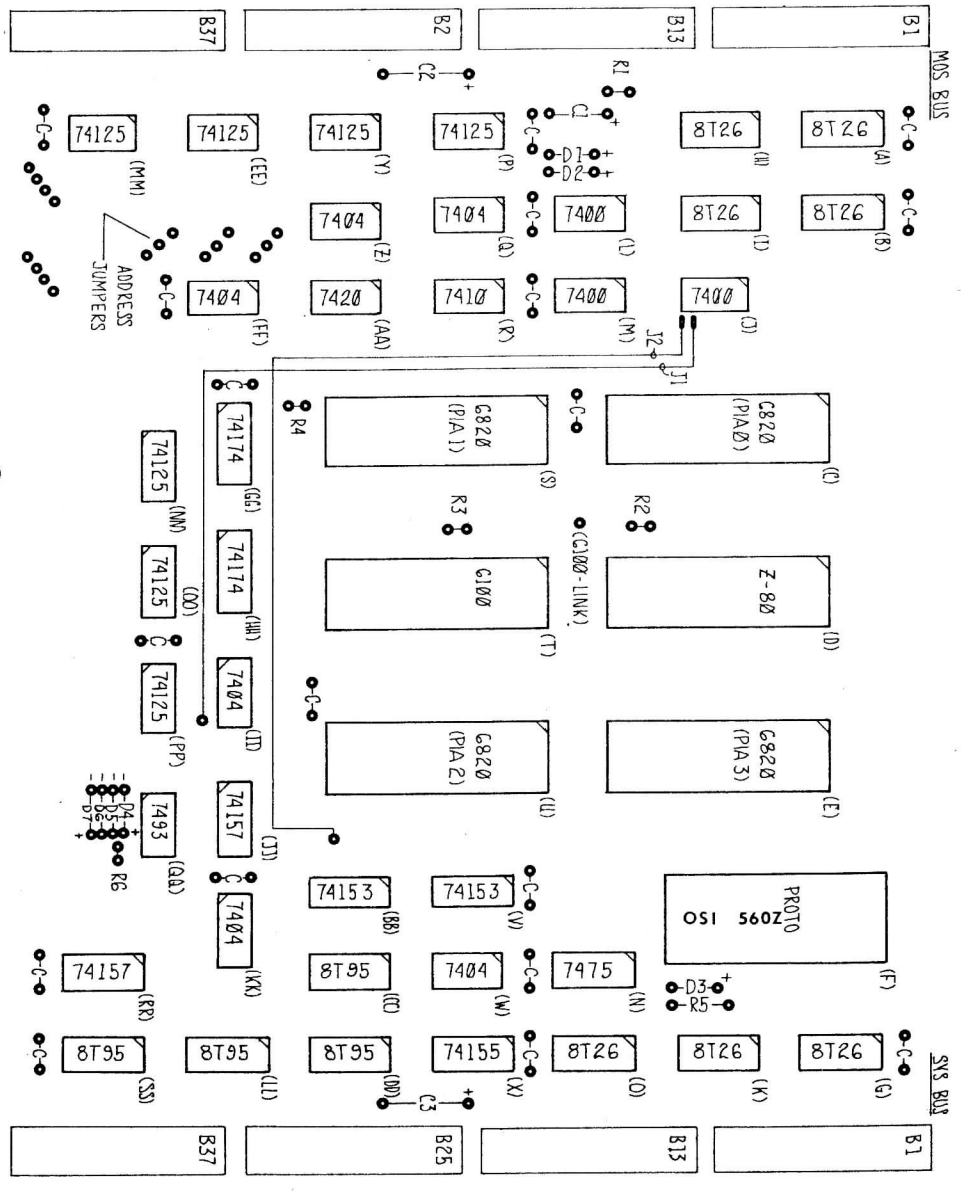


DIAGRAM 6- CLOCK GENERATOR AND BUS CONTROL



400 CPU

Description:

The OSI 400 CPU Board is the heart of any OSI 400 or Challenger System. It minimally contains the microprocessor chip, the system PROM monitor, and bus drivers. It can maximally be configured as a complete stand-alone computer with two PROMs, 1,024 words of RAM, a serial I/O port, and a parallel I/O port and still maintain full system expansion capability. The minimized address logic and Schottky data buffering allow ultra-high speed operation.

Applications:

The OSI 400 can be used as a complete, stand-alone computer in conjunction with a serial terminal and power supply. It is used as the CPU in any OSI 400 or Challenger system. An OSI 400 and 440 board can be populated as a complete computer and CRT terminal!

Specifications:

Mechanical: 8" X 10" G-10 Double Sided Plated Through Hole Board

Electrical: +5V at 800 ma Maximum
-9V at 100 ma Maximum

Processors: Supports any one of the following: MOS Technology 6502, 6502A, 6501, or 6512, Motorola 6800, 6800A, 6802, 6802B

PROM: Supports up to two of the following: OSI 65A Serial Monitor, OSI 65V Video Monitor, OSI 65F Floppy Disk Bootstrap.

RAM: Optional 1K by 8 of 2102 type parts.

Serial I/O: ACIA based 20 ma loop or RS-232
Up to 100,000 baud

Parallel I/O: Supports one of the following PIA type devices for 16 parallel I/O lines: 6820, 6520, 6522, 6530, 6830

Other Features: Buffering to drive up to 250 OSI system boards
Provisions for user supplied front panel and DMA capability

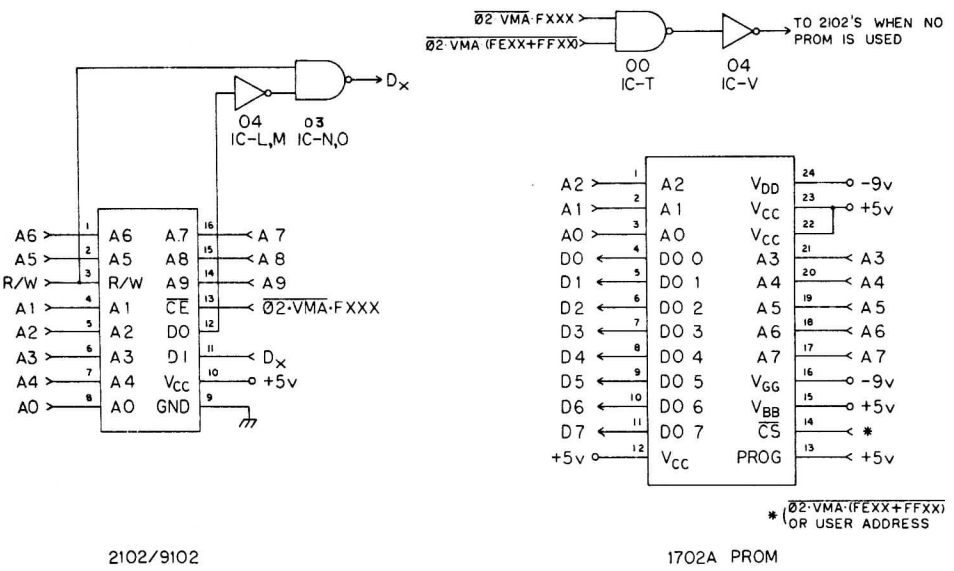


DIAGRAM 2- RAM/PROM IMPLEMENTATION

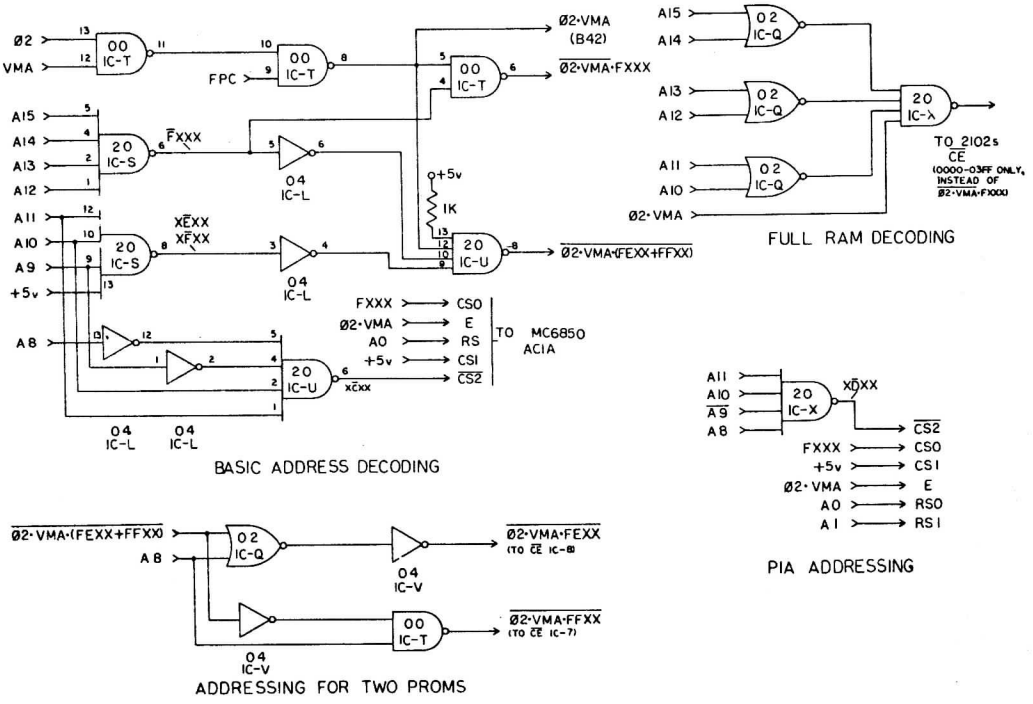
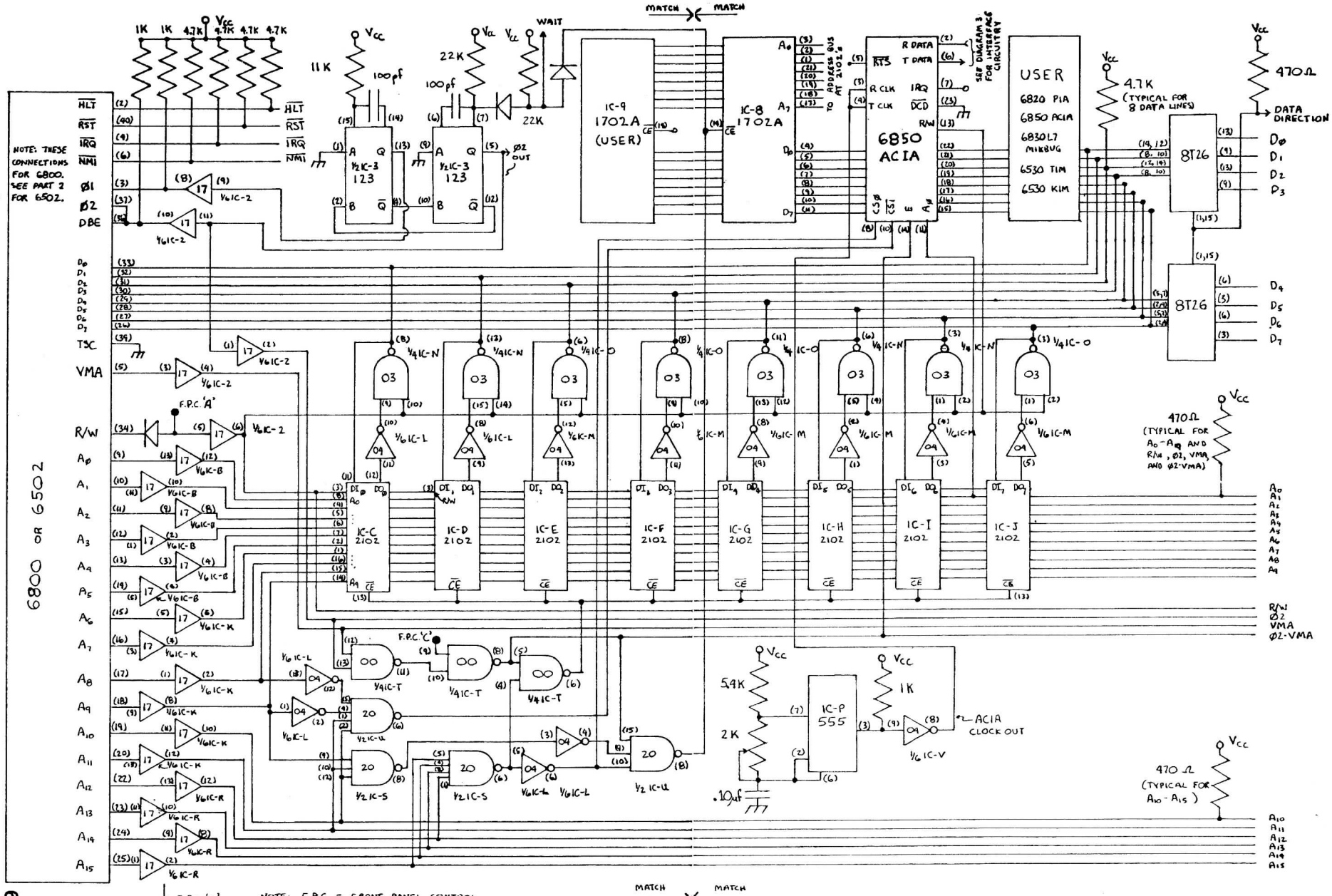


DIAGRAM 1


6800 OR 6502
NOTE: THESE CONNECTIONS FOR 6800. SEE PART 2 FOR 6502.
HLT
RST
IRQ
NMI
ØI
Ø2
DBE
TSC
VMA
R/W
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7
1K
4.7K
Vcc
11K
22K
100pf
WAIT
MATCH
1/2IC-3 123
IC-9 1702A (USER)
IC-8 1702A
6850 ACIA
USER
6820 PIA
6850 ACIA
6830L7 MIKBUG
6530 TIM
6530 KIM
4.7K (TYPICAL FOR 8 DATA LINES)
470Ω
DATA DIRECTION
8T26
IC-C 2102
IC-D 2102
IC-E 2102
IC-F 2102
IC-G 2102
IC-H 2102
IC-I 2102
IC-J 2102
F.P.C. 'A'
F.P.C. 'B'
F.P.C. 'C'
5.9K
2K
.10μf
IC-P 555
ACIA CLOCK OUT
470Ω (TYPICAL FOR A0-A8 AND R/W, Ø2, VMA AND Ø2·VMA)
470Ω (TYPICAL FOR A10-A15)
NOTE: F.P.C. = FRONT PANEL CONTROL. SOME POWER AND GROUND CONNECTIONS NOT SHOWN.

OHIO SCIENTIFIC
11681 Hayden St Hiram, OH 44234

Comprehensive Information Package II