OPERATION AND MAINTENANCE MANUAL

for

3300 SERIES DISC DRIVES

Manufactured by

OHIO SCIENTIFIC MEMORY PRODUCTS, INC.
5740 Thornwood Drive
Goleta, California 93117

(805) 964-3535

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INTRODUCTION

This manual describes the 3300 Series of Disc Drives, manufactured by Ohio Scientific Memory Products, Inc., 5740 Thornwood Drive, Goleta, California 93117.

The manual describes installation, operation, interfacing, and maintenance of the 3300 Series of Disc Drives. This information is contained in the first five sections of the manual; Section Six contains schematic diagrams, assembly drawings, and a list of replaceable parts.
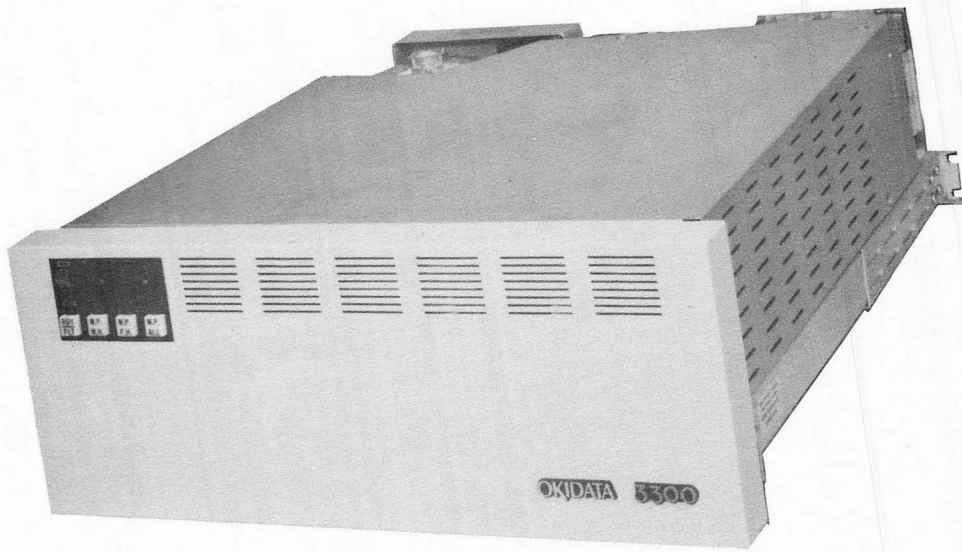
3300 FRONT VIEW
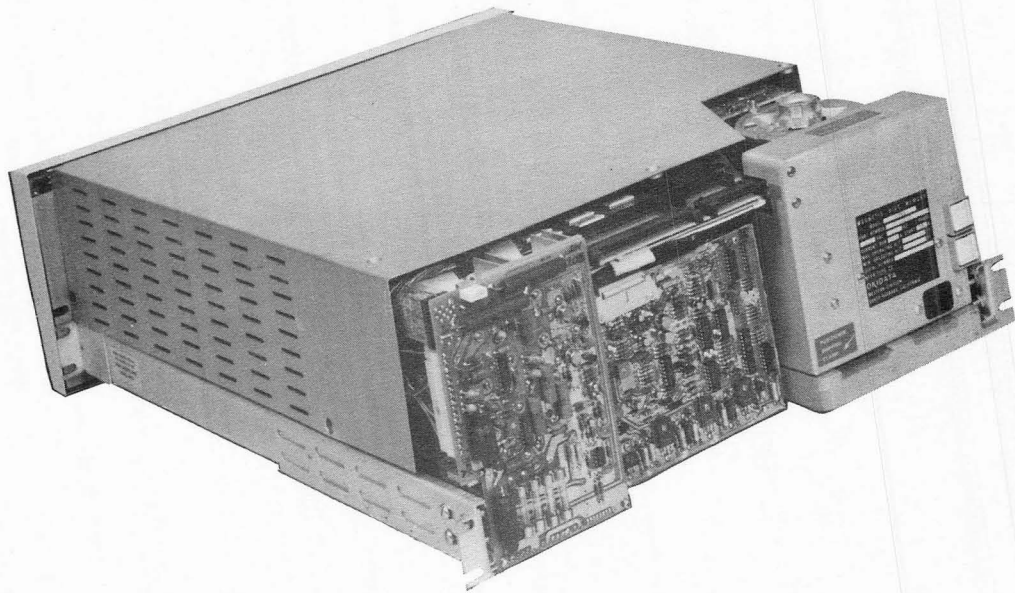
3300 REAR VIEW

SECTION I

GENERAL DESCRIPTION

1.1 GENERAL INFORMATION

The   Model 3300 Series is a family of disc
drives which is intended to fill the memory needs of
a large variety of minicomputer and medium-scale
computer systems. The basic drive mechanism can be
configured with one, two, three or four non-removable
discs. Up to six surfaces can be used for data accessed
by moving head(s), one surface being required for servo
information. In addition, fixed heads may be included
to provide data storage with minimum access time.

Unformatted capacities range from:

    a) 13.47 to 80.80 Mbyte, moving head.

    b) 0.40 to 2.42 Mbyte, fixed head in increments
       of 0.40 Mbyte when added to a moving head
       spindle.

    c) 0.80 to 3.22 Mbyte, fixed head, in increments
       of 0.40 Mbyte fixed head only.

The seven basic models of the 3300 family and the
maximum fixed and/or moving head capacities are shown
in Table 1. The disc and head arrangement for each of
these models is shown schematically in Table 1-2.

1.2 TECHNOLOGY

The heads and discs used in the 3300 are equivalent to
those used in the most advanced, yet field-proven IBM
drives, the 3340. To guarantee reliability, every effort
has been made to utilize the heads and discs in the same
manner as in the 3340. Therefore spindle speeds, bit
density, and track density have been made similar to the
3340 drives. This is true also for the optional fixed
heads.

    Disc rotational speed RPM   2964

    Track density fixed heads (tracks/in) 33.3

    Track density moving heads (tracks/in) 286

    Bit density (inner track) bits/in   6122 approx.

TABLE 1

AVAILABLE CONFIGURATIONS
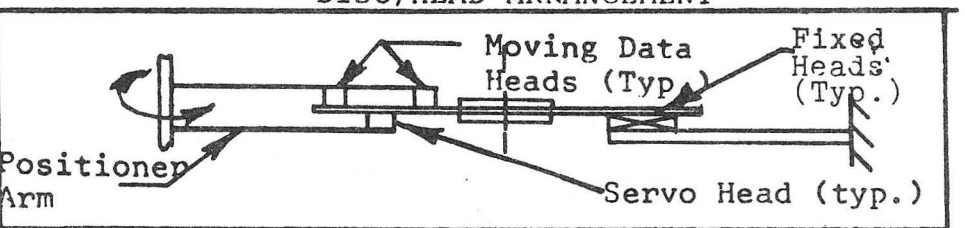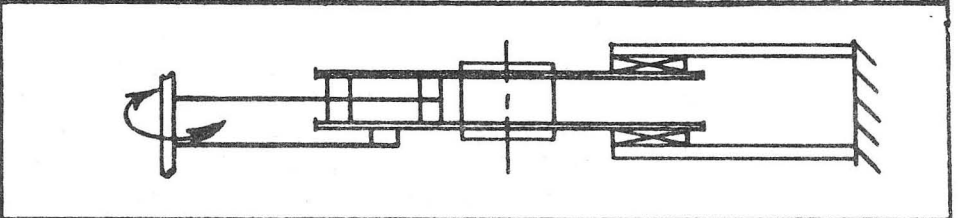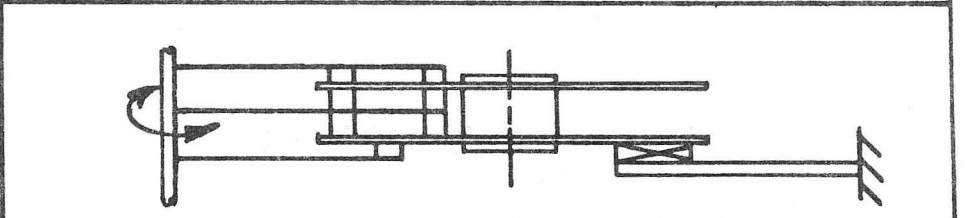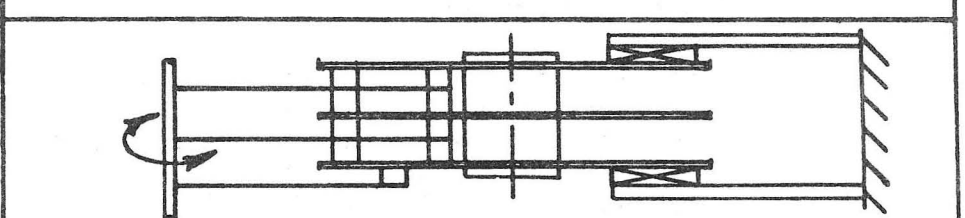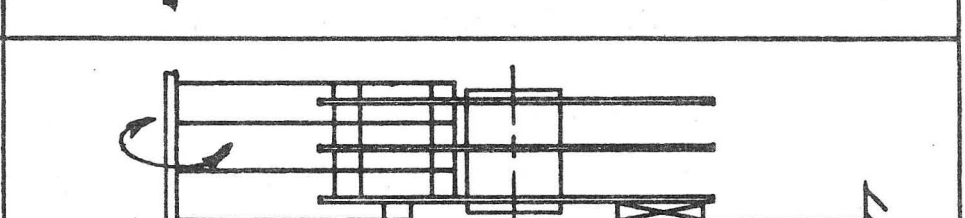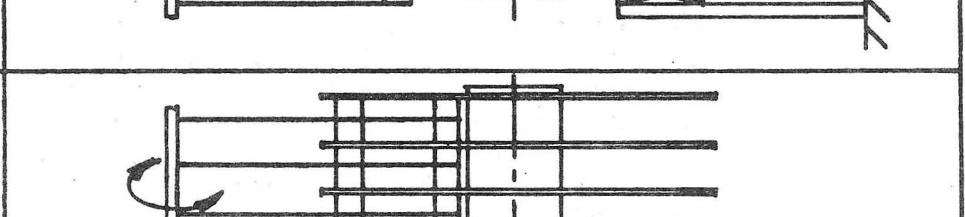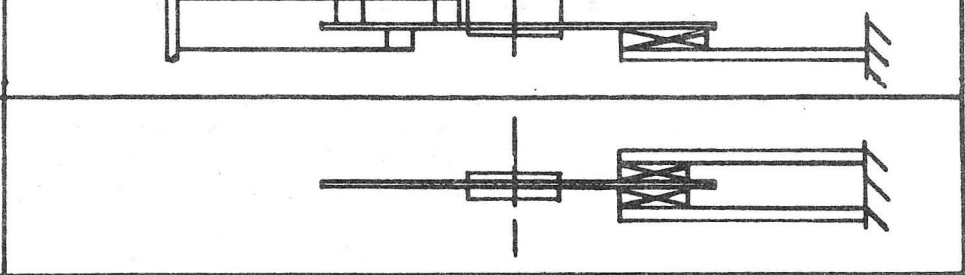
Number of Discs	Model Number	CAPACITY Max. Fixed Head Option Unformatted Megabits	Unformatted Megabytes	Moving Head Unformatted Megabytes	Remarks
1	3301	6.45	0.80	13.47	1 surface Moving Head
2	3302	19.35	2.42	26.94	2 surfaces Moving Head
2	3303	6.45	0.80	40.39	3 surfaces Moving Head
3	3304	19.35	2.42	53.86	4 surfaces Moving Head
3	3305	6.45	0.80	67.33	5 surfaces Moving Head
4	3306	6.45	0.80	80.80	6 surfaces Moving Head Max. Capacity
1	3307	25.81	3.22		1 platter Fixed Head only

NOTES: Moving head capacities are a minimum useable with a maximum number of defective tracks.

Fixed head capacities are a minimum useable. One spare addressable track is provided for each group of 20 tracks; however, it may be defective.

All moving head machines have 339 addressable cylinders with two data heads per data surface.

TABLE 1-2 - CONFIGURATIONS

MODEL NUMBER	DISC/HEAD ARRANGEMENT
3301	
3302	
3303	
3304	
3305	
3306	
3307	

Like IBM's System 32 (which also uses 3340 heads and discs), the 3300 uses a simple, reliable rotary positioner. Like the 3340, the 3300 uses a track following servo and does not require a tachometer. A portion of the lower disc surface contains pre-recorded information allowing for servo positioning directly off the discs, eliminating most temperature and initial adjustment problems associated with high track density recording. Also like the System 32, the discs are contained in a sealed enclosure which allows for recirculation of clean air through an absolute filter.

1.3   DESCRIPTION OF COMPONENTS

DISC ENCLOSURE

The discs, moving heads, fixed heads, and positioner arm are contained in a factory sealed enclosure. This feature, coupled with a recirculating filtration system, results in a clean air environment which virtually eliminates head/disc failures. Components within the enclosure cannot be maintained in the field.

CLEAN AIR PACKAGE

Consisting of a blower, main filter, and breather filter, the clean air system is designed to pass 29 CFM of already clean air through the main filter which is able to stop 99.97% of all particles larger than 0.3 micron in diameter. This results in the clean air in the enclosure being recirculated through the filter up to 60 times per minute. The blower also serves to provide a slight positive pressure to the enclosure so that any small leaks do not result in the intake of contaminated air.

The function of the breather filter is to allow the system to achieve pressure equilibrium regardless of altitude or temperature change without resulting in a negative pressure in the disc enclosure.

The blower spindle and breather filter can be replaced in the field without contaminating the enclosure. The main filter should never need to be replaced.

DECK AND SPINDLE

A rigid, cast aluminum deck is used to mount the disc spindle and positioner motor providing a stiff, dimensionally stable coupling of these two elements without unnecessary bulk or weight.

SPINDLE BRAKE

A brake band is located directly on the disc spindle pulley providing smooth yet rapid deceleration of the disc without creating undue stress on the spindle drive belt.

SPINDLE MOTOR

A capacitor start induction motor is used to achieve rapid yet smooth acceleration of the disc.

AC DISTRIBUTION

Contains spindle motor start components, line filter, and AC fuses.

POWER SUPPLY

All DC power is generated internally. All elements are mounted on a single base plate for easy removal.

HEAT SINK ASSEMBLY

Contains positioner power amplifier and +5 V, -5.2 V and -2 V regulators. An easily removable fan provides cooling for the heat sink and printed circuit boards on top of the unit.

PRINTED CIRCUIT BOARDS

All printed circuit boards are mounted such that components and test points are immediately accessible. These boards perform the following functions:

Matrix: Moving head preamps and switching.

Data: Encoding, decoding and clocking of moving and fixed head data.

Servo/Logic: Derives position servo information and controls machine functions.

Interface: Contains receivers and drivers and gates I/O lines, plus customer options.

Fixed Head Amplifier: Contains fixed head preamps and switching (optional).

Power Amplifier: Contains positioner power amplifier and +5 V, -5.2 V and -2 V regulators.

CONTROL PANEL

Contains operator controls.

FIXED HEAD MODULE

Fixed heads are mounted with diodes on a modular plate in groups of 21 heads each up to 84 heads per module. No electronics is contained within the disc enclosure. One head in each group of 21 is a spare and may be defective.

POSITIONER MOTOR

Heads are moved from track to track by an arm connected directly to the positioner motor shaft. The positioner motor can be removed from the drive without contaminating the disc enclosure.

INTERFACE CONNECTORS

HEAT SINK
ASSEMBLY

SPINDLE MOTOR

INTERFACE PCB

BREATHER FILTER
(UNDER PCB)

FIXED HEAD
AMP. PCB

SERVO/LOGIC PCB

DATA PCB

CONTROL PANEL

INTERFACE
CONNECTORS

AC DISTRIBUTION
ASSEMBLY

AC FUSE

FIXED HEAD AMPLIFIER PCB

POWER
AMPLIFIER PCB

MATRIX PCB

LINE POWER
CONNECTOR

SPINDLE SHIPPING
CLAMP IN STORAGE POSITION

SPINDLE BRAKE SOLENOID

AC VOLTAGE PLUG

POSITIONER MOTOR

POWER SUPPLY
ASSEMBLY

HEAT SINK FAN

SPINDLE PULLEY
AND BRAKE

POSITIONER
SHIPPING CLAMP

HOLE FOR SHIPPING
CLAMP HARDWARE
STORAGE

DECK CASTING

AIR FILTER

INDEX TRANSDUCER

AIR BLOWER

1.4   SPECIFICATIONS

Capacity Ranges	See Table of Available Configurations
Capacity per Track (Unformatted)	20160 Bytes
Addressable Cylinders	339
Heads and Media	IBM (3340) Equivalent
Bit Density (BPI)	6122 Approximately
Track Density (Moving Head) (TPI)	286
Data Tracks per Surface (Moving Head)	678
Track Density (Fixed Head) (TPI)	33.3
Maximum Data Tracks per Surface (Fixed Head)	80
Average Moving Head Position Time (Msec)	38
Maximum Seek (Msec)	75
Single Track Seek (Msec)	10
Average Latency (Msec)	10.12
RPM (Nominal)	2964
Transfer Rate (Megabits/Sec)	7.97
Head Positioner Type	Rotary Motor
Positioner Servo	Track Follow from Dedicated Surface Area
Error Rate (Recoverable)	10^{10} Bits - No Retries or Error Correction
Error Rate (Hard)	10^{13} Bits

Size (Height - Inches x Depth from Mounting Surface - Inches)	7 x 22, 19" Retma Rack Mount
Mounting	Horizontal or Vertical on slides
Weight (Lbs.)	70 Maximum
Air Filtration	0.3 Micron (Absolute Filter) Forced Air - Recirculating @ 29 CFM
Operating Temperature (°C)	10 to 40
Operating Humidity (% R.H.)	20 to 80% (No Condensation)
Power Supply	Built-In Taps for Common Voltages (Pulley Selection Required on Spindle Motor for 50/60 Hz). Spindle Motor Selection Required for 112/225 V.

1.5   OPTIONS

A wide selection of options are available to make the
3300 completely compatible with a wide variety of
system requirements. All options except the number of
fixed heads are field upgradeable, most by plug-ins
in the I/O Board.

1.5.1   FIXED HEADS

Fixed heads can be added to moving head models
in groups of 20 heads each up to a maximum
capacity as shown in Table 1. Fixed heads can
be used in an "overlap seek" mode. (See 3.4)

1.5.2   CONTIGOUS FIXED HEAD ADDRESSING

A PROM can be provided to make all fixed heads
addressable by a contigous set of binary
numbers.

1.5.3   VARIABLE SECTORING (ADDRESS MARK)

Read and write address marks can be provided.

1.5.4   WRITE PROTECT

A portion of moving head data, all fixed head
data, or the entire drive can be protected from
writing with control panel switches.

1.5.5   CDC-9762 COMPATIBLE INTERFACE

The 3300 can be made compatible with the flat
cable version of the CDC-9762 (Storage Module)

1.5.6   CHOICE OF TRACK CAPACITY

The number of data bytes per revolution can be
varied somewhat to accomodate unique user formats
and sector data fields without waste of capacity.

1.5.7   UNIT SELECT SWITCHES

Unit select thumbwheel switches can be provided
on the control panel.

SECTION II

INSTALLATION

2.1   INSTALLATION PLANNING

2.2   EQUIPMENT LOCATION

The 3300 Series Disc Drive may be located adjacent
to any other electronic data processing equipment
provided the temperature, humidity, and other envi-
ronmental characteristics are within the limits
specified in Table 1-3. The equipment should not
be located in a strong magnetic field, because the
head assemblies and other components may become
magnetized and, thus, interfere with the read/write
process.

To obtain optimum performance from the equipment,
the ambient temperature fluctuation should be kept
as small as possible and a reasonably clean and
dust free environment should be provided. It is
also important that a free flow of air is allowed
around the equipment and through the rack in which
it is mounted.

The Disc Drive should be mounted in a standard 19-
inch wide rack cabinet and located on a firm, vibra-
tion free surface. The Disc Drive requires 7 inches
of vertical rack space. Figure 2-5 shows mounting
dimensions and slide installation details for the
Disc Drive.

2.3   CABLING CONSIDERATIONS

All intercomponent cabling within the Disc Drive is
completed at the factory, but the interface signal,
cabling (both data and control), and primary AC
power connections must be completed in the field. A
ground strap must be connected between a convenient
point on the 3300 deck casting and the power supply
DC ground of the controller. Instructions for fabri-
cating the necessary cables are contained below.

It is necessary to fabricate the cables between the
Disc Drive and the Controller. Up to four cables are
used depending on whether the Drive contains fixed
heads, and whether a "Star" or "Daisy Chain" inter-
connect is used.

"A" cables contain status and control signals. "B"
cables contain data and clock signals. "A" cables
connect to J 31 and J34 . "B" cables connect to
J 32 and J 33.
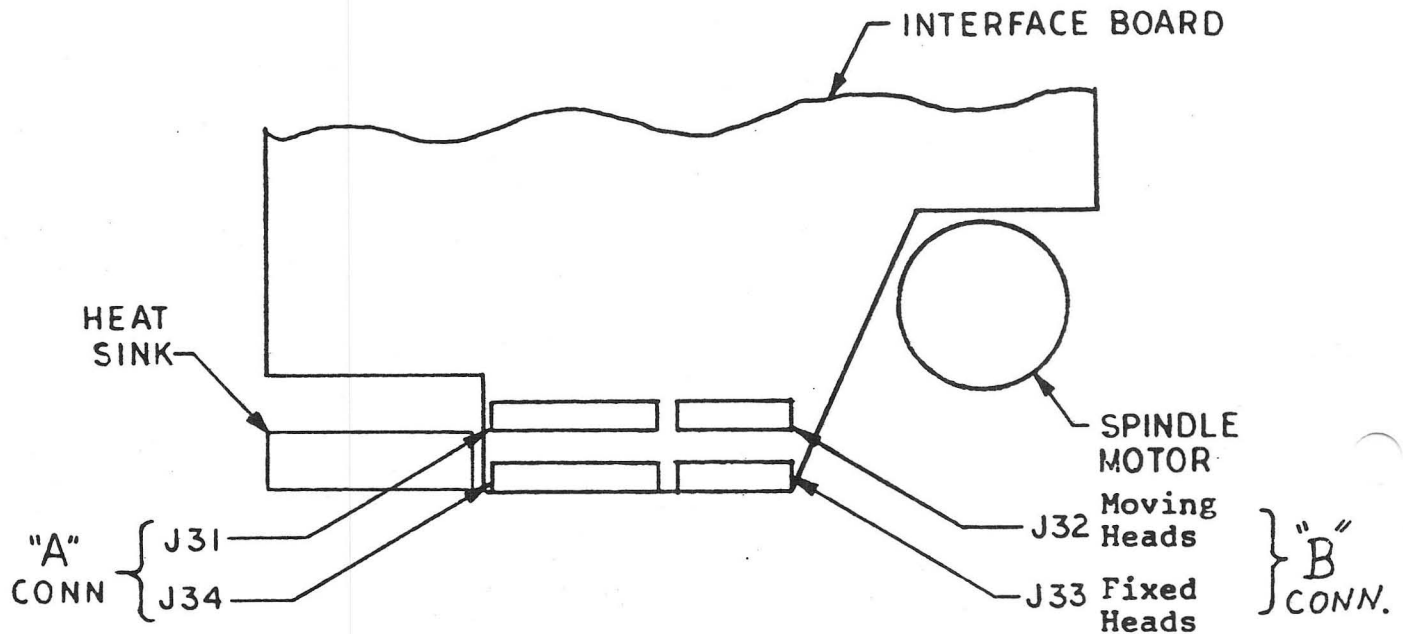
Flat Cable Interface (CDC 9760 Option)

The standard interface accomodates two "A" connectors
and one "B" connector. If multiple drives are con-
nected to the same controller, "A" connectors can be
either in a "star" or "daisy chain" configuration.
"B" connectors must be in a "star" configuration only.

If the drive contains fixed heads a second "B" con-
nector is provided which must also be connected to
the controller in a "star" configuration. The same
"A" connectors can still be used in either a "star"
or "daisy chain" mode. Such arrangements are shown
below. The maximum lengths of the cables can be 100
feet cumulative for the "A" cable "daisy chained"
and 50 feet for each "B" cable.
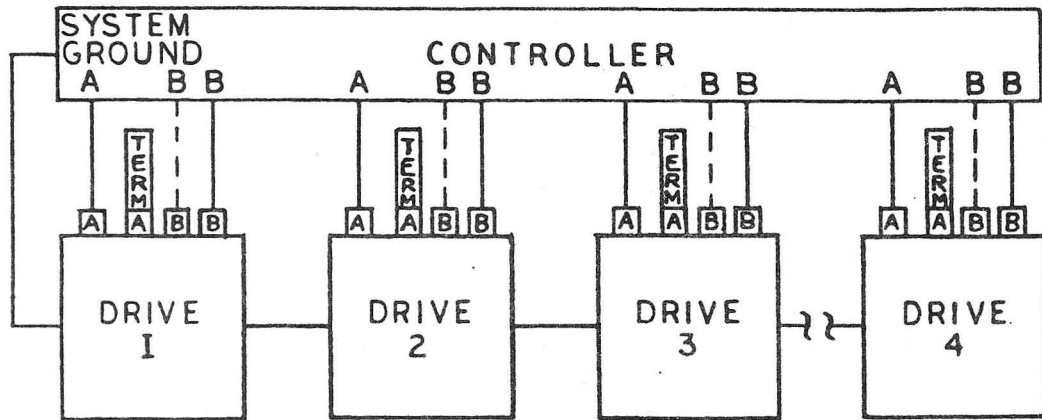
"Star" Interconnect
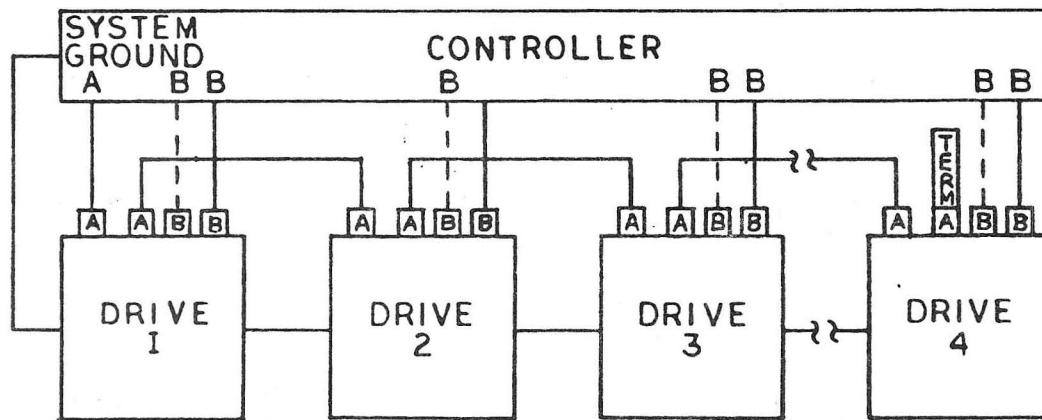
"Daisy Chain" Interconnect

Figure 2-1

2.4 TERMINATORS

Signal line terminating resistors are installed for all "B" connectors on the Interface Board at the factory. An "A" connector terminator assembly Okidata Part Number 30116   must be added as shown depending on whether "Star" or "Daisy Chain" inter-connect is used.

Termination resistors as shown in Figures 2, 3 & 4 must be provided at the transmitter and receiver end of each line at the controller.

2.5 TRANSMITTERS AND RECEIVERS

Transmitters and receivers of the industry standard type 75110A and 75107B or equivalent are used to provide a balanced transmission system. Transmitters and receivers used in the controller must be com-patible. See Figures 2-2, 2-3, & 2-4.

2.6 CONNECTORS AND CABLE (See Tables 2-1 & 2-2 for pin assign-ments)

Description	Amp P/N	3M P/N	Ansley P/N	Spectra Strip P/N
"A" Connector (60 Pin)	88012-2	--	609-6001M	
"A" Cable 30 Pair Twisted 28 awg.				SS-455-248-60
"B" Connector (26 Pin)	86905-2	3399-3000	609-2601M	
"B" Cable 26 Line with Ground Plane and Drain Wire		3476-26		

Maximum Cable Length: "A" Cable 100 ft. cumulative
                        "B" Cable 50 ft.

Ground Strap: Tinned copper braid 7/16 flat width

Power Cable: Size per appropriate current (2.8-2.9) connector per 2.7

75107B - DUAL LINE RECEIVER

TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES		OUTPUT Y
	G	S	
$V_{ID} \geq 25$ mV	L or H	L or H	H
	L or H	L	H
-25 mV $< V_{ID} < 25$ mV	L	L or H	H
	H	H	INDETERMINATE
	L or H	L	H
$V_{ID} \leq -25$ mV	L	L or H	H
	H	H	L
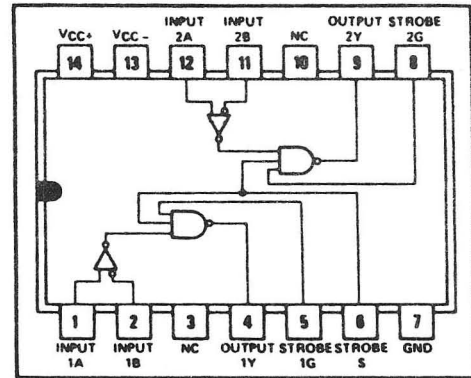
NC—No internal connection

75110 - DUAL LINE DRIVER

TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the on state

High output represents the off state
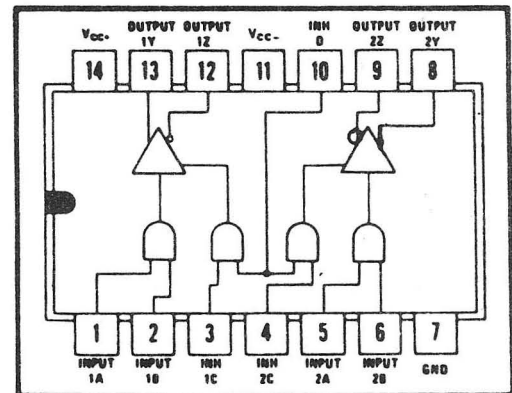
FIGURE 2-2 A AND B CABLE LINE DRIVERS

CONTROLLER | A CABLE | DRIVE | TERMINATOR

100 CUMULATIVE FEET MAX
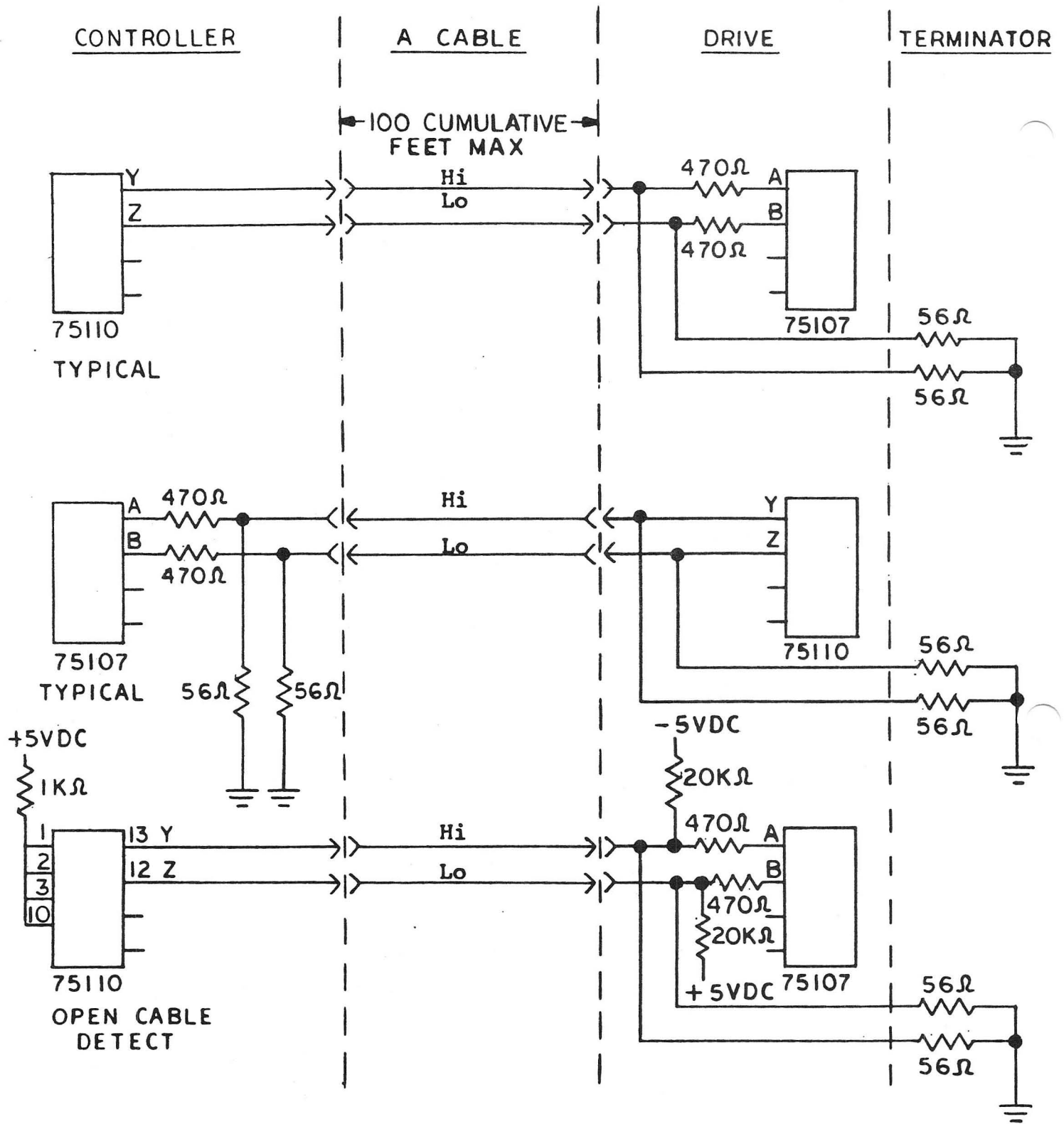
FIGURE 2-3 A CABLE TRANSMITTERS & RECEIVER

II-6

CONTROLLER

B CABLE

DRIVE 0

Hi

Lo

75110

470Ω

470Ω

75107

50 FT
MAX

82Ω

82Ω

A

470Ω

Hi

Y

B

470Ω

Lo

Z

75107

82Ω

82Ω

75110
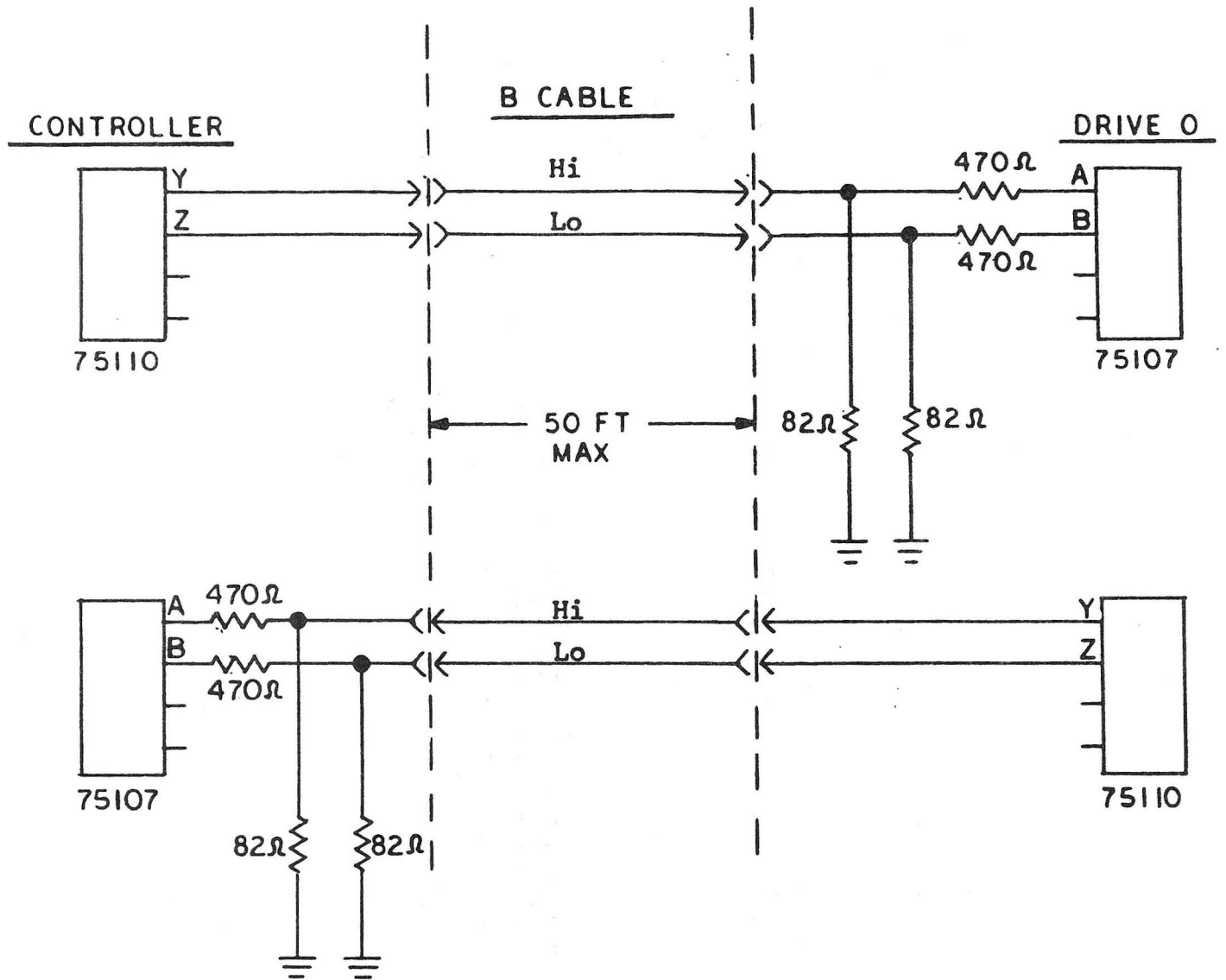
FIGURE 2-4"B"CABLE TRANSMITTERS & RECEIVERS
II-7

TABLE 2-1

"A" CABLE CONNECTIONS

- FLAT CABLE INTERFACE -

PIN NUMBERS

LO	HI	LINE
22	52	Unit Select Tag
23	53	Unit Select 2^0
24	54	Unit Select 2^1
26	56	Unit Select 2^2
27	57	Unit Select 2^3
1	31	Tag 1
2	32	Tag 2
3	33	Tag 3
4	34	Bit 0
5	35	Bit 1
6	36	Bit 2
7	37	Bit 3
8	38	Bit 4
9	39	Bit 5
10	40	Bit 6
11	41	Bit 7
12	42	Bit 8
13	43	Bit 9
14	44	Open Cable Detector
18	48	Index
25	55	Sector
15	45	Fault
16	46	Seek Error
17	47	On Cylinder
19	49	Unit Ready
20	50	Address Mark Found
28	58	Write Protected
	29	Power Sequence Pick
	59	Power Sequence Hold
21	51	Busy
30	60	Ground

TABLE 2-2

"B" CABLE CONNECTIONS

PIN NUMBERS

HI	LO	DATA LINE
14	2	Servo Clock
16	3	Read Data
17	5	Read Clock
19	6	Write Clock
20	8	Write Data
9	22	Unit Selected
23	10	Seek End
24	12	Index (Ungated)
26	13	Sector (Ungated)

Pin numbers 1, 15, 4, 18, 7, 21, 11 & 25 are ground.

2.7   POWER CABLE

The customer must fabricate a power cable consistent
with his system's AC distribution and power require-
ments outlined below. The standard AC connector,
located on the rear of the machine, is an inter-
nationally approved 3-prong receptacle whose dimensions
are shown below:
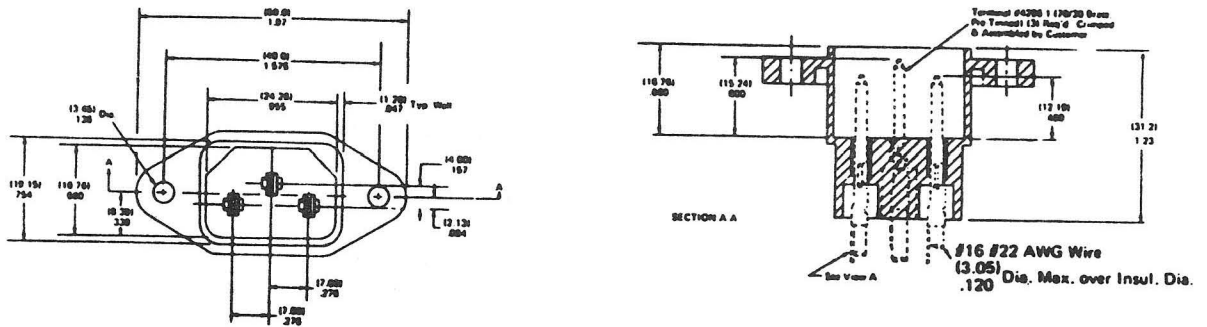
2.8   STARTING CURRENT
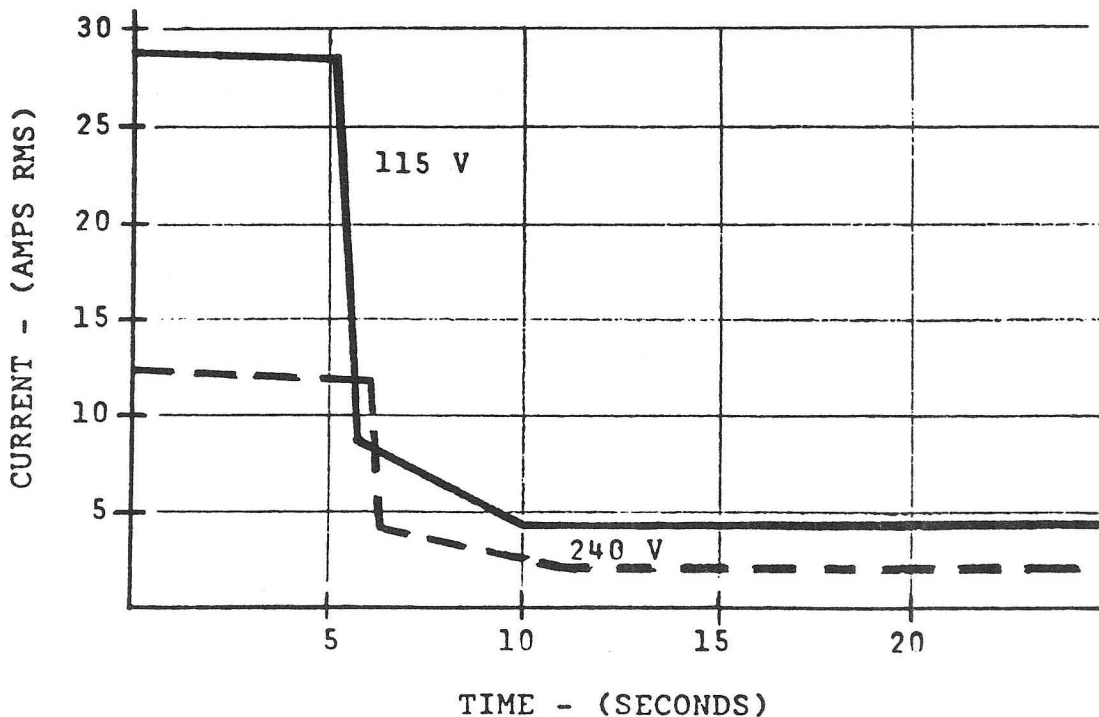
2.9 RUNNING CURRENT AND POWER

The following values are maximum with discs spinning and positioner undergoing a worst case seek:

Voltage	Frequency	Current (Amps)	Power (VA)	Power Factor
115	60	5.2	616	.81
240	50	2.4	575	.85

2.10 UNPACKING THE DISC DRIVE

The Disc Drive is shipped in a special packing case and frame which should be saved if re-shipment of the equipment is planned.

Within the packing case, the Disc Drive is mounted on each side to a frame with two bolts. This frame can be used to hold the unit when it is removed and placed on a level surface on either of six sides for inspection or future servicing. Use of the frame for servicing is not necessary, however, as the unit can be placed on a level surface on its side as shown in Figure 5-1.

A set of slides, the front panel, and a hardware kit for mounting these parts is contained in the package located beneath the disc drive.

As the equipment is unpacked, care should be exercised to prevent damage to the finished surfaces of the Disc Drive, and all parts should be examined for evidence of damage during shipment (particularly if the inner container has been punctured). If any parts are damaged, advise OSMP, Incorporated and file a claim with the transfer company. The crated weight of the Disc Drive is approximately 100 pounds.

Inspect all sides of the unit for loose connectors and/or components, and replace where necessary.

2.11   INSTALLATION PROCEDURE (REFER TO FIGURE A)

a) Extend both of the slides provided and remove
   the sliding element from the stationary element
   by depressing the release clip.

b) Mount the stationary slide elements in a standard
   19 inch rack as shown in Figure 2-5. Be sure the
   width dimension is maintained front to rear across
   both elements or binding will occur. Both the
   front and rear mounting brackets must be used to
   support the weight of the Disc Drive.

c) Remove the shipping frame from the Disc Drive
   one side at a time, letting it rest on a level
   surface which is clean of debris.

d) Attach the moving element of the slides to each
   side of the Disc Drive casting as shown in
   Figure A using the 10-24 screws provided.

e) Attach the front cover mounting brackets as shown
   in Detail A with the 10-24 screws provided.

<u>CAUTION</u>

The Disc Drive weighs approximately 65 pounds.
The rack into which the Disc Drive is mounted
must be of sufficient weight to prevent over-
turning when the Disc Drive is extended into
its service position.

f) Now carefully lift the Disc Drive and engage the
   moving slide element attached to the Drive into
   the stationary element previously mounted to the
   rack and slide back into the rack until the front
   cover bracket engages the rack. Should binding
   occur, the stationary slide element should be
   adjusted for a constant width front to rear.

g) Slide the Disc Drive forward until it hits its
   stops. This is the service position.

h) Mount the front panel by snapping in place as shown in Detail A.

i) Now carefully slide the Drive back into the rack being particularly careful that no interference exists. If interference exists, move the stationary elements of the slides to increase clearance while maintaining the width dimension front to rear. This same procedure must be followed if interference exists on the top or bottom of the Disc Drive.

j) Return the unit to the extended service position and remove the front cover.

k) Attach the interface cables and make sure the unit can slide freely with no binding of cables.

l) Check again for any loose connections or components.

CAUTION

Be sure the breather filter, Page 9, is clear and unobstructed when the unit is in its operating position within the rack. Serious damage can result to heads and discs if this filter is obstructed.

CAUTION

Serious damage to the spindle motor and start components can result if 100 V is applied to a 200 V machine or vice versa.

m) Check that the voltage and frequency at the power connector corresponds to those listed on the unit name plate.

n) Following power supply schematic (30120), determine if the power supply transformer taps can be changed to a voltage close to that of the line to be used. If necessary, change the jumpers in the power supply plug, per sect. 5.3.

o) Check the fuses. Two AC fuses are located at the
rear of the AC distribution box and four DC fuses
are located at the lower rear of the heat sink
assembly. (Figures 5-34 & 5-5)

p) Familiarize yourself with the Disc Drive controls
by reading Paragraphs 3.1 through 3.3.

IMPORTANT

The head positioner within the Disc Drive is
shipped with a shipping clamp which must be
loosened before power is applied to the machine.

CAUTION

The shipping clamp arm must not be moved while
the discs are at rest or serious damage to heads
and discs can result.

q) Refer to Figure 5-1. Remove the positioner ship-
ping clamp screw, being careful not to move the
shipping clamp arm. Bolt the screw and washer to
the casting for possible future use. Remove the
spindle shipping clamp from the spindle pulley
and rotate into storage position, retaining this
hardware for possible future use.

CAUTION

If the machine is to be re-shipped, or removed
from the rack, the shipping clamp arm under the
head positioner and the spindle shipping clamp
must be fastened in place. If not, serious damage
to heads and discs will result. When fastening
the spindle shipping clamp, rotate spindle only
in direction indicated.

CAUTION

NEVER move the shipping clamp arm while the discs
are at rest. As part of the power off sequence,
the shipping clamp arm should come to rest ready
for clamping. If this does not occur, power the
drive up and down again.

r) With the power switch at the control panel in the
off position, connect the power cable.

s) Turn the power switch on. The power switch should illuminate and the Drive should come up to speed. The "Ready" light should come on. Turn the power switch off.

t) Slide the Drive carefully back into the rack and fasten in place with (2) 10-32 screws. (Figure 2-5)

u) Snap the front panel into position.

19.000
DISK DRIVE

19.062

DETAIL A

CHASSIS SLIDE

FRONT COVER
MOUNTING BRKT

RELEASE CLIP

SLIDE MTG ADJUSTMENT

STATIONARY
ELEMENT

SLIDING ELEMENT

26.00
SERVICE POSITION

10-24 X 3/8 LG PAN HD SCR
(5 REQD)
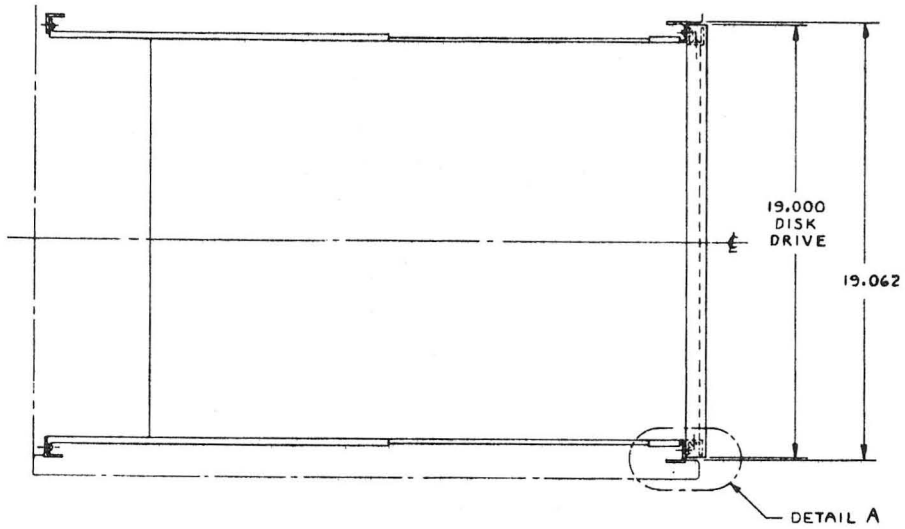
10-32 X 1/2 LG PAN HD SCR
(8 REQD) FARSIDE
NO.10 FLAT WASH (8 REQD)
NO.10 SPLIT LK WASH (8 REQD)

18.312

17.750
MIN. OPENING BETWEEN
MOUNTING RAILS

16.87
SLIDE MTG DIM

1.12

7.00

.625

1.125

.875

.030
NOM GAP

7.00

6.969
COVER

10-32 X 3/8 LG SCREW
FASTENS DRIVE TO
CABINET RAIL
(ACCESSABLE ONLY WITH
FRONT COVER REMOVED)

FRONT COVER

FRONT COVER MOUNTING BRACKET

10-24 X 1/2 LG PAN HD SCR (4 REQD)
NO.10 FLAT WASH (4 REQD)
NO.10 SPLIT LK WASH (4 REQD)

FRONT COVER FASTENERS (SNAP ON)

CABINET RAIL

10-32 X 3/8 LG PAN HD SCR (2 REQD)
NO.10 FLAT WASH (2 REQD)
NO.10 SPLIT LK WASH (2 REQD)

DETAIL A

SHIPPING FRAME

REMOVE SCREWS
AND USE FOR
MOUNTING SLIDES
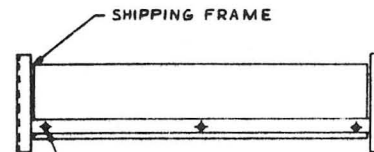
SHIPPING FRAME
REMOVAL DETAIL

INSTALLATION DRAWING

FIGURE 2-5

SECTION III

OPERATION, INTERFACING AND FORMATTING

3.1   INTRODUCTION

This section contains information on operation, interfacing and formatting the Disc Drive. Operation of the Disc Drive is basically under system control and there is little to be done by the operator other than applying power under normal conditions.

To properly operate, the Disc Drive must be connected to a properly configured controller. This section describes all interface line functions and timing requirements.

Efficient utilization of the Disc Drive capacity and error free performance are heavily dependant on how the Drive is formatted. This section describes format requirements and indicates how to calculate the efficiency of capacity utilization for a given format.

ON
OFF
4
14
RDY FLT
W.P. F.H.
W.P. M.H.
W.P. ALL
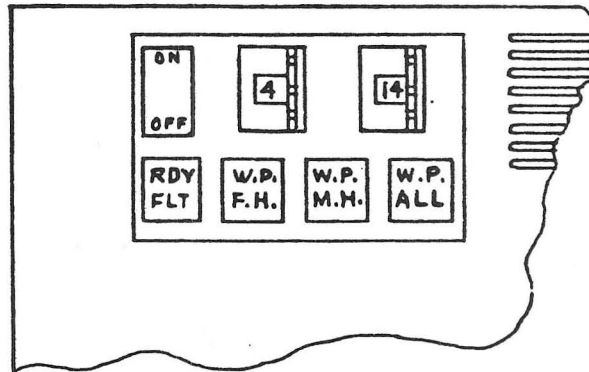
3.2 CONTROLS AND INDICATORS

All controls and indicators are located at the upper
left hand corner of the front panel. The following
switches and indicator lights are provided as
standard:

Name	Function
Power On/Off	Indicator/Switch 'On' initiates the power-up sequence within the drive. 'Off' removes primary power within the Drive initiating the shutdown sequence. The switch is illuminated when primary power is on.
Ready/Fault	Indicator indicates 'Ready' by being constantly illuminated. 'Fault' is indicated by a flashing illumination on and off.

Optional Controls:

Name	Function
Write Protect	Illuminated push button
Fixed Head (W.P.F.H.)	Protects fixed head data only.
Moving Head (W.P.M.H.)	Protects moving head data on one surface only.
All (W.P.ALL)	Protects entire Drive.
Unit Address	Thumbwheel switch (16 position). One or two switches can be provided to accomodate both fixed and moving heads. Positions 14 and 15 are reserved for maintainance only. This switch position should be changed only when the Drive is off line (not selected).

If the Disc Drive is not provided with a Unit Select thumbwheel switch it will be provided with a DIP plug (P/N 30387) on the Interface board; the unit address will be 0 for moving heads and 1 for fixed heads, if any.

3.3   FAULT CONDITIONS

The 3300 is designed to detect a variety of fault conditions where an internal self-protect feature is executed and external indicators are set for the operator and disc controller. Fault recovery, consisting of an internal restore operation, requires manual intervention in the cases where a fault condition persists and for certain fault types.

Under normal conditions both the Power switch and Ready indicator will be continuously illuminated.

If the Power light and Ready light go off, AC power has failed. Check the fuses and line power.

If the Power light remains on, but the Ready light goes off, or flashes, follow this procedure:

a) If furnished with thumbwheel unit select switches be sure both unit adresses are not the same.

b) Wait 15 minutes with power on to see if automatic recovery occurs.

c) Turn power off, then "on".

d) If the Ready light does not come on, check fuses.

e) If the condition persists or quickly recurs, service is required.

3.4   INTERFACE (DATA AND CONTROL)

The Disc Drive interface is compatible with the CDC 9762 (Storage Module), with the following exceptions:

a) The system must handle the Drive data transfer rate (7.97 MBits per sec).

b) The system should transfer and receive data in NRZ (CDC NRZ option).

c) Up to (12) head addresses are legal, and only track addresses 0 through 338 are legal.

Moving head and fixed head hybrid drives utilize a common interface. Fixed head tracks are addressed using the cylinder address lines (also used for moving heads). Fixed heads will be designated by a unit select address which is different from the moving heads in the same drive. Unit addresses are accomplished with a plug on the interface board, or with optional control panel thumbwheel switches.

Overlap Seek:

The fixed head unit and moving head unit appear to a controller as two independent drives permitting an overlap seek feature where read or write on fixed heads may be enabled while moving heads are undergoing a seek in the same drive. For this purpose, two "B" connectors are provided on drives containing both fixed and moving heads. (See Pages II-2 & III-5).

TABLE 3-1

CDC 9762 COMPATIBLE INTERFACE

"A" CABLE

```
                           UNIT SELECT TAG
                           UNIT ADDRESS LINES (0 TO 3)
                           TAG 1 (CYLINDER ADDRESS)
                           TAG 2 (HEAD SELECT)
                           TAG 3 (CONTROL SELECT)
                           BUS LINES (0 TO 9)
                           OPEN CABLE DETECT
                           INDEX
COMPUTER                   SECTOR
                           FAULT
SYSTEM                     SEEK ERROR
                           ON CYLINDER
DISC                       UNIT READY
                           ADDRESS MARK FOUND
CONTROLLER                 WRITE PROTECTED
                           BUSY
                           POWER SEQUENCE PICK
                           POWER SEQUENCE HOLD
                           "B" CABLE (MOVING HEADS)

                           SERVO CLOCK
                           READ DATA
                           READ CLOCK
                           WRITE CLOCK
                           WRITE DATA
                           UNIT SELECTED
                           SEEK END
                           INDEX
                           SECTOR



                           *"B" CABLE (FIXED HEADS)

                           SERVO CLOCK
                           READ DATA
                           READ CLOCK
                           WRITE CLOCK
                           WRITE DATA
                           UNIT SELECTED
                           SEEK END
                           INDEX
                           SECTOR
```

3300

INTERFACE

BOARD
*

*OPTIONAL   CON'T.

III-5

TABLE 3-1 (cont'd)

DEFINITION OF "A" CABLE BUS LINES

BUS LINES	TAG 1 (CYLINDER ADR.)	TAG 2 (HEAD ADR.)	TAG 3 (CONTROL FUNCTION)
0	1	1	WRITE ENABLE
1	2	2	READ ENABLE
2	4	4	SERVO OFFSET +
3	8	8	SERVO OFFSET −
4	16	−	FAULT CLEAR
5	32	−	ADDRESS MARK ENABLE*
6	64	−	RESTORE
7	128	−	DATA STROBE EARLY
8	256	−	DATA STROBE LATE
9		−	RELEASE

*OPTIONAL

3.5   INTERFACE SIGNALS (SEE SECTION 2 FOR CABLING: ALSO
SEE TABLE 3-1)

CABLE "A" SIGNALS (RECEIVED BY THE UNIT):

a) Cylinder Address (Tag 1)

Ten bus lines (Tag 1) are used to carry the
cylinder address to the 3300. Since the disc
is a direct addressing device, the controller
need only place the new address on the lines
and strobe the lines with Tag 1 (see Figure
3-4). The unit must be On Cylinder before
Tag 1 is sent. The bus lines should be stable
throughout the tag time. Tag 1 must be from
1.0 us to 0.5 ms in duration. Only cylinder
addresses from 0 through 338 will be accepted
by the drive; greater numbers will result in
"Seek Error".

b) Head Select (Tag 2)

This signal is the head address that will be
selected by bits 0 through 4. Tag 2 must be
from 1.0 us to 0.5 ms in duration.

c) Control Select (Tag 3)

This signal acts as an enable and must be
true for the entire control operation.

1. Write Gate (Bit 0)

The Write Gate line enables the write
driver. Data is automatically protected
by inhibiting the Write Enable in all
fault conditions viz:

A. Fault, line true

B. On Cylinder, not true

C. Seek Error, line true

D. Ready, not true

E. Open Cable

2. Read Gate (Bit 1)

Enabling of the Read Gate enables digital
read data to the transmission lines. The
leading edge of Read Gate triggers the read
chain to synchronize on an all zeros pattern.

III-7

3. Servo Offset Plus (Bit 2)

   When this signal is true, the actuator is
   offset from the nominal On Cylinder position
   towards the spindle.

4. Servo Offset Minus (Bit 3)

   When this signal is true, the actuator is
   offset from the nominal On Cylinder position
   away from the spindle.

5. Fault Clear (Bit 4)

   A 100 ns minimum pulse sent to the 3300 will
   clear the fault flip-flop for the selected
   unit if the fault condition no longer exists.

6. AM Enable (Bit 5) (Optional)

   The AM (Address Mark) Enable line, in con-
   junction with Write Gate or Read Gate, allows
   the writing or recovering of Address Marks
   (See Figure 3-3). When AM Enable is true while
   Write Gate is true, the writer will stop
   toggling and erase the data, creating an
   Address Mark. Write Fault detection in the
   unit is inhibited by this signal.

   When AM Enable is true while Read Gate is
   true, an analog voltage comparator detects
   the absence of read signal. If the duration
   of the erased area is greater than 16 bits,
   an Address Mark Found signal will be issued.

   NOTE:
   If Address Mark is not used, Bit 5 must be
   held inactive during Control Select functions.

   Address Mark should be 3.0 to 3.5 bytes in
   length with no transitions.

7. RTZ (Bit 6)

   A 250 ns minimum, 1.0 ms maximum pulse, sent
   to the unit will cause the actuator to seek
   track 0, reset the Head Register and clear
   the Seek Error flip-flop. For the fixed head
   unit the Track Address Register will be cleared
   as opposed to the Head Register.

This seek is significantly longer than a
normal seek to track 0, and should only
be used for recalibration, not data
acquisition.

8. Data Strobe Early (Bit 7)

When this line is true, the PLO Data
Separator will strobe the data at a time
earlier than nominal. Normal strobe tim-
ing will be returned when the line is false.

9. Data Strobe Late (Bit 8)

When this line is true, the PLO Data
Separator will strobe the data at a time
later than nominal. Normal strobe timing
will be returned when the line is false.

NOTE:

The Data Strobe and Servo Offset signals
are intended to be used as an aid to re-
cover marginal data. The Servo Offset
and Data Strobe position return to nominal
when the respective signals go false. A
Servo Offset will result in loss of On Cyl-
inder and Seek End for a period of 3.2ms
maximum (see Figure 3-4). The maximum time
for the carriage to move from forward to
reverse offset or vice versa will not exceed
7ms; The Servo Offset lines should never be
simultaneously on. Data shall not be written
while in the offset mode.

10. Release (Bit 9) (Dual Channel Only)

This bit is currently ignored by the inter-
face when used with unit addresses 0 through
13. For unit addresses 14 and 15, this line
is used to assert margin mode and to override
write faults.

d) Unit Select Lines (2^0, 2^1, 2^2, 2^3) and Unit Select Tags

The Unit Select Tag signal gates the four Unit Select
Lines into the logic number compare circuit. The unit
will be selected internally 200 nsec (maximum after
leading edge of this signal). For timing, see Figure
3-2. The moving head and fixed head unit numbers may
be selected by either two thumbwheel switches on the
front panel or by one jumper plug on the I/O board.
Unit addresses 14 and 15 are reserved for use in field
maintenance.

e) Open Cable Detector

Inhibits write gate and unit select when the "A" interface cable is disconnected or controller power is lost.

f) Power Sequence Pick and Hold

The lines are bussed through on the drive to prevent interference with a "daisy chain" of drives which utilize the automatic power sequencing option.

CABLE "A" SIGNALS (TRANSMITTED BY THE UNIT):

a) Sector Mark

Signal derived from the servo track. Any number of sectors can be provided ranging from 2 bytes per sector to 8192 bytes per sector. The number of bytes per sector is selected by a DIP plug (P/N 30388) on the I/O board. The last sector of the revolution may be longer if necessary.

b) Index

This signal occurs once per revolution, and its leading edge is considered the leading edge of the Sector Zero, typically 2.5 usec. (See Figure 3-1). Timing integrity is retained throughout seek operations.

c) Unit Ready

Indicates that selected unit is up to speed, heads are on a track, and no fault exists.

d) Address Mark Found (Optional)

Address Mark Found is a 9.0 max. usec pulse which is sent to the controller following recognition of at least 16 missing transitions and the first zero of the zeros pattern.

The controller should drop the Address Mark Enable line (Bit 5) upon receiving Address Mark Found (AMF) and valid data will be presented on the I/O lines following the AMF pulse (Figure 3-3).

e) On Cylinder

For moving heads "On Cylinder" indicates that the heads are positioned over a track. For fixed heads, this response is made automatically once a track is selected. This status line is cleared with any seek instruction. For moving heads, a carriage offset will result in loss of "On Cylinder" for a period of 3.2 ms (nominal). See Figure 3-4.

f) Seek Error

Seek Error will be true for moving heads when either Seek Late or Illegal Address (an address greater than the number of data cylinders) occurs. Seek Error will inhibit "On Cylinder" and Write Enable and will only be cleared by performing an RTZ. For fixed heads Seek Error will not be used unless the contiguous track address option is present. In that event Seek Error will be true if an address greater than the number of fixed heads in the drive is requested. "On Cylinder" and Write Enable are disabled in the same fashion as the moving heads.

g) Fault

Fault for the selected unit will be set true for a number of fault conditions and will remain true until the fault condition no longer exists and a Fault Clear pulse is received. Fault conditions are:

1. Multiple Heads Selected

2. Write Protect Violation

3. Multiple Control Tags Received

4. Read or Write Off Cylinder

5. Simultaneous Write and Read Gates

6. Write While Servo Offset

7. Write Current Not On During Write

8. Write Current On During Non-Write

9. Fixed and Moving Head Unit Number Set Equal by Front Panel Switches or by Unit Address Plug.

10. Loss of DC Power

h) Write Protected (Optional)

This signal is true for the selected unit for as long as a Write Protected portion of the drive is addressed. Those portions which may be protected are:

1. Moving Head 0 (all associated tracks)

2. All Fixed Head Tracks

3. Entire Drive (all moving and fixed head tracks)

Attempting to write while protected will cause a fault to be issued.

i) Busy

This line provides compatibility with controllers which utilize the dual port option. Busy is always low to indicate the drive is not currently busy with another controller.

CABLE "B" SIGNALS (RECEIVED BY THE UNIT):

a) Write Clock

This line transmits the Write Clock signal which must be synchronized to the NRZ data as illustrated in Figure 3-6. The Write Clock is the Servo Clock retransmitted to the drive by the controller during a write operation. The received Write Clock is phase-locked again to eliminate any potential transmission distortion. So as not to require a phase-lock startup time, Write Clock should be transmitted continuously.

b) Write Data

Carries data to be recorded on the disc. Data is NRZ, and is clocked onto the disc by the disc drive. See Figure 3-6.

CABLE "B" SIGNALS (TRANSMITTED BY THE UNIT):

a) Servo Clock

Phase-locked 7.97 MHz clock generated from the servo track tribits. It is used to transfer data to the drive. Servo Clock is available at all times (not gated with Unit Select). See Figure 3-6.

b) Read Data

Carries data recovered from the disc. Data
is NRZ. See Figure 3-5.

c) Read Clock

The Read Clock defines the beginning of a data
cell. It is an internally derived clock signal
and is synchronous with the detected data as
specified in Figure 3-5. This signal is trans-
mitted continuously, and is in phase sync within
7 us after Read Gate.

d) Seek End

Seek End goes true with either "On Cylinder"
or "Seek Error", indicating that a seek oper-
ation has terminated. Seek End will remain
true so long as the positioner remains on cyl-
inder. Seek End status is cleared for at least
30 usec following Tag 1 or servo offset.

e) Unit Selected

When the four unit select bit lines compare
with the jumper plug on the interface board,
and when the leading edge of unit select tag
is received, the unit selected line becomes
true and is transmitted to the controller on
the "B" cable. Multiple unit selected responses
on a daisy-chain system indicate duplicate plugs
have been installed. See Figure 3-2.

f) Sector (Optional)

Sector Mark is transmitted continuously, inde-
pendent of Unit Select, in order to provide look-
ahead for the controller.

g) Index (Optional)

Index is transmitted continuously, independent
of Unit Select, in order to provide look-ahead
for the controller.
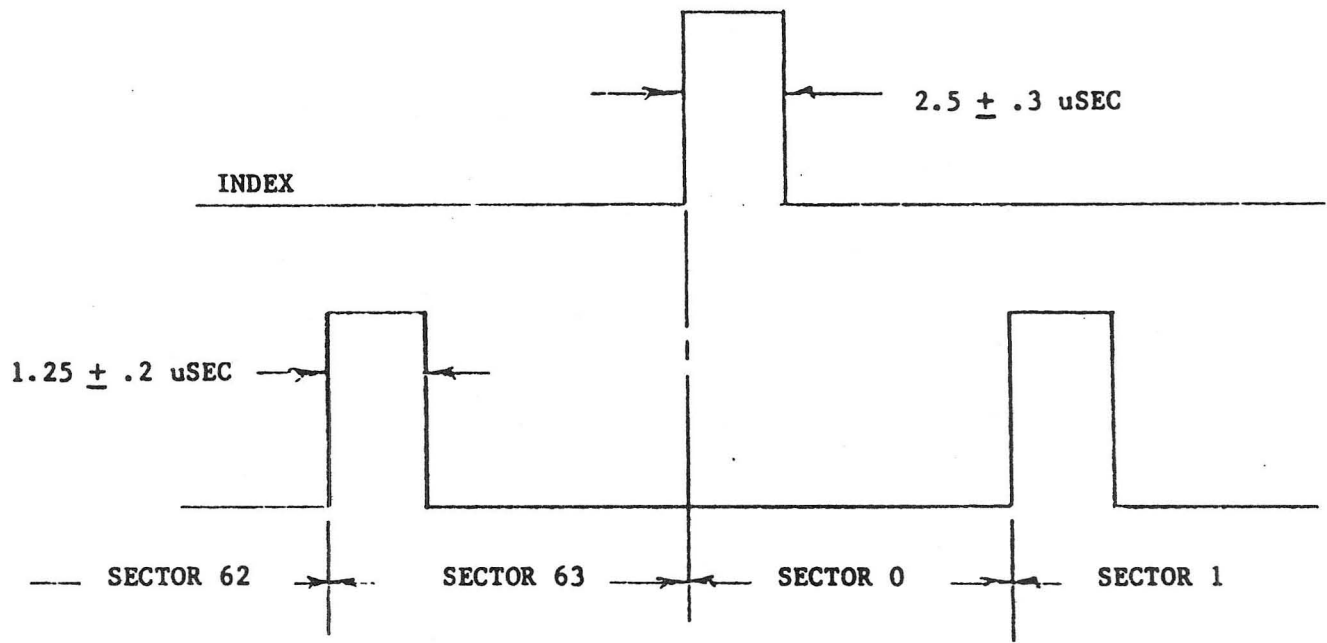
FIGURE 3-1   INDEX AND SECTOR TIMING
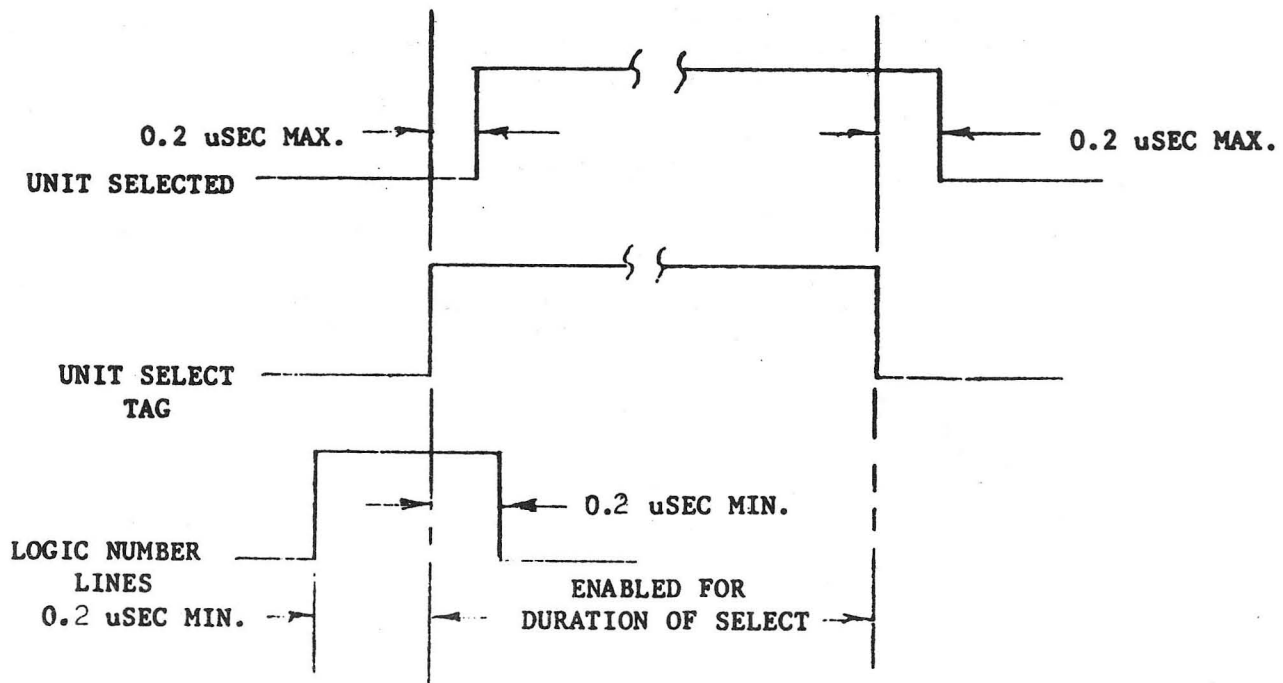
FIGURE 3-2   LOGIC NUMBER SELECT CODE AND TIMING DIAGRAM

SPLICE ③

| DATA FORMAT | ... | ZEROS | AM | 7 BYTES ZEROS MIN. | SYNC | ADDRESS | ZEROS | 7 BYTES ZEROS | SYNC | DATA |

READ OPERATION

HEAD SELECT (TAG 2) — 5uS MIN

READ GATE (BIT 1) ①

CONTROL SELECT (TAG 3) — 200 NS MIN ②

ADDRESS MARK ENABLE (BIT 5) — 1.0 uS MAX. — 9.0 uS MAX.

ADDRESS MARK FOUND

READ DATA — VALID DATA — VALID DATA

WRITE OPERATION

CONTROL SELECT (TAG 3) — 1 BYTE MIN.

WRITE GATE (BIT 0) — 3 BYTES MIN. 3.5 BYTES MAX.

ADDRESS MARK ENABLE (BIT 5) — 5 uS MIN.

HEAD SELECT (TAG 2)

NOTES:

1. READ GATE MUST BE DROPPED PRIOR TO THE ONE BYTE WRITE SPLICE. IT MUST BE REINITIATED AFTER THE WRITE SPLICE AND WITH AT LEAST 7 BYTES OF ZERO BITS REMAINING IN THE SYNC FIELD.

2. ADDRESS MARK ENABLE SHOULD OCCUR SIMULTANEOUSLY WITH READ ENABLE.

3. WRITE SPLICE IS DEFINED AS THAT POINT WHERE A WRITE OPERATION IS BEGUN OR TERMINATED. AN ABRUPT PHASE SHIFT IN THE RECORDED SIGNAL USUALLY OCCURS AT THIS POINT.

FIGURE 3-3 TYPICAL TIMING WITH ADDRESS MARK
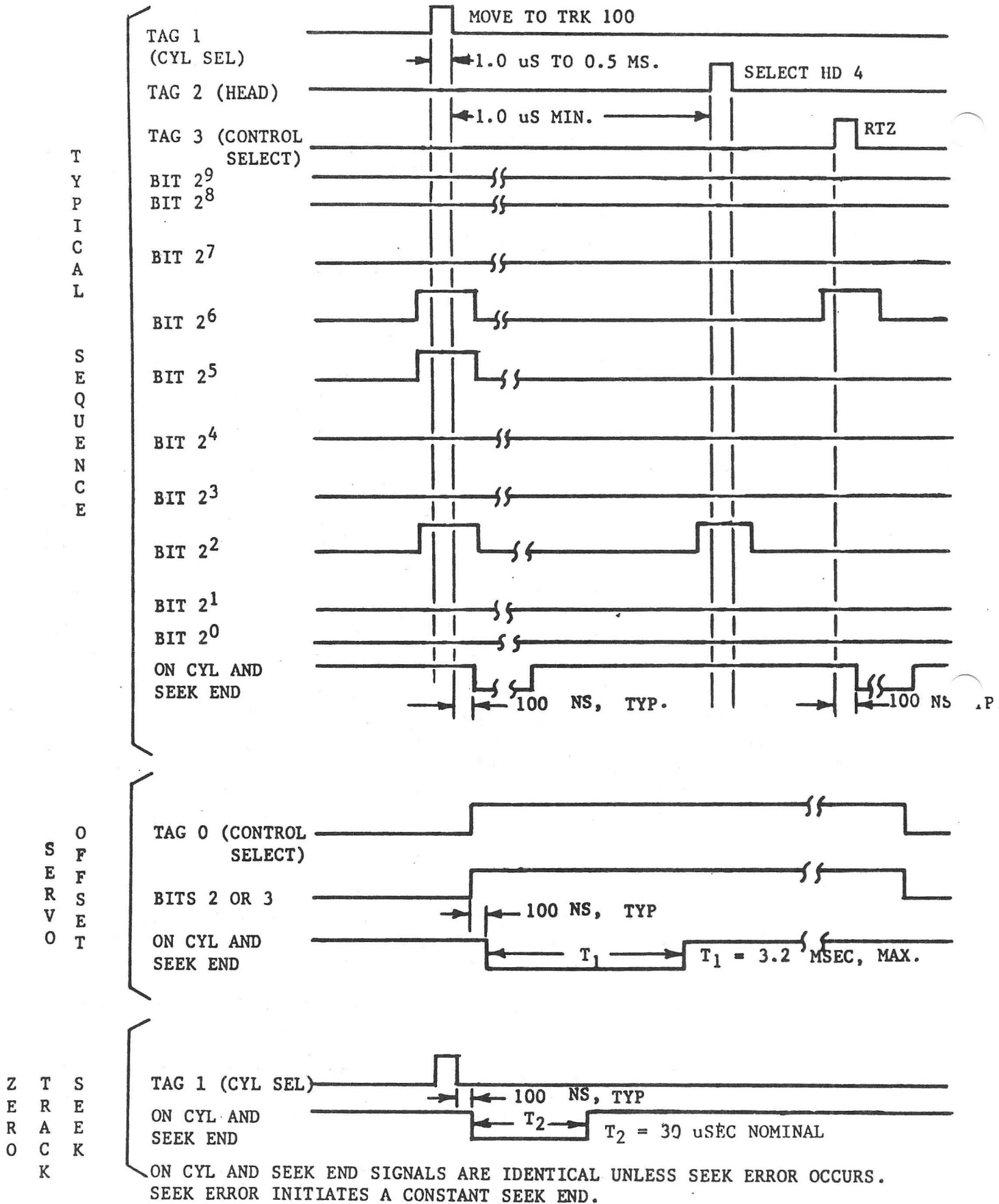
FIGURE 3-4 ON CYLINDER TIMING

III-16-

READ CLOCK

125.5 ± 2   6 ± 4   ②   62.7 ± 6

NRZ DATA   0   0   1   0   1   0   0

125.5 ± 10
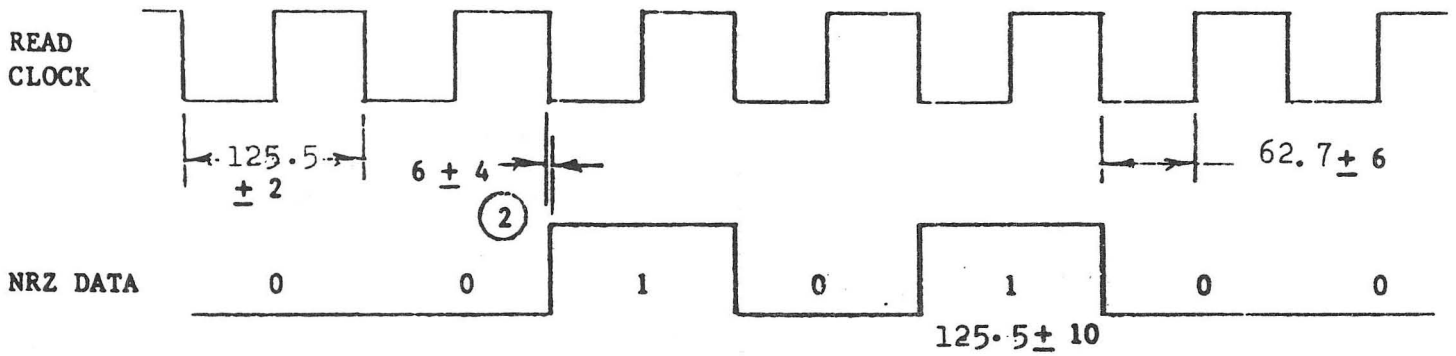
NOTES:

1. ALL TIMES IN NSEC.

②. NEGATIVE EDGE OF CLOCK PRECEDES SIGNIFICANT EDGE OF DATA AT I/O CONNECTOR.

FIGURE 3-5. READ DATA TIMING

7.97 MHZ SERVO CLOCK ③

125.5   ②   62.7 ± 2

NRZ DATA ③   0   0   0   ②   1   0   1   0   0

125.5

62.7 ± 30   62.7 ± 25

7.97 MHZ WRITE CLOCK ③
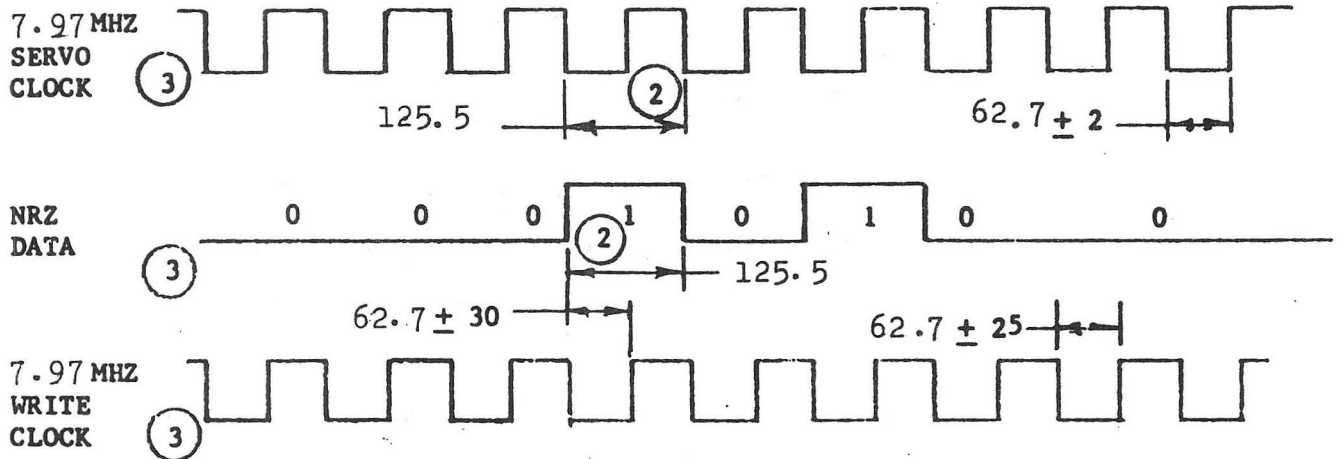
NOTES:

1. ALL TIMES IN NSEC.

②. SIMILAR PERIOD SYMMETRY SHALL BE ±2 NSEC AT I/O CONNECTOR IN DRIVE, SPEED VARIATION TOLERANCE SHALL BE ±5% OF PERIOD WHICH INCLUDES SPINDLE SPEED TOLERANCE AND TRIBIT DROPOUT WHILE CARRIAGE IS MOVING.

③. AT I/O CONNECTOR IN CONTROLLER.

FIGURE 3-6 WRITE DATA AND SERVO CLOCK TIMING

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1.0 uSEC MIN. ②

TAG LINE ①

0.2 uSEC MIN.

TAG LINE

0.2 uSEC

1.0 uSEC MIN.

TYPICAL
BUS BIT
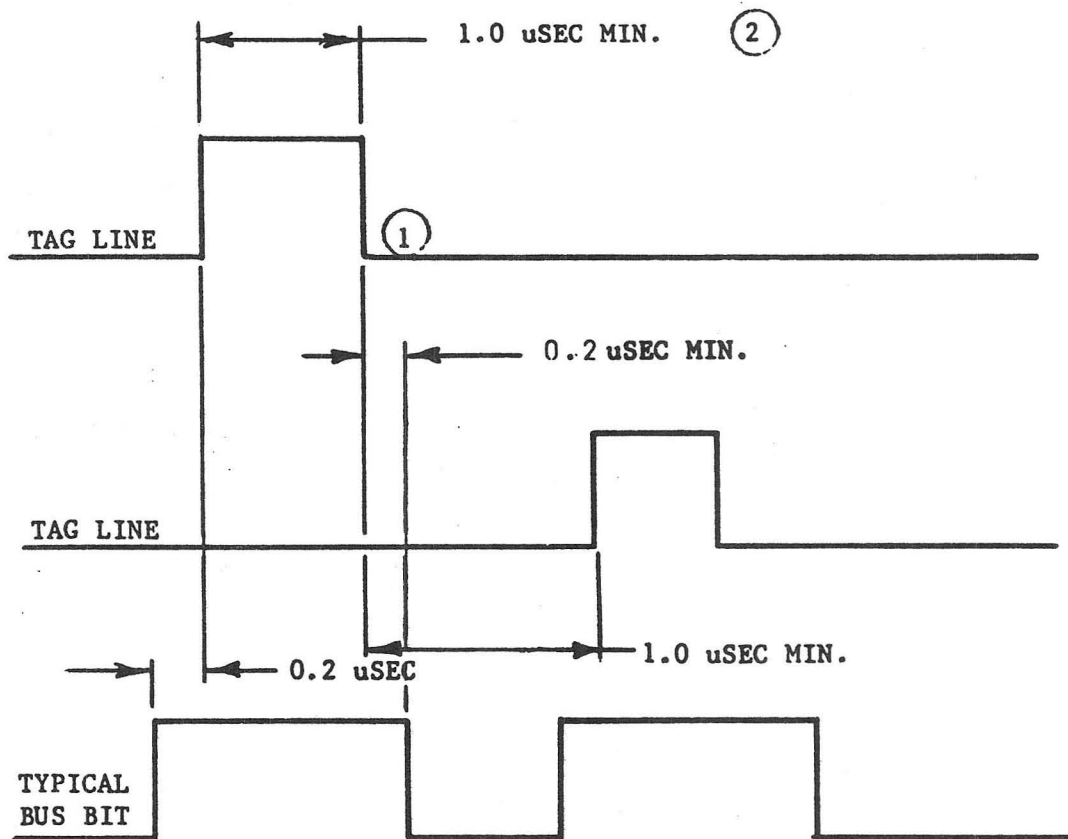
① DOES NOT APPLY TO CONTROL SELECT FUNCTIONS.

② TAG 1 (CYL SEL) MAX. LENGTH IS 0.5 MSEC.

FIGURE 3-7 TAG LINE AND BUS TIMING TOLERANCE

3.6   DATA FORMAT AND DATA CONTROL TIMING

a) Format Suggestions

NOTE

With 20160 bytes per track, the OSMP
3300 capacity is identical to the CDC SMD
and MMD drive capacities and, therefore,
the 3300 can be formatted with the same
formats recommended for the CDC drives.
In addition, the 3300 with 20160 bytes
per track may be formatted with more use-
able bytes per track than the CDC drives
due to faster PLO lock-up time and non-
removable drive media which eliminates
head skew problems. These higher capacity
formats for both fixed and variable sector
data records are shown in Figures 3-8 and
3-9.

The record format on the disc is under control of
the controller. The index and sector pulses are
available for use by the controller to indicate
the beginning of a track or sector.

Some hardware oriented constraints must be recog-
nized when designing a format. The following is
a list of those format parameters:

1. Beginning-of-Record Tolerance

   This tolerance must be provided to allow
   for worst case conditions of mechanical
   and circuit tolerances.

   This gap must be written with a minimum
   of 2 bytes of zeros.

NOTE

To allow for head switching between sectors,
a gap of 7 bytes of zeros is recommended.

2. Read PLO Synchronization

   The synchronization time needed to allow
   the phase-locked oscillator to synchronize
   is 7 us of zeros.

3. Sync Pattern

The Sync Pattern consists of a 00000001
pattern indicating the beginning of the
address or data area (one "one" bit is
the minimum required).

NOTE

In the sample formats (Figures 3-8 & 3-9),
the first 7 0's in this pattern are used
to augment the PLO sync bytes.

4. Write Splice

The write driver turn-on time is 0.3 usec.
Therefore, a write splice area must be
provided in the format preceeding data. It
is recommended 1 byte be provided for this
function.

5. End-of-Record Pad

This field is one byte to ensure that the
last bit is not distorted or destroyed in
an erroneous readback.

6. End-of-Record Tolerance

This tolerance is a two byte pad of zeros.

b) Write Format Procedure

Provisions must be made within the controller to for-
mat the disc. The following procedure is recommended
for fixed sector formats:

1. Select desired unit, cylinder, head and
   sector.

2. The controller must provide a 5 us minimum
   delay between selecting a head and initia-
   ting a search for leading edge of sector.
   This delay will ensure that the unit will
   be ready to write when the sector leading
   edge is detected.

3. Search for leading edge of desired sector.

FIXED SECTOR

INDEX/SECTOR			N IDENTICAL SECTORS						INDEX/SECTOR
BEGIN RECORD 7 BYTES	PLO SYNC 7 BYTES	*ADDRESS 8 BYTES	WRITE SPLICE 1 BYTE	PLO SYNC 7 BYTES	SYNC PATTERN 1 BYTE 00000001	* DATA	* CRC 2 BYTES	EOR PAD 1 BYTE	END OF RECORD 3 BYTES

SYNC PATTERN 00000001	FLAG STATUS & LOGICAL UNIT	UPPER CYLINDER	LOWER CYLINDER	HEAD	SECTOR	CRC	CRC
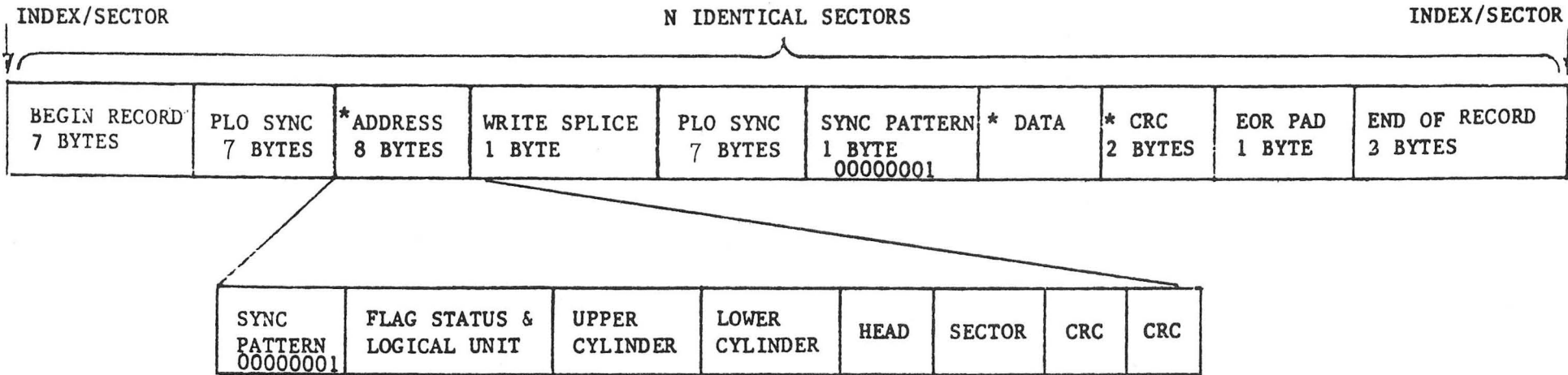
EXAMPLE NO. 1:   WHAT IS DATA FIELD LENGTH USING 64 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - \text{(SYNC FIELDS, TOLERANCE GAPS, AND ADDRESS)}$$

$$\text{DATA FIELD} = \frac{20160}{64} - 36 = 279 \frac{\text{BYTES}}{\text{SECTOR}}$$

DATA = 279 BYTES/SECTOR

$$\% \text{ EFFICIENCY} = \frac{279 \times 64}{20160} \times 100 = 88\%$$

* THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

FIGURE 3-8 FIXED SECTOR FORMAT

INDEX	N IDENTICAL SECTORS									INDEX	
BEGIN RECORD 7 BYTES	AM 3 BYTES	PLO SYNC 7 BYTES	ADDRESS 8 BYTES	WRITE SPLICE 1 BYTE	PLO SYNC 7 BYTES	SYNC PATTERN 1 BYTE	DATA	CRC 2 BYTES	EOR PAD 1 BYTE	END OF TRACK 2 BYTES	BEGIN RECORD 6 BYTES

SYNC PATTERN	FLAG STATUS & LOGICAL UNIT	UPPER CYLINDER	LOWER CYLINDER	HEAD	SECTOR	CRC	CRC

III-22
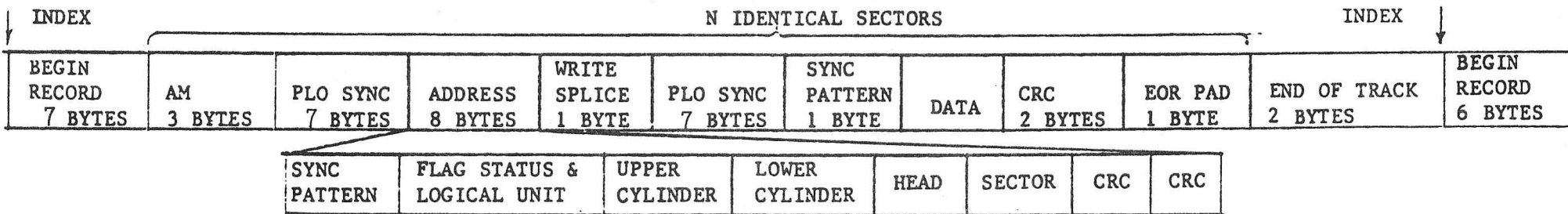
EXAMPLE NO. 1:   WHAT IS DATA FIELD LENGTH USING 64 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK} - \text{MECHANICAL TOLERANCES}}{\text{NUMBER OF SECTORS/TRACK}} - (\text{SYNC FIELDS AND ADDRESS})$$

$$\text{DATA FIELD} = \frac{20160\frac{\text{BYTES}}{\text{TRACK}} - 9\frac{\text{BYTES}}{\text{TRACK}}}{64\frac{\text{SECTORS}}{\text{TRACK}}} - 30\frac{\text{BYTES}}{\text{SECTOR}} = 284\frac{\text{BYTES}}{\text{SECTOR}}$$

$$\% \text{ EFFICIENCY} = \frac{284 \times 64}{20160} \times 100 = 90\%$$

EXAMPLE NO. 2:   WHAT IS NUMBER OF SECTORS USING 512 DATA BYTES?

$$\text{N SECTORS } \frac{20160 - 9}{512 + 30} = 37 \text{ SECTORS}$$

$$\% \text{ EFFICIENCY} = \frac{512 \times 37}{20160} \times 100 = 94\%$$

THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

FIGURE 3-9 VARIABLE SECTOR FORMAT

4. Detect leading edge of selected sector.

5. Immediately bring up Write Gate and start writing zeros.

6. Write all zeros for beginning of record and PLO sync areas (14 bytes in sample formats).

7. Write a sync pattern, the address, and the address checkword.

8. Write all zeros for write splice gap and PLO sync field (8 bytes in sample formats).

9. Write a sync pattern, the data field, the two byte data field checkword, and the one byte pad at the end of the checkword. The data field should be written with all ones.

10. The end tolerance gap is the only part of the format where there may be erased areas with no write data.

11. If the next sector of the same track is to be formatted and the head is not de-selected, the Write Gate may be left on. The controller should write all zeros in the tolerance gap.

c) Control Timing (Figure 3-10)

1. Read

The control line associated with a read command is the Read Gate line.

The leading edge of Read Gate forces the phase-locked oscillator to synchronize on an all zeros pattern. For the format described in Figure 3-8, Read Gate should be enabled no later than 56 clock counts after the leading edge of index or sector (7 us); additionally, Read Gate must not be enabled during the head switching time (Refer to Figure 3-10). The sync pattern search may begin 56 servo clocks after the leading edge of Read Gate (7 us).

Data I/O lines may not have valid data until 7 us from leading edge of Read Gate, due to phase-lock synchronizing time.

Ensure that there will be no splice area after Read Gate is brought up.

2. Write Data Field

   The control line associated with a write operation is Write Gate.

   The sector address must always be read and verified prior to writing the data field, except while formatting.

   Writing the data field must always be preceded by writing the PLO sync field and sync pattern.

   The controller must provide a three bit internal delay (approximately 0.3 us) between the trailing edge of the Read Gate signal and the leading edge of the Write Gate signal (see Figure 3-10). This delay will allow for signal propagation tolerances and prevent a possible overlap of the Read and Write Gate in the unit.

   Writing the data field must always be followed by writing the checkword and at least an eight bit pad at the end of the checkword.

   During formatting, Write Gate is raised immediately upon sensing index or sector. During a record update, Write Gate is raised 300 ns after the last bit of an address.

CONTROL
SELECT
(TAG 3)

*SEE NOTE

HEAD SELECT
(TAG 2)

INDEX OR
SECTOR MARK

HEAD
SELECTED
(INTERNAL)

5.0 uS MAX.

READ
GATE

7.0 ± 0.5 uS
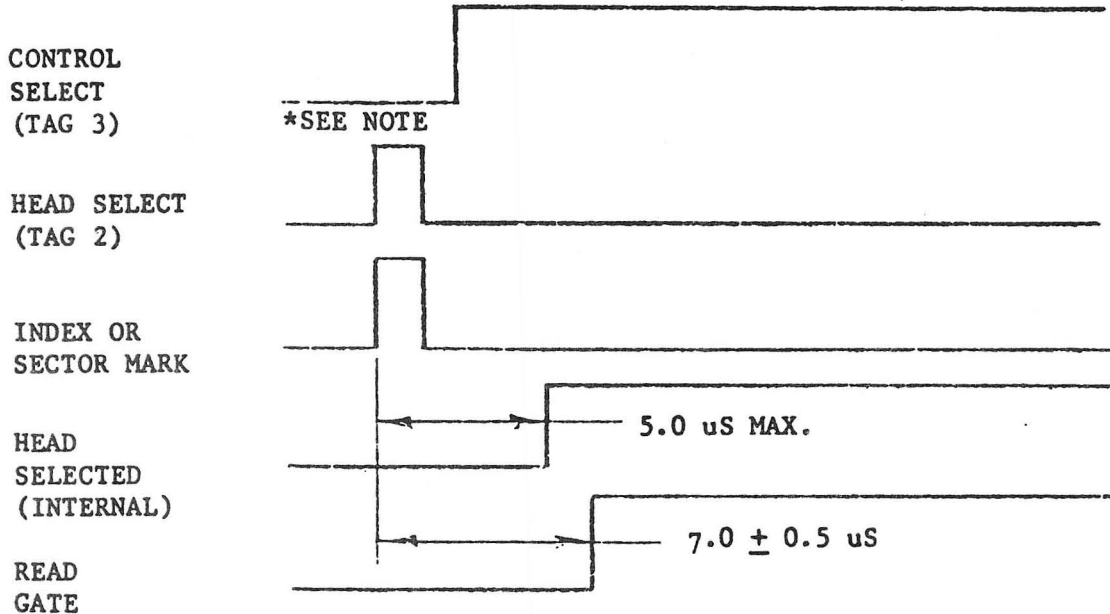
NOTE: READ OPERATION HEAD SELECT MAY NOT OCCUR
        LATER THAN 7.0 uS AFTER INDEX OR SECTOR.
        (with format of Figure 3-8)

TYPICAL READ CONTROL TIMING

CONTROL
SELECT
(TAG 3)

READ ADDRESS

WRITE HEAD GAP,
SYNC PATTERN
AND DATA FIELD

READ
GATE

10 uS MIN

0.3 uS MIN
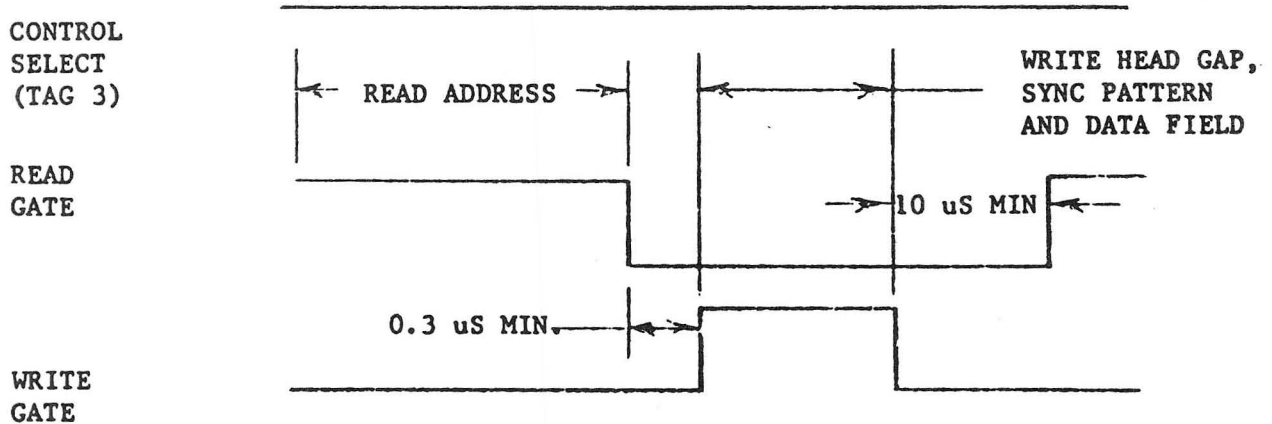
WRITE
GATE

TYPICAL WRITE CONTROL TIMING

FIGURE 11   CONTROL TIMING

III-25

SECTION IV

PRINCIPLES OF OPERATION

4.0 <u>INTRODUCTION</u>

For ease of understanding the principles of oper-
ation of the 3300 disc drive, major functional
groups and associated sub-assemblies are described
separately. The functional separation of the sys-
tem relates conveniently to the actual packaging
of sub-assemblies. The part number of the sub-
assembly and its associated schematic and assembly
drawing, are the same. These drawings are contained
in Section VI, and should be used in conjunction
with this Section to derive complete understanding.

<u>NOTE</u>

Throughout the text, component designators are pre-
fixed with the Page number of the associated sche-
matic, for ease of location of the appropriate circuit.
Logic signal polarity is indicated by the presence or
absence of a bar above the logic term.

4.0.1 The following are the major functional groups and
associated sub-assemblies in the order in which they
are presented:

Functional Group	Sub-Assembly	Part No.
1) A/C Distribution	A/C Distribution	30337
2) Power Supply	Power Supply	30334
	Power Amplifier P.C.B.	30105
	Power Amplifier Assy.	30332
3) Head Positioning Servo	Servo/Logic	30103
4) Data	Matrix	30440
	Fixed Head Amp. (optional)	30104
	Data	30102
5) Interface	Interface (optional)	30115

4.1   AC DISTRIBUTION

The AC Distribution system is shown in Figure 4-1.
The 120 Volt units differ from the 240 Volt units
by different values for the fuses, F1 and F2, the
change of spindle motor, motor start relay and motor
start capacitor. All of these components are located
in assembly P/N 30337. The AC distribution assembly
is located at the left rear of the machine (Fig. 5-36).
The power On-Off switch also changes from 120V to
240 V due to the different lamp voltage required.

When the operator control panel power switch is turned
on, the power supply is energized and the control pan-
el light is lit. Now the brake solenoid is energized
by the power supply.

The switch on the brake solenoid is closed when the
solenoid is energized, closing the spindle motor cir-
cuit. The solenoid is powered by the +32V power sup-
ply. When the brake band is released, a second switch
on the brake band assembly places a dropping resistor
in series with the solenoid to reduce solenoid power
and to hold the brake disengaged.

After brake disengagement, the spindle motor is ener-
gized. A motor start relay connects the start capac-
itor due to the high current in the run winding. The
capacitor and start winding produce a high starting
torque and rapidly accelerate the disc. As the disc
approaches running speed, the start capacitor is
disconnected.

The fan motor is powered by the 115V tap on the power
supply transformer for all line voltage and no changes
are required to adapt the fan to any selectable line
voltage.

A RFI filter is connected to the power line to prevent
line induced noise from affecting disc drive operation.

The main input fuse, F1, protects the AC box, spindle
motor and RFI filter. A second lower current fuse,
F2, is used to protect the power supply from damage.
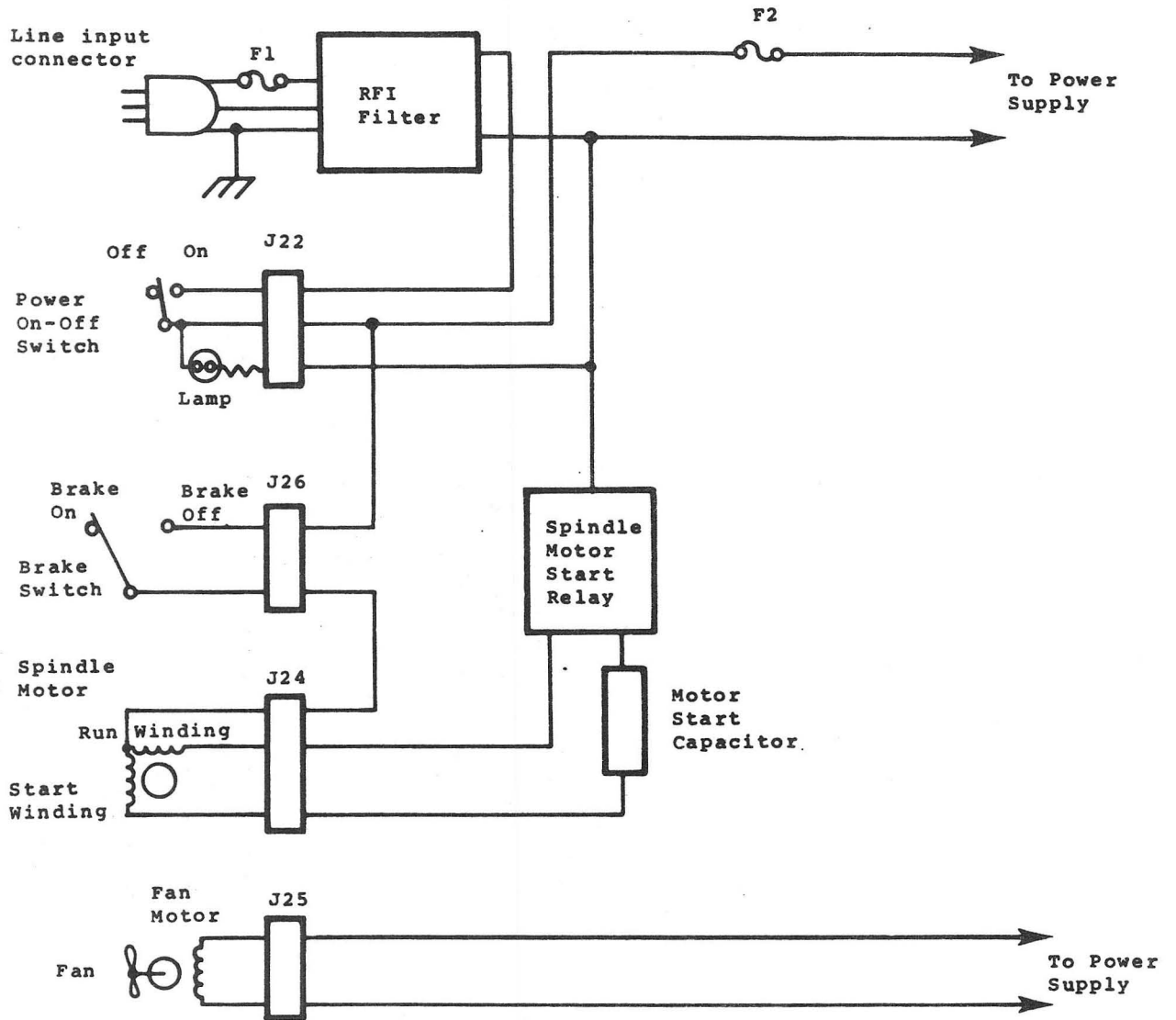
Figure 4-1
A/C Distribution System

4.2   D/C POWER SUPPLY

Figure 4-2 shows the power distribution for the
3300 disc drive system. A detailed diagram is
located in Section VI (Dwg. 30114).
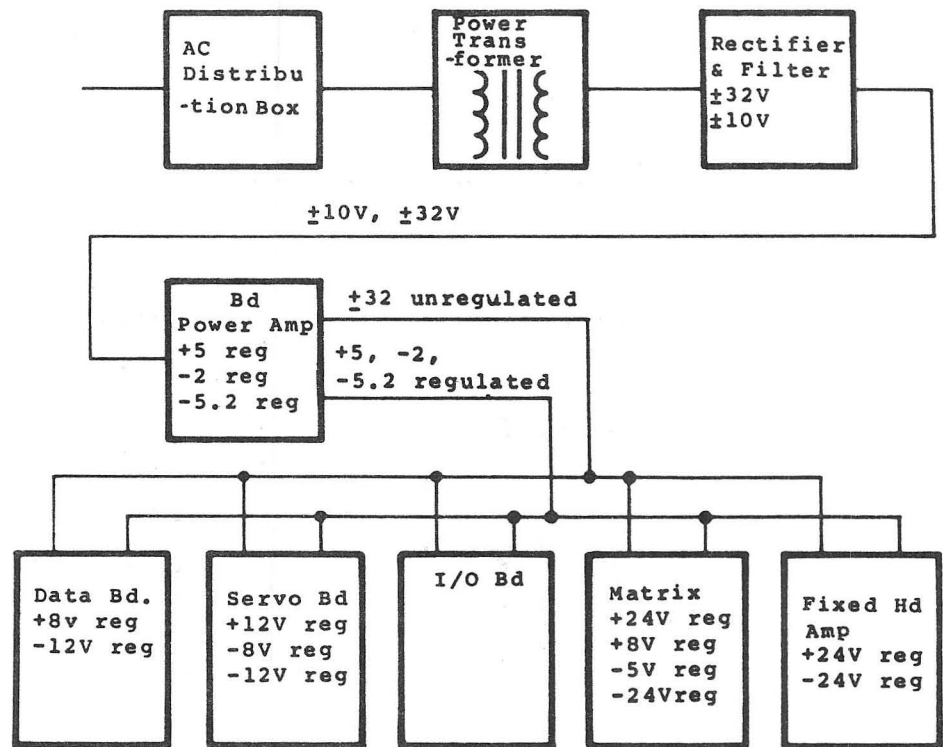
Figure 4-2
Power Distribution

The power transformers, rectifier and filter are
located on the bottom plate of the disc drive
(Fig. 5-3), and comprise assembly P/N 30334.

Figure 4-3 shows the transformer primary wiring
connections required for the 120 vac or 240 vac.
The connections for all transformer taps are listed
on the power supply schematic. The fan is always

powered by the same windings on the power transformer. The power transformers are used as an Auto transformer to power the fan at the same nominal voltage regardless of input line connections.

Simplified Transformer Connection
120V operation

Simplified Transformer Connection
240 Volt Operation
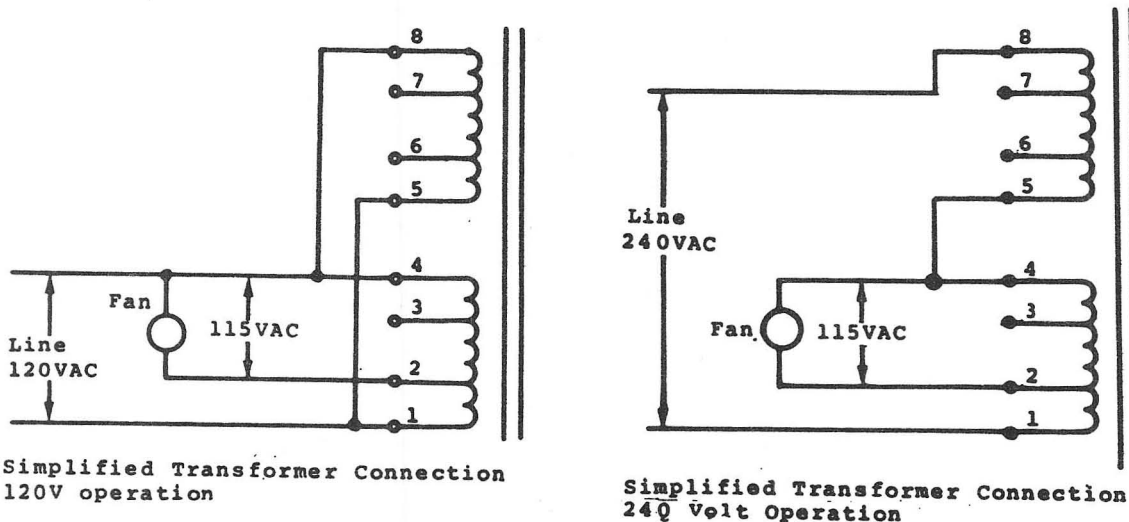
Figure 4-3
Transformer Primary Connections

The transformer secondary is connected as a center tapped full wave bridge circuit. This center tapped circuit produces equal amplitude positive and negative voltages from a single centered tapped secondary. The rectifiers drive a capacitor input filter. Separate transformers are used to produce the nominal $\pm$ 10 volts and $\pm$ 32 volt unregulated outputs. The power wiring harness from the rectifier-filter connects to the power amplifier board.

The power amplifier PC board (P/N 30105) and power amplifier board assembly 30332 are located at the right rear of the drive (Fig. 5-9). The power amplifier board assembly has the series pass regulators for +5 (VDC), -5.2 (VDC) and -2 (VDC) located upon its heat sink.

The control circuitry is on the power amplifier
printed circuit board. The +10VDC unregulated
is regulated to +5.0VDC, and -10VDC unregulated
is regulated to -5.2VDC. The regulated -2VDC is
derived from the -5.2VDC. The -2 volt regulator
is an Integrated Circuit series pass regulator
with all control circuitry in that same package.
The (+32 VDC) unregulated is used to power the
position motor via the control transistors lo-
cated on the power amplifier module. The +32VDC
unregulated is distributed to the remaining P.C.
cards where it is regulated as required. "3
terminal" regulators, like the -2V regulator, are
used with output voltages as required to provide
regulated power. See figure 4-2 for power distribution.

4.3   HEAD POSITIONING SERVO SYSTEM

4.3.1   General

In a moving disc drive, the head positioning system
serves two primary functions:

a) Move the data heads from one cylinder to another
    as demanded at the interface as rapidly as possible.

b) Maintain the location of the heads on cylinder
    as accurately as possible.

The 3300 uses a "Track Following" technique to achieve
these objectives in which a dedicated servo head is
used to generate position information for the system
from the pre-recorded servo tracks located on the
bottom surface of the lower disc (Fig. 4-4).

DATA SURFACE   SERVO SURFACE
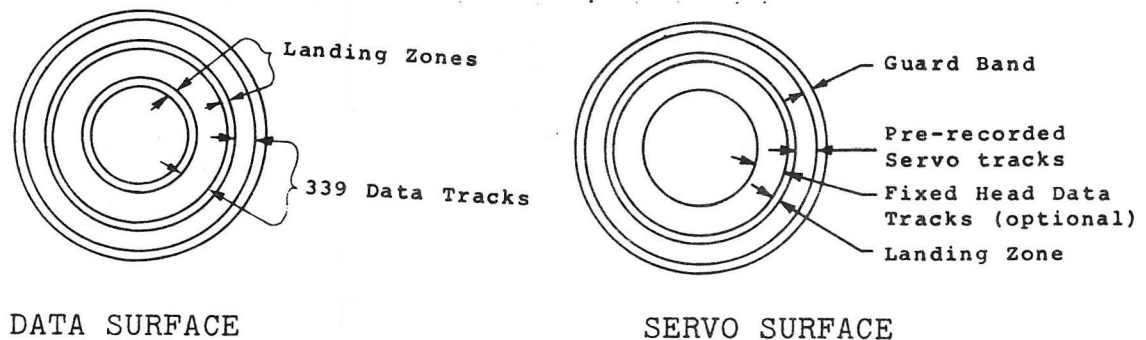
Figure 4-4
Disc Servo and Data Locations
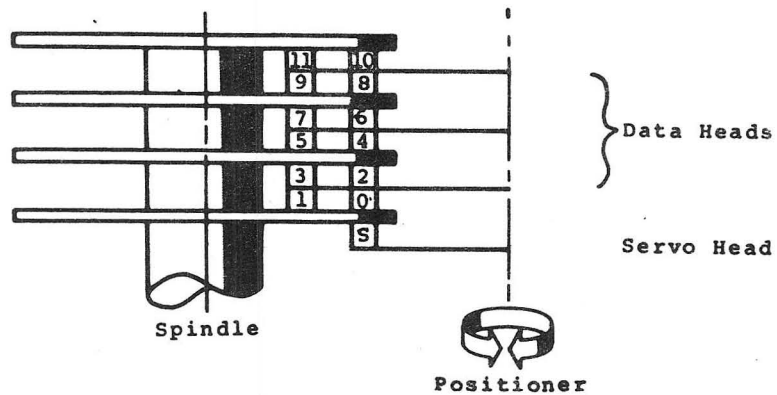
Figure 4-5
Moving Head Positions

As can be seen is Figure 4-5, all the data heads
and the servo head are mounted mechanically to a
common head mount which is attached to the position
arm. Therefore, when the servo head achieves a
particular track position, all data heads also
achieve a corresponding track position. Depending
on the number of heads in the drive, all data tracks
accessed for a given servo head comprise a
"Cylinder".

To achieve its primary objective, the positioning
servo, used in the 3300, operates in two modes:

a. "Coarse" or velocity feedback mode.

b. "Detent" or position feedback mode.

The "Coarse" mode is used to locate the heads as
rapidly as possible over a desired track location.
In this mode, the heads are accelerated as rapidly
as possible to high velocity, and at the appropriate
position they are rapidly decelerated so that
velocity is near zero at the desired track location
(Fig. 4-6).

The "Detent" mode is used to position the heads
accurately over the track location and keep them
there regardless of vibration, thermal effects, etc.
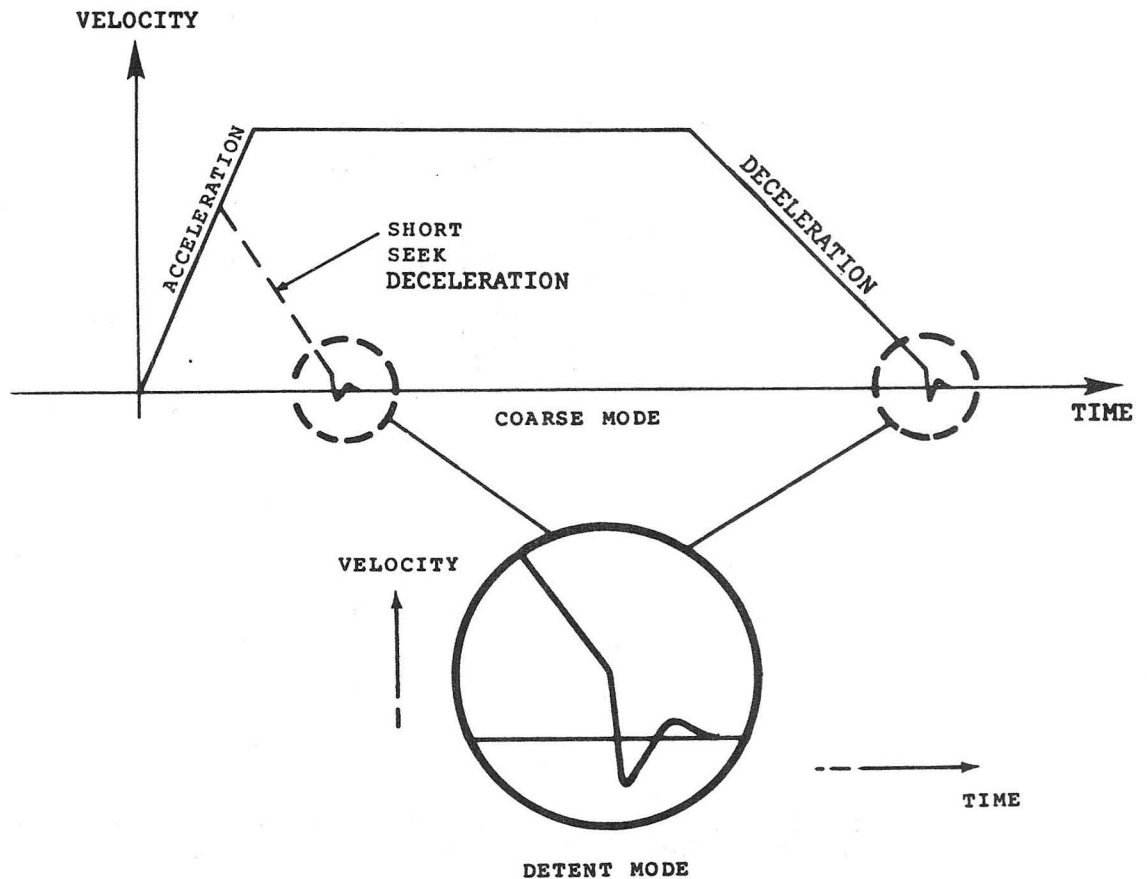
Figure 4-6
Positioner Motion During Seek

The block diagram of Figure 4-7 gives an overview
of the basic functional blocks of the servo system.
The servo system can be divided into four major
blocks: the servo demodulation block, to decode
recorded servo information; the arithmetic section,
to store and process current and requested track
location information; the control section, to
execute requested commands; the servo control section,
to position the servo and data heads to the requested
track location. The circuits associated with these
servo functions are located on the Servo/Logic
board (P/N 30103).

4.3.2   Servo Head Signal

The servo track information is pre-recorded as
shown in Figure 4-8. The servo disc is written in
alternating bands of "A" and "B" tracks except in
guardband, where a modified "B" track pattern
is written. The upper track of Figure 4-8 shows

IV-8
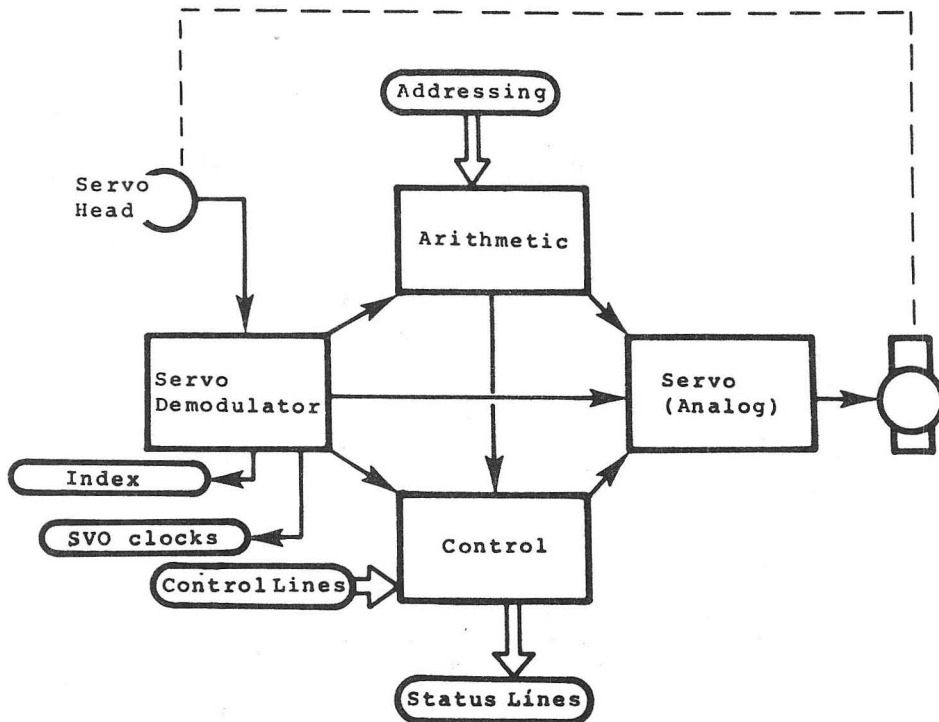
Figure 4-7
Servo System Functional Diagram

the electrical signal when the servo head is
directly over an "A" track. The positive going
portion of the signal is referred to as a "Sync
Pulse"; the negative going portion is referred to
as a "servo pulse".

When directly on track "B", the head signal is the
same as when on track "A", except for the time
relation between the sync and servo pulses. An "A"
track servo pulse is about 1/3 of a time period
from the sync, whereas the "B" track servo is about
2/3 of a time period from the sync pulse.

Figure 4-8 shows the servo head signal when the
head is between an "A" and "B" servo track, and
what happens to the signal as the servo head
moves toward an "A" or "B" track. The "A" servo
bit reduces in amplitude as a "B" track is
approached and at the same time, "B" track servo
bit increases in amplitude. The opposite occurs
as an "A" track is approached.

IV-9

SYNC PULSES

SERVO PULSES

On
"A"
Servo
Tracks

Near "A"

On
Data
Track

- - → Normal Pattern → ← Index Decoded Here → ← Normal Pattern — - -

Near "B"

On "B"
Servo Track

Guard Band
(no index)
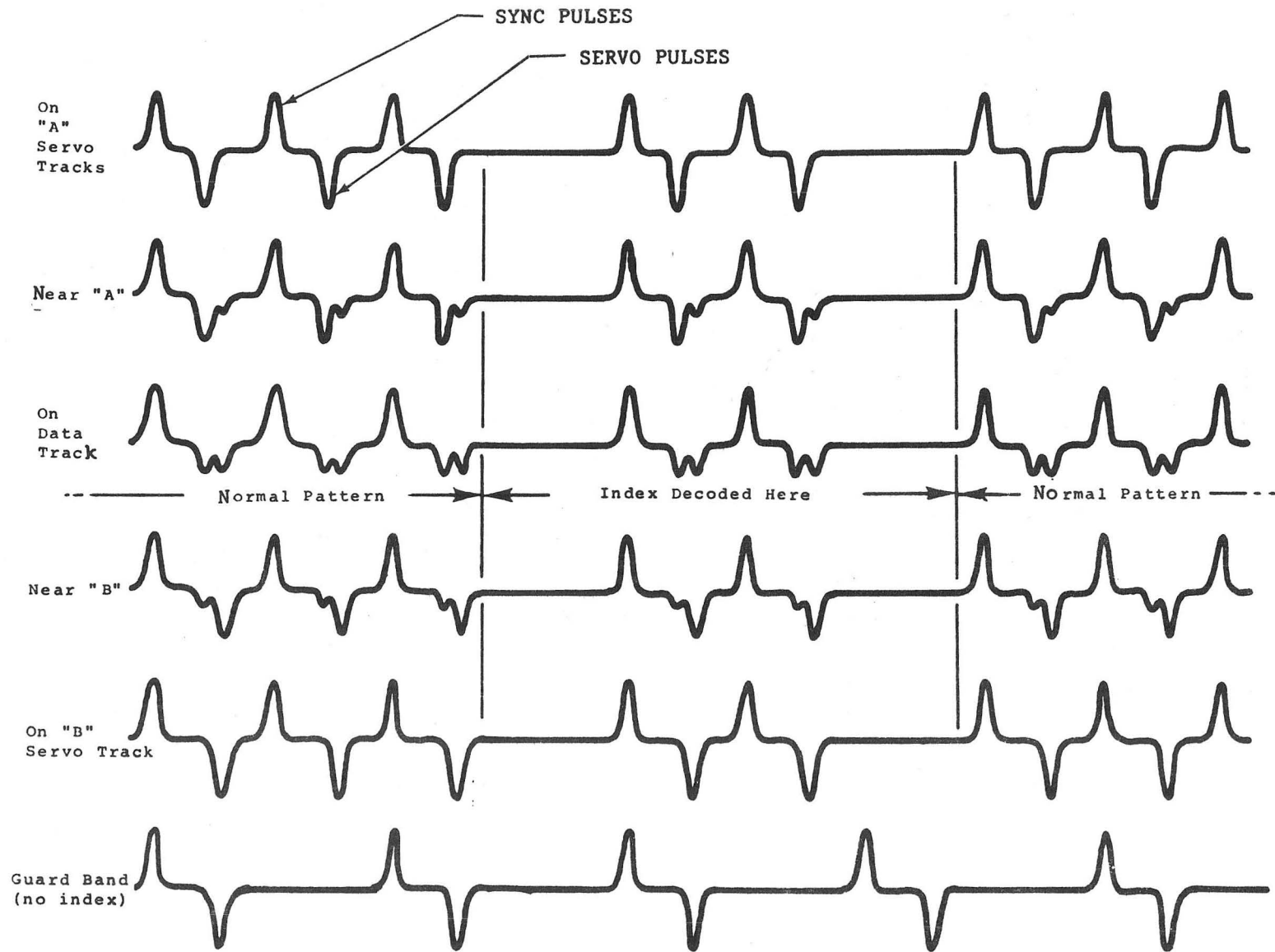
Figure 4-8
Servo Head Signal

The sync bits on "A" and "B" tracks are written in the same time position on both "A" and "B" tracks. When the servo head is moved between an "A" to a "B" track, the signal from the "A" track decreases and the signal from "B" track increases an equal amount, so the servo head signal, which is the sum of the two track signals, stays the same. The servo head signal in guardband consists of a modified "B" signal on every track with alternate bytes dropped. The dropped bytes are decoded to detect the term "GUARDBAND" (Fig. 4-8).

The index pattern is a four byte pattern repeating once per track revolution. This pattern is coded by the deletion of a byte, composed of a sync and servo bit, insertion of two bytes, and deletion of a byte. This pattern is written once per revolution and its angular position is constant, regardless of track location (Fig. 4-8).

The "B" track index pattern is the same as recorded on an "A" track.

4.3.3.   Servo Head Signal Processing (Servo Demodulator)

Figure 4-9 shows a block diagram of the process of decoding the servo track information. The head has an "on-board" preamplifier (contained within the disc enclosure) to improve signal-to-noise ratio and reduce noise pickup. The preamplifier requires ground and -8V for power and has a push-pull output signal.

The servo head preamplifier is terminated at the input to the servo board (P/N 30103). Integrated circuit 1U4 and FET 1Q1 form a variable gain amplifier. The variable gain amplifier drives a low pass filter to limit the band width to that required to pass the information recorded on the servo track and reduce the unwanted noise outside the bandwidth of interest.

The filter drives a discrete component amplifier 1U9 and is buffered by emitter follower 1U10, whose output is AC coupled to the sync and servo separator circuits. Transistor 1Q2, 1CR9 let the positive going sync pulses pass and clamp off the servo pulses. Comparator 1U6 threshold detects the sync pulses. Hysteresis is added to prevent triggering due to noise.
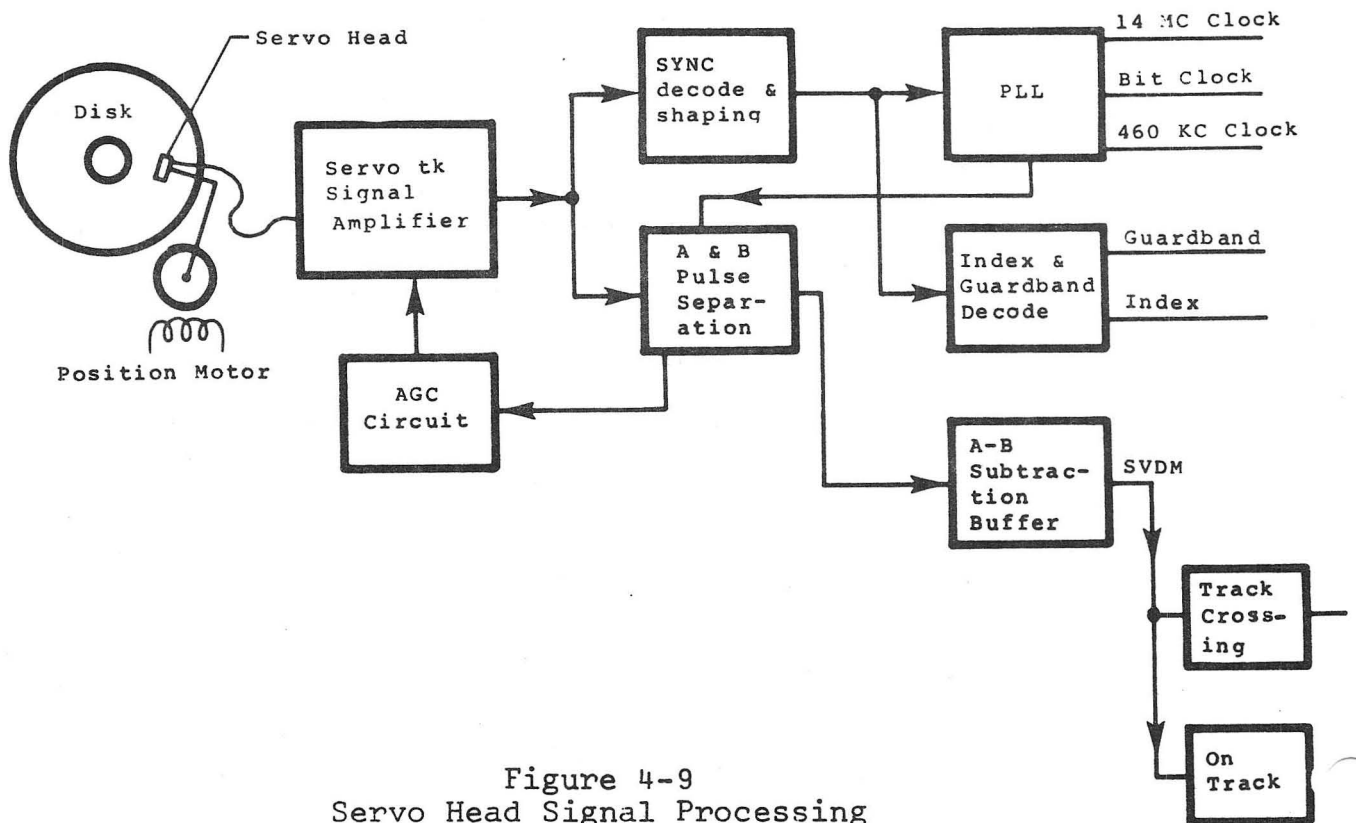
Figure 4-9
Servo Head Signal Processing
(Servo Demodulator)

The sync pulses are formed into a squarewave signal
by one-shot 1U7 to produce terms SYNC and $\overline{SYNC}$.
Figure 4-10 shows the timing for servo processing.

The term SVODATA is generated by 1U11. SYNC sets
1U11 and "T" time T_{10} resets 1U11 part 1. ("T" times
are generated by a phase locked loop to be covered
later.) As shown in Figure 4-10, SVODATA is a
waveform whose pulse width is a function of the
phase error between sync and time T_{10}. Figure 4-10
shows the waveform SVODATA for normal, early, late
and missing SYNC PULSE. SVODATA is used to drive
1U11 part 2, in the absence of a sync pulse, as
shown in Figure 4-10. If SVODATA is low, 1U11 part 2
(SO) is clocked by the phase locked loop to record
all missing sync pulses as logic level zeros.
1U28 is a four stage shift register. The presence or
absence of a sync pulse is shifted through this
register. The bit pattern in the four shift registers
is monitored to decode index and guardband (refer to
4.3.4).
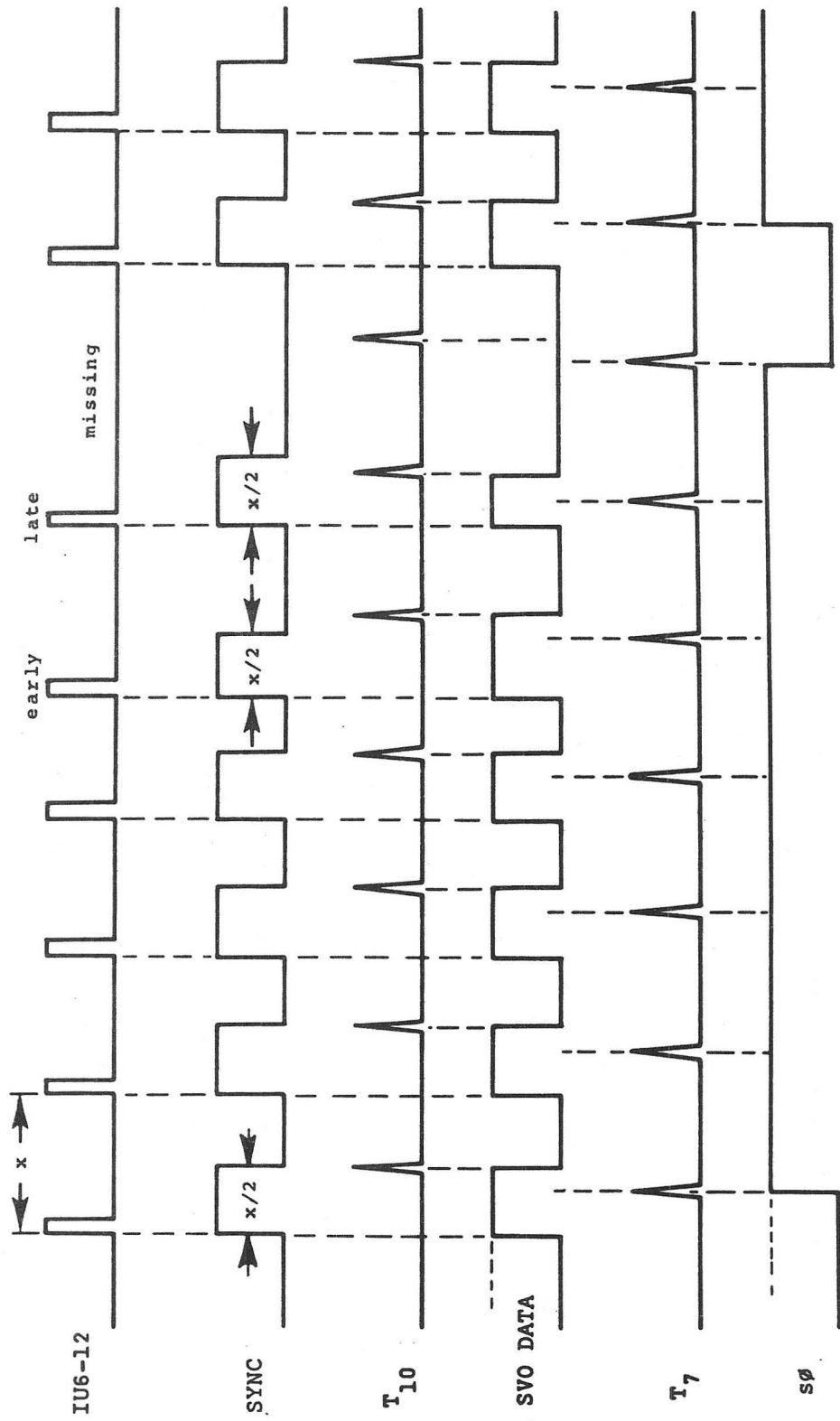
Figure 4-10
Phase Lock Timing
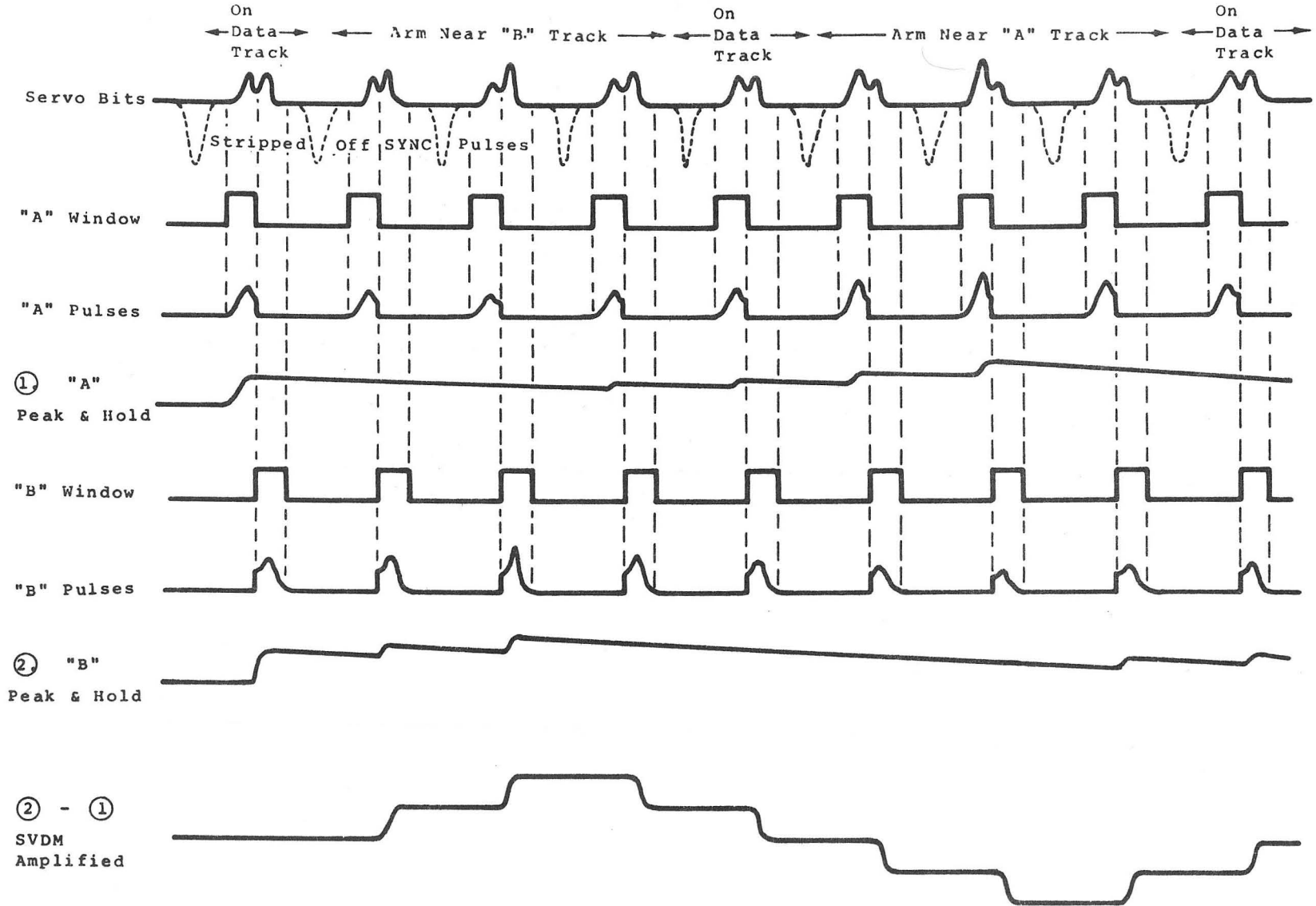
Figure 4-11
Servo Demodulated Signal (SVDM)

The phase locked loop (PLL) is locked to the sync pulses on the servo disc. To avoid disturbance of the PLL during an index or guardband pattern, when sync bytes are deleted, and the possible occurrence of a defect in the media dropping the sync bit, the loss of a sync bit must also result in the loss of a SVODATA bit. As covered above, 1U11 is clocked on by SYNC and off by phase locked loop "T" time T_{10}. (See Fig. 4-10). At the time of the missing sync bit, SVODATA also deletes a bit so both the reference signal 1U29-2 and the variable signal 1U29-6 have the same frequency and phase. This circuit assures that no change in the error amplifier signal and no disturbance fo the PLL occur.

The PLL used can lock up in harmonic modes, if not prevented. Diode 1CR11, resistors 1R101 and 1R52 hold the VCO 1U8 frequency high until disc speed, which determines sync pulse frequency, is sufficiently high to allow correct phase lock.

The phase detector 1U29, 1R45, 1R47, 1C22 and 1C23 average the waveforms of SYNC and SVODATA. Any phase error between 1U29 pins 2 and 6 results in unequal amplitudes on 1C22 and 1C23. Capacitors 1C22 and 1C23 amplitudes are subtracted and amplified by error amplifier 1U12. This error signal is fed to voltage controlled oscillator (VCO) 1U8 and the phase is corrected until no phase error exists. The VCO runs at 32 times the sync pulse frequency. The VCO has adjustments to set the minimum and maximum frequency of oscillation.

The flip-flop 1U37 divides the frequency by 2. This signal goes to the divide by 16 counter 1U21. The counter output is decoded by 1U20 and 1U19 to have 16 "t" times lasting 1/16th of the period between sync pulses.

Integrated circuit 3U37 part 2 is used to check for a frequency error between SYNC and SVODATA signals. Any error will disable the positioner motor and set a fault on "Seek Late".

The one-shot 3U47 detects any continuous loss of sync and if faulted, will set "Seek Late" through the phase lock detector, 3U37 part 2.

The servo position information pulses from tracks A and B are separated from the analog the same as were the sync pulses. 1Q3, 1CR10 clamp off the sync pulses.

To separate the "A" pulses from the "B" pulses, the
timing signals from the PLL are used, as shown in
Fig. 4-11. "A" pulses are recovered by opening a
"window" during the time position when "A" pulses
are expected. "B" pulses are separated exactly the
same way at the "B" time window. Times T2 and T6
open and close the "A" window gate 1U17 pin 12.
Times T8, T12 open and close the "B" window gate
1U17 pin 7.

1U16 pin 2, 1U15 sample and hold the peak value of
"A" pulses. 1U16 pin 12, 1U14 sample and hold the
peak value of "B" pulses.

The sum of the peaks of the "A" and "B" pulses are
held at a constant amplitude by the automatic gain
control (AGC) circuitry.

The input to 1U1 sums the peak of the "A" and "B"
sampled pulse. Potentiometer 1R1 sets the reference
level for AGC amplitude, 1CR1 is for temperature
compensation.

Any error between the "A" and "B" pulse amplitude
sum and the reference potentiometer is amplified by
1U1 and adjusts the gain of the input amplifier by
FET 1Q1.

The FET 1Q1 is a variable gain shunting resistor used
to adjust the actual signal level produced by the
servo head preamplifier.

The peak values of "A" and "B" pulses at any servo
head position are subtracted by 1U13 to demodulate
the recorded servo information (SVDM). Resistor 1R56,
or 1R79 is used to correct for offsets due to unequal
amplitude of "A" and "B" pulses. The servo-demodulated
signal (SVDM) is a nearly sinusoidal representation of
head position, and is used to derive position, velocity
and acceleration feedback for the servo system as well
as to count track crossings, etc.

4.3.4   Index and Guardband

Figure 4-12 shows the timing and decoding of index
and guardband signals. SVODATA is clocked by time T7
and shifted through shift register S0-S4. A 0110
pattern is for index and is decoded by 1U43 ignoring
S4. Gates 1U35, 1U36 decode patterns 01010 and 10101
to produce a nearly continuous high signal in
guardband signal and a continuous low signal when
out of a guardband.

4.3.5   Track Crossing Pulses (TCP)

The track crossing detectors monitor SVDM to detect
motion of the servo head while positioning across
servo tracks. Figure 4-13 is a timing diagram of the
track crossing detector circuits. SVDM input signal
is filtered by 4C131 and 4C132 to prevent noise
pulses from triggering the track crossing detectors.

Amplifier 4U89 inverts SVDM to generate $\overline{SVDM}$. Inverted
positive track crossing pulses ($\overline{PTCP}$) are derived from
$\overline{SVDM}$ and threshold detected by 4U83 pin 4 and inverted
by 4U85 to produce inverted positive track crossing
pulses ($\overline{PTCP}$). In the same manner SVDM is used to
produce inverted negative track crossing pulses
($\overline{NTCP}$). Inverted track crossing pulses ($\overline{TCP}$) are
produced by the logical "and" of $\overline{PTCP}$ and $\overline{NTCP}$
by 2U47.

"Ontrack" differs from TCP only by the threshold
level of the on track detectors (see Fig. 4-13).

4.3.6   Illegal Address

Illegal Address is part of the arithmetic logic
section and is used to verify if the demanded
address is within range of the disc drive unit.
Figure 4-14 is a flow chart of the illegal address
section.

Integrated circuits 2U66, 2U65, 2U47 test for valid
address, if the address is valid 2U47 gate will be
enabled and latches 2U67, 2U76, 2U75 will be receptive
to a Seek Strobe. If invalid address present 2U47
gate will not allow Seek Strobe to latch in a new
address.
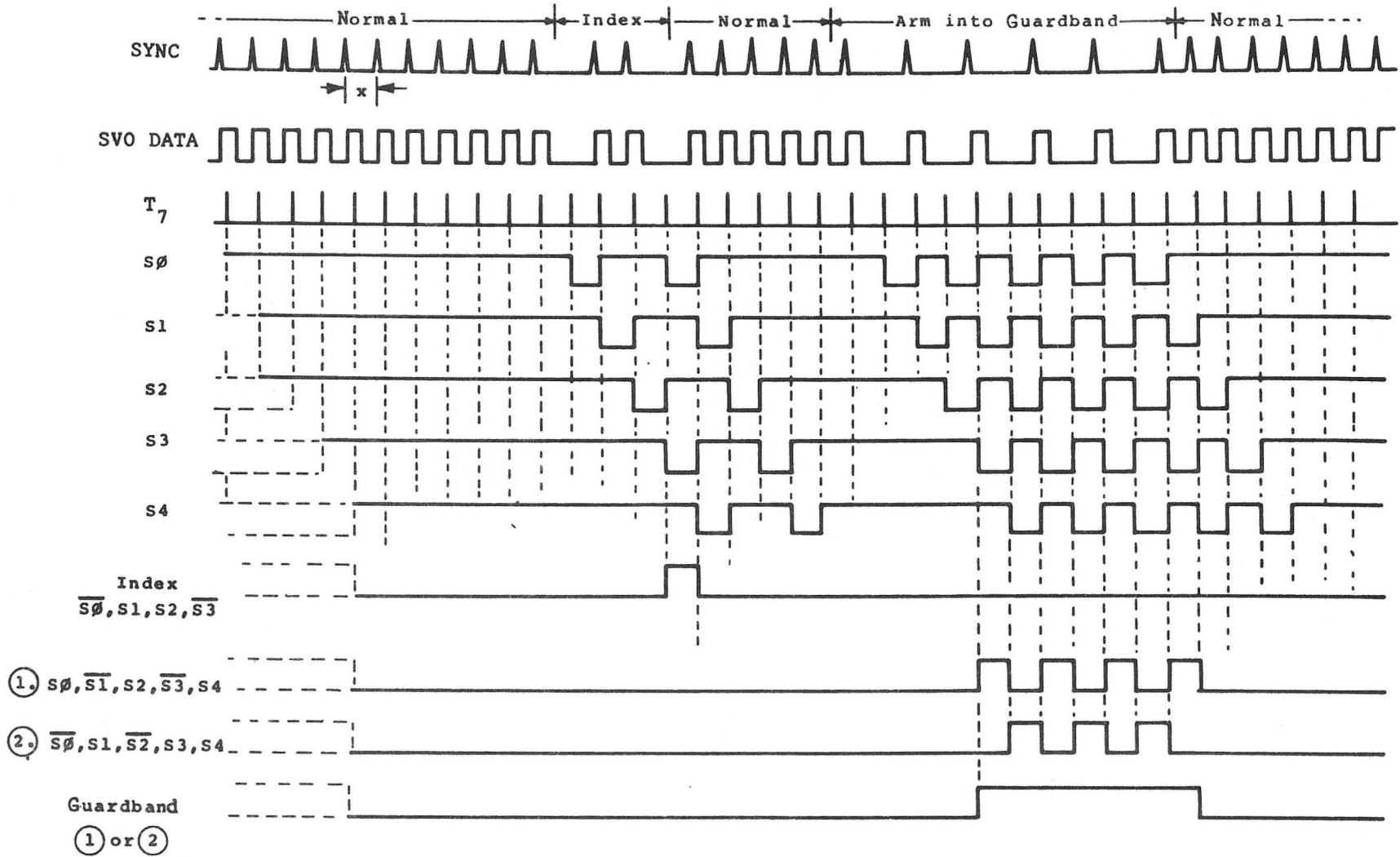
Figure 4-12
Index & Guardband Decoding
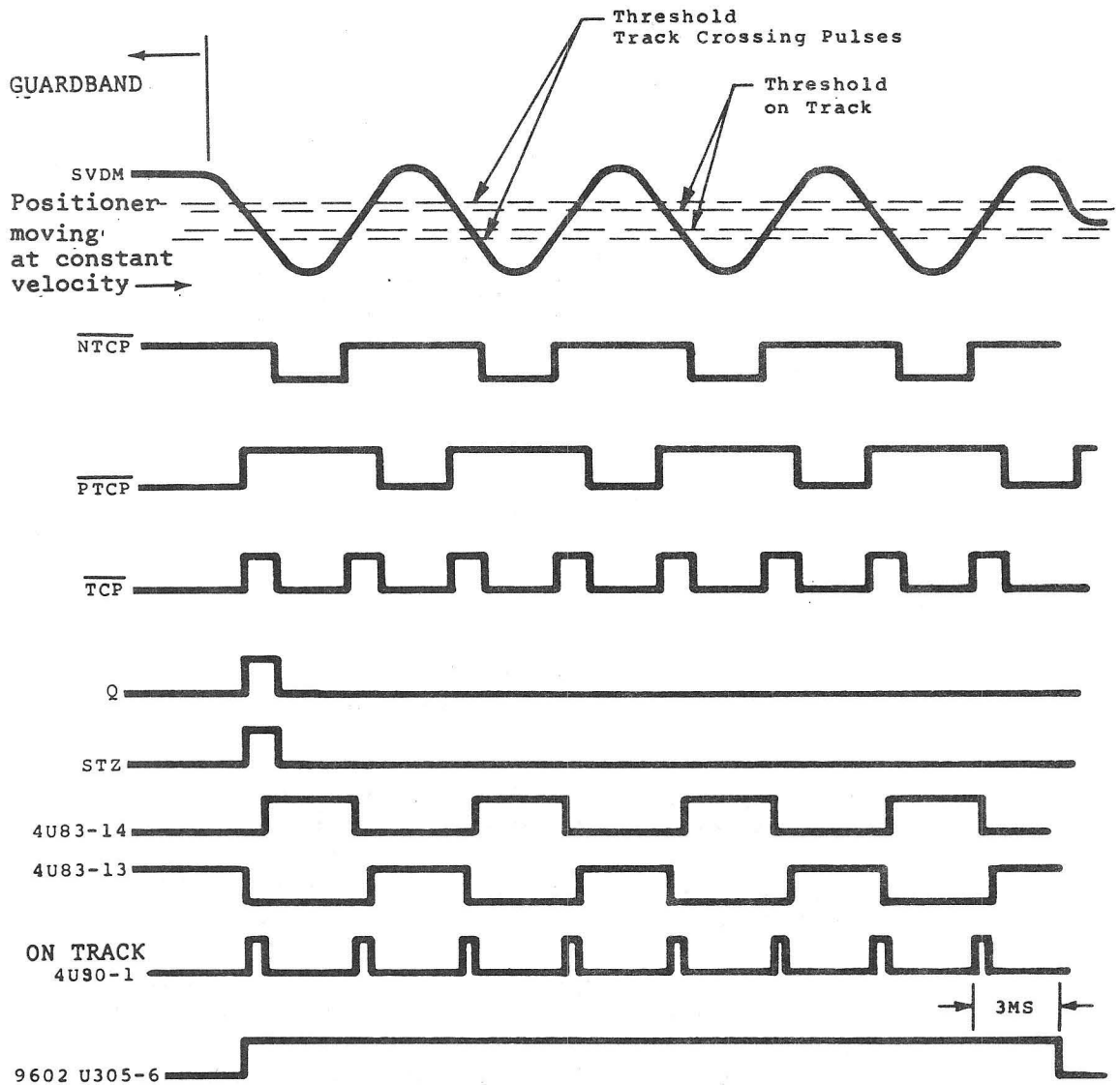
Figure 4-13
Track Crossing Detector
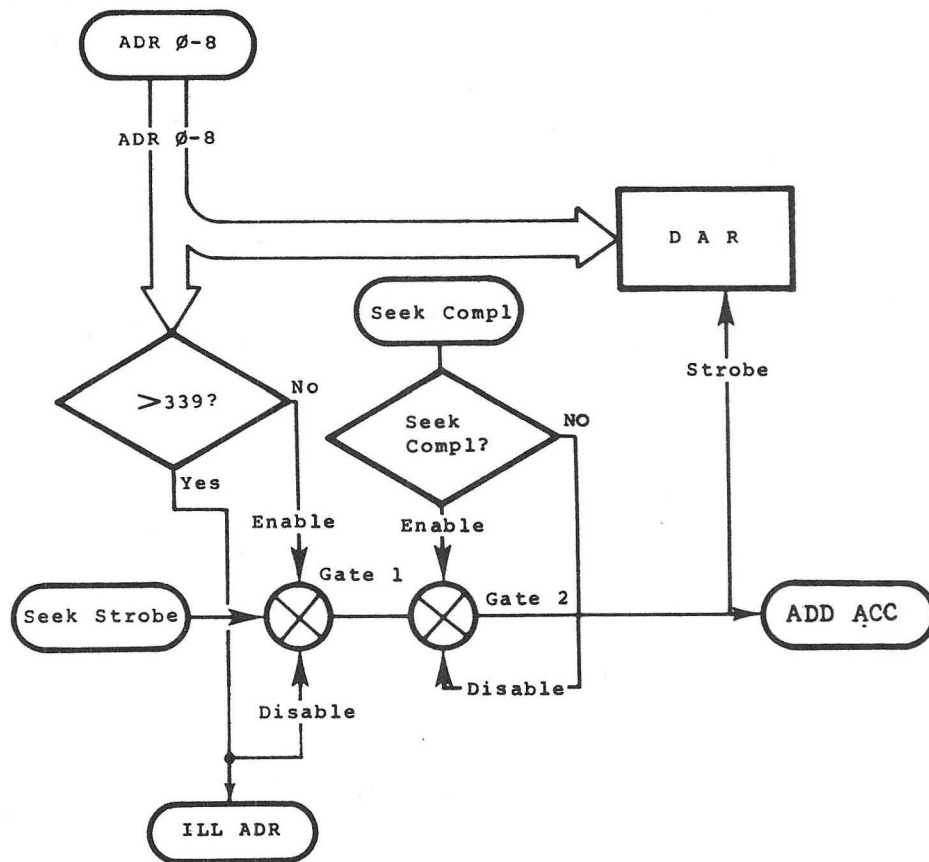
Figure 4-14
Illegal Address

Seek Complete (SEEK COMPL), a term yet to be covered,
is false unless the current seek is complete and will
disable a new seek strobe until the present seek is
complete. See 4.3.7 for complete information on
Seek Complete.

In summary, if legal address and seek complete are
present a new address is latched in the Demand Address
Register (DAR) and is acknowledged by a pulse from
3U31. If either the present seek is not complete or
an illegal address is present the strobe to the DAR
is blocked. If an illegal address is present during
a Seek strobe, 2U69 sets the illegal address line
and a restore must be commanded to clear the illegal
address status line.

4.3.7   Seek Cycle Logic

Figure 4-15 outlines the flow chart of a seek
cycle. The successful strobing of a new demand
address starts a new seek cycle. When the DAR does
not equal the current address register (CAR),
2U63, 2U55, and 2U72, the servo drops from position
mode (Detent) and into velocity mode (Coarse). At
the same time, the 1's complement adder, 2U64,
2U56 and 2U73 determines the direction the arm must
move. If DAR is greater than CAR, a command is issued
to move forward toward disc center, and the CAR is set
to count up at each $\overline{TCP}$ signal. If CAR is greater
than DAR, a command is issued to move reverse toward
the disc edge, and the CAR is set to count down at
each $\overline{TCP}$. The CAR is counted up or down until CAR
equals DAR, then the difference equals zero gate
2U53, 2U52, 2U65 holds the CAR and changes the
servo system to the position mode to detent between
servo tracks where data is to be read or written.

To detent, DAR is checked to determine if the DAR
was odd or even, the least significant DAR bit
determines the sign.

Figure 4-16 shows the SVDM change of sign as a
function of odd or even tracks. Even tracks have a
negative slope and odd tracks have a positive slope.

Once detent is completed the servo head is held
between "A" and "B" servo tracks and ontrack stays
true. Inverted on track delayed ($\overline{ONTRKDLY}$) one-shot
3U27 times out, clocking seek complete (SEEK COMPL)
flip-flop 3U48 and setting SEEK COMPL true.

4.3.8   Restore Logic

The flow diagram for a restore cycle is blocked out
in Figure 4-17. When a restore command is issued
3U31 and 3U24 form a restore pulse (RESTOREP).
RESTOREP sets 3U58 to the slew mode (SLEW) and 3U59
to inverted Seek Complete inhibit mode ($\overline{SKCPLI}$).

Slew is done with the servo system in velocity mode.
The velocity is constant and slow. 4R213 sets the
slew velocity. Slew moves the servo head to guardband.
When guardband is entered 3U50 flip flop is set, starting

Figure 4-15
Seek Cycle

Guard Band

+

0

−

Near "B" Track

Centered Between "A" & "B" Tracks

Near "A" Track

Trk #0   Trk #1   Trk #2   Trk #3   Trk #4   Trk #5   Trk #6   Trk #7
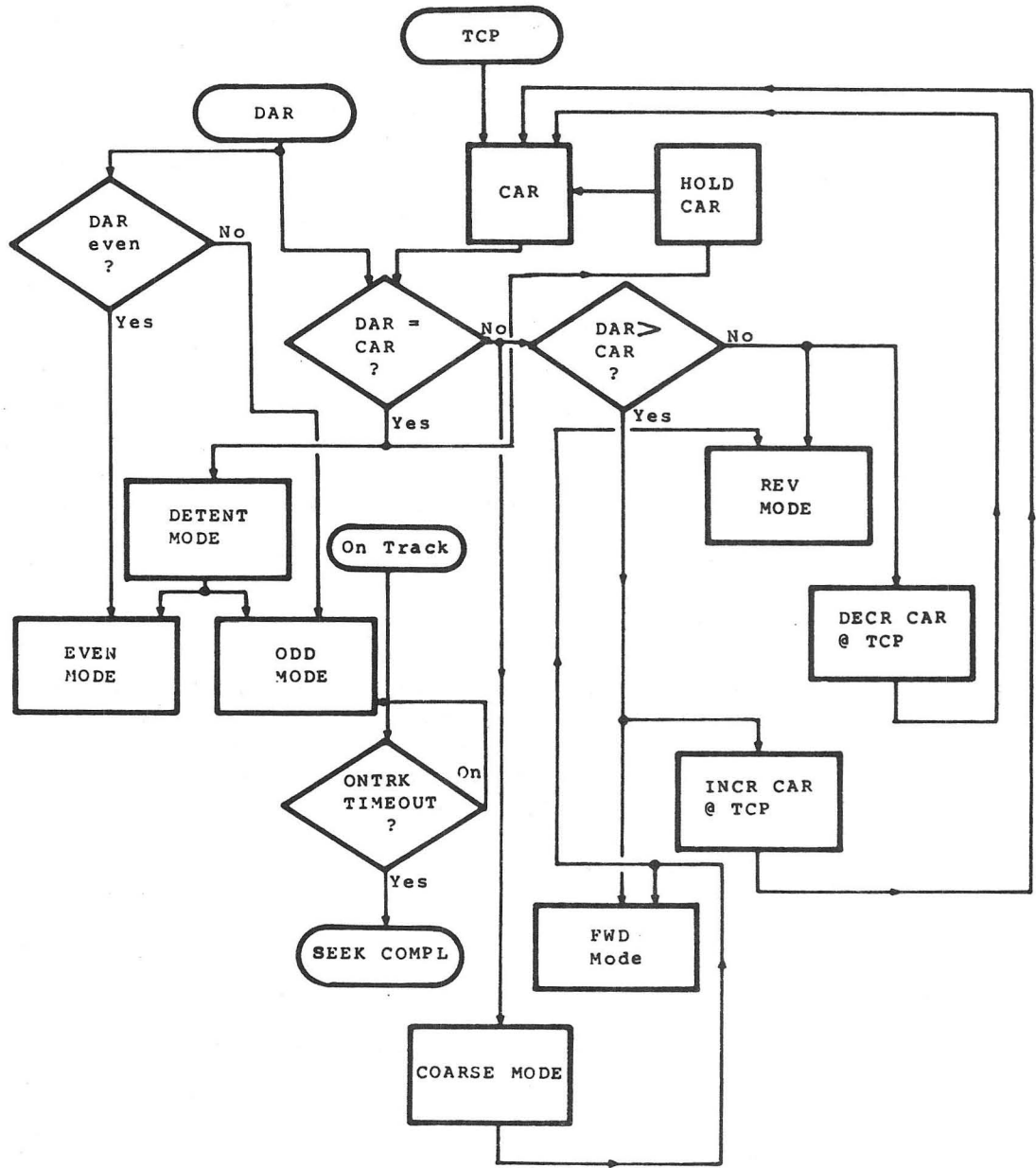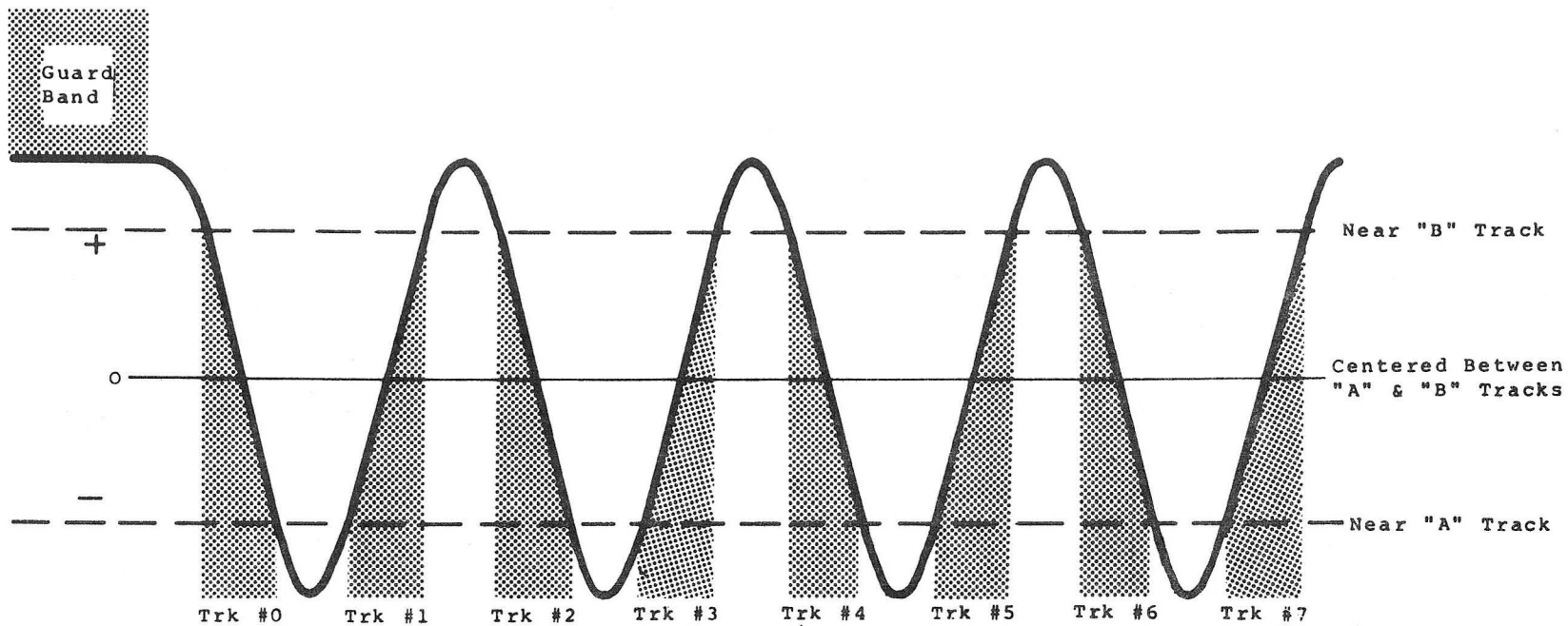
Positive Slope On Odd Track

Negative Slope on Even Track

Figure 4-16
Servo Demod. Change of Slope
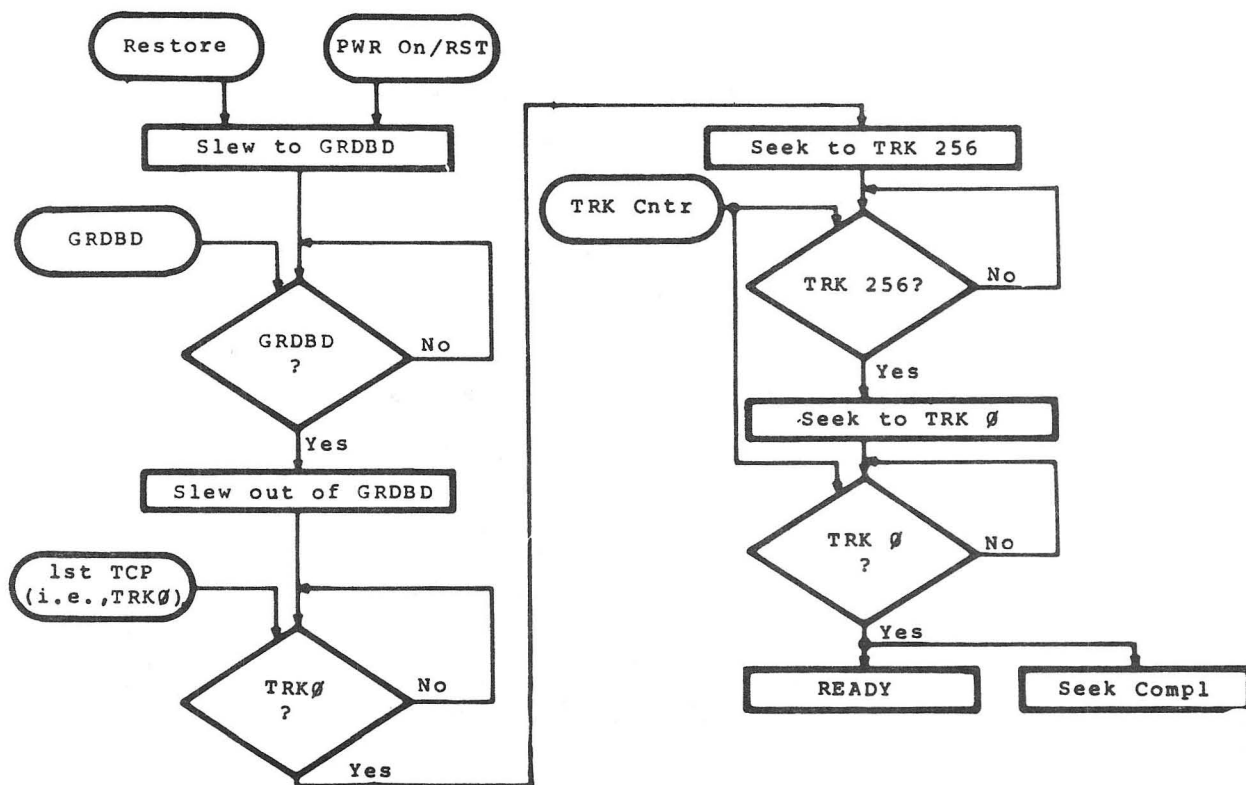
Figure 4-17
Restore Cycle

arm to slew forward out of guardband. Flip flop
3U50 is armed to detect the first $\overline{PTCP}$. This is the
prime purpose of the guardband signal. When the first
$\overline{PTCP}$ is detected 3U50-11 is set giving an inverted
store zero command ($\overline{STZ}$). $\overline{STZ}$ sets both the CAR and
DAR to zero. SKCPLI locks a 256 track seek command
directly to adder circuitry through 2U60.

A standard seek is done to reach track 256. After
detenting on track 256 long enough to time out
$\overline{ONTRKDLY}$, $\overline{SKCPLI}$ is set high by $\overline{ONTRKDLY}$ and 2U60
now feeds DAR bit 8 to the adder circuits. DAR was
loaded with zeros by $\overline{STZ}$ and so the servo does a
normal seek to track zero. SEEK COMPL is set true
and the ready line is set true.

IV-24

4.3.9   Velocity (Coarse) Mode Servo

The head velocity is derived from SVDM. SVDM is
differentiated by 4C130 and operational amplifier
4U94. Operational amplifiers 4U82 and 4U81 form a
full wave rectifier bridge to rectify the rate of
change of SVDM. The rectified signal has a value
that is proportional to servo head velocity.

When in position mode, the differentiated SVDM
represents velocity and is used as a compensation
term to cancel the time lag caused by inertia
inherent in the system.

Field effect transistors (FETs) are used as switches
to select proper terms into the feedback loops. A
high level signal, +5v to +12v, will deplete the
channel and shut off the device. A voltage near zero
will form a channel and allow conduction. FETs 4U93
are FET switches that gate the proper velocity term
during velocity and position modes.

Derived velocity is not direction sensitive and di-
rection must be derived from CAR and DAR and the
proper sign added. Operational amplifier 4U88 uses
a FET switch to control an amplifier whose gain can
be either +1 or -1. With the FET switch on a -1 gain
amplifier is made. With the FET off a source follower
of +1 gain results.

When the servo system is in velocity mode, the program-
mable read-only memory (PROM), 2U61 stores the desired
velocity profile as a function of tracks to go as com-
puted from CAR and DAR. Above 64 tracks from the final
track destination, all PROM outputs are forced true by
2U25. Upon reaching a track difference of 64, the PROM
is active, digitally producing the desired deceleration
profile. The digital to analog converter (DAC) 2U70
converts the digital information to the desired analog
velocity profile. Access time Pot, 2R157, adjusts the
DAC analog output voltage to control actual head veloc-
ity in the coarse mode. Desired velocity is constant
when more than 64 tracks from desired track and a modi-
fied square root function for less than 64 tracks to go.
The square root function is used to provide constant de-
celeration to the desired track. The final velocity is
set by last track move resistor 4R205. Figure 4-18
shows the desired head velocity for > 64 track moves, at
64 tracks and < 64 track moves.

>64 tks   64 tks <64 tks On Track

Desired Velocity Generated by DAC
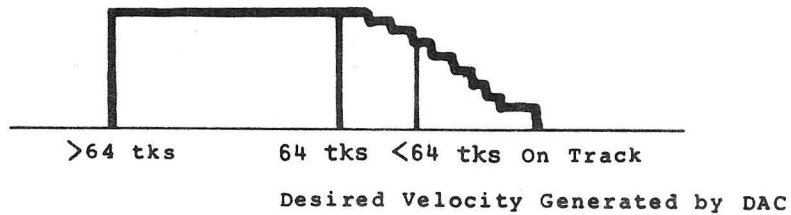
Figure 4-18
Desired Velocity Generated by DAC

Figure 4-19 shows the actual head velocity as a
function of tracks to go. The system inertia and the
positioner motor protecting current limit prevent
instantaneous following of the desired velocity
profile. At a large distance from the last track
to go, the system is tolerant of large errors in
actual velocity. When near the last track to go,
the feedback loop is in control and desired
velocity is a good match to actual velocity.

> 64 Tks   64 Tks <64 Tks On Track

Actual Velocity of Servo Arm
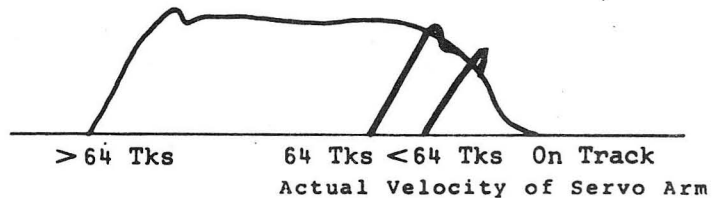
Figure 4-19
Actual Velocity of Servo Arm

4.3.10   Position (Detent) Mode Servo

When the difference between DAR and CAR equals zero,
the servo system switches to the position mode and
the system proceeds to "detent" on the specified

track. The SVDM signal is summed by the master sum-
ming junction, 4U78 input. If SVDM is not zero, an
error signal will force the position motor to position
the servo head toward half way between the selected
"A" - "B" track, and force SVDM to zero volts (Fig.
4-16). From Figure 4-16 it can also be seen that a
polarity changing switch is required as a function
of odd or even track selection. 4U87 is the operat-
ional amplifier used to control polarity.

A velocity signal for position mode is also summed at
the master junction. The velocity signal is used to
stabilize the system when between "A" and "B" tracks;
when the head motion stops, velocity is zero. Velocity
compensation is added by FET switches, 4U93 and 4U84.

A "boot strapped" twin "T" filter is used to reject
resonance centered about 2kHZ and prevents high fre-
quency oscillations. Resistors 4R182, 4R181, 4R207
and capacitors 4C115, 4C118, 4C114 are used to form
the filter. Resistors R224 and R223 are used to add
positive feedback to the filter to reduce filter band-
width.

Pot 4R172 is used to cancel any offsets in the operat-
ional amplifiers 4U87, 4U94, 4U88 or 4U80 by applying
a bias current into the junction to correct any offset
of the servo head. FET switches 4U84 can introduce
intentional offset under I/O control for data recovery.
Test point, TP12, can also offset bias the servo head
and is used to test servo performance.

4.3.11   Servo Power Amplifier

The positioner motor is driven by the power amplifier
located on the power amplifier assembly module (P/N
30332). Feedback is used to make the motor appear to
be driven by a current source.

The power amplifier uses complementary darlington
power transistors biased so that only one can conduct
at a time when driving the position motor. Transistors
1Q8 and 1Q9 are the power transistors. Transistors 1Q1,
1Q2, 1Q3 and 1Q4 are used to drive the power transistors
in a closed-loop feedback system. Integrated circuit
1U1 is a differential amplifier used to amplify current
loop error signals and reject common-mode noise. The
position motor current is sensed by 1R26 on the power
amplifier board. Amplifier 4U68 amplifies the voltage
developed by resistor 1R26 to develop a voltage at TP10
that is proportional to motor current.

The summing junction for the current feedback loop, 4U91 input, detects any error in current between 4R206 and 4R204. Any error present is amplified by error amplifiers 4U91 and 4U77 to provide a correctional signal to the power amplifiers. This signal in turn increases or decreases the motor current as required to reduce the error to zero. A block diagram of the current loop can be visualized as a block whose output is current to the motor proportional to an input voltage to resistor 4R204.

The maximum current that can be applied to the position motor is limited to prevent position motor demagnetization. Zener diodes 4CR32 and 4CR33 conduct to feed a large error current into the summing junction if the voltage at TP10 is higher than the zener's breakdown voltage. The error amplifier loop reacts by reducing the motor current and voltage at TP10. If the voltage at TP10 is limited, the motor current is limited; since a direct relationship exists between TP10 and motor current.

4.3.12   Head Positioner Servo Block Diagrams

Figures 4-20a, b and c show the signal flow during a seek operation. The dark lines show the signal flow path.

Figure 4-20a is the flow path during a move when there is greater than 64 tracks to go. If DAR is larger than CAR, the FWD is enabled as shown by the solid dark lines. If DAR is smaller than CAR, then REV is enabled as shown by the dashed dark lines.

Figure 4-20b is the same as Figure 1a except that either; the head move has progressed until less than 64 tracks remain to go or the initial move request was for less than 64 tracks.

Figure 4-20c shows the signal flow when the head move is completed and the servo system becomes a position servo to detent on the selected data track.

If detented on odd track, ODD is enabled as shown by solid lines. If detented on even track, EVEN is enabled as shown by dashed lines.
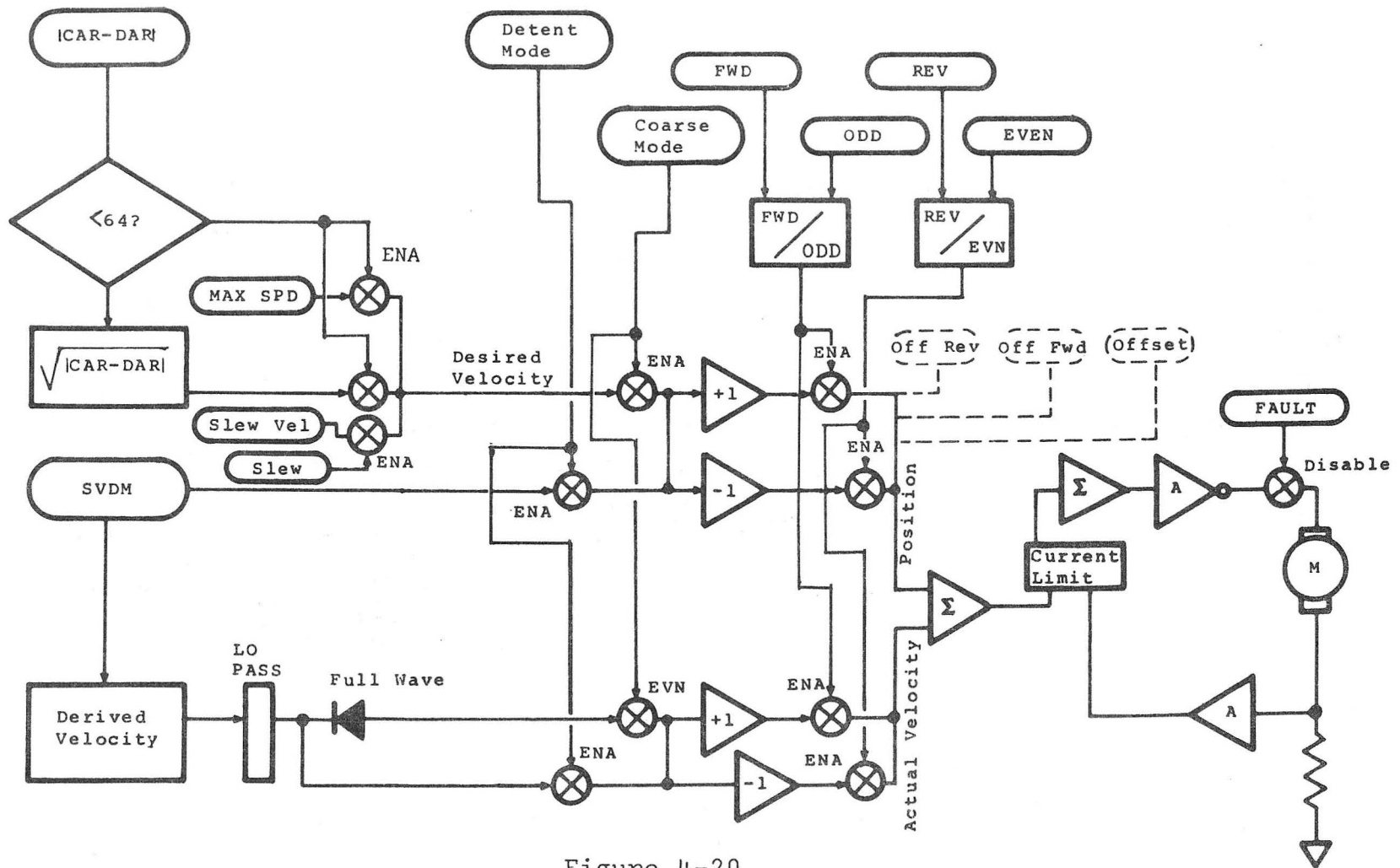
Figure 4-20
Block Diagram Head Positioning Servo System
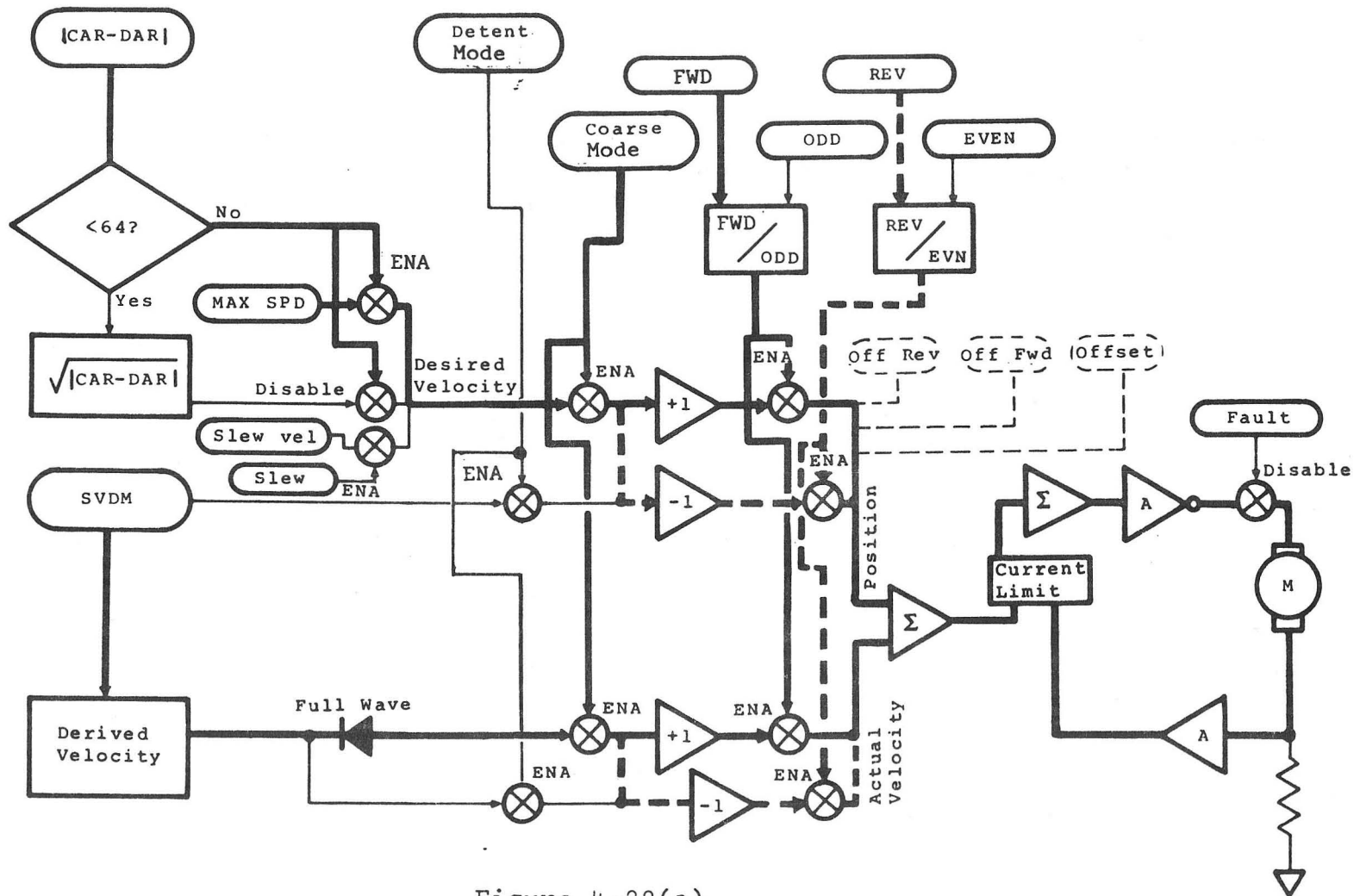
Figure 4-20(a)
Head Positioning Servo-Velocity Mode
(Greater Than 64 Tracks to go)
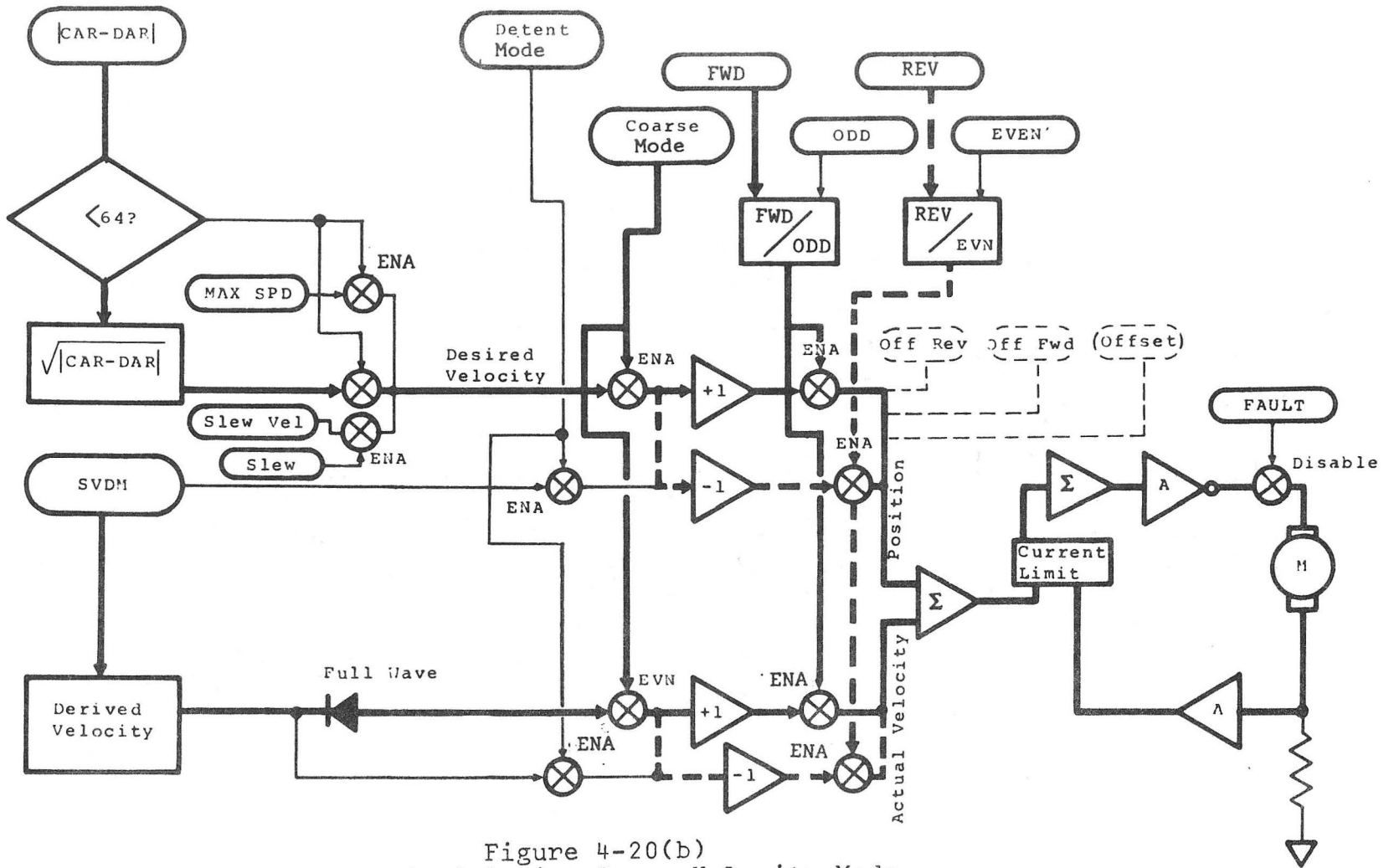
Figure 4-20(b)
Head Positioning Servo-Velocity Mode
(Less Than 64 Tracks to go)
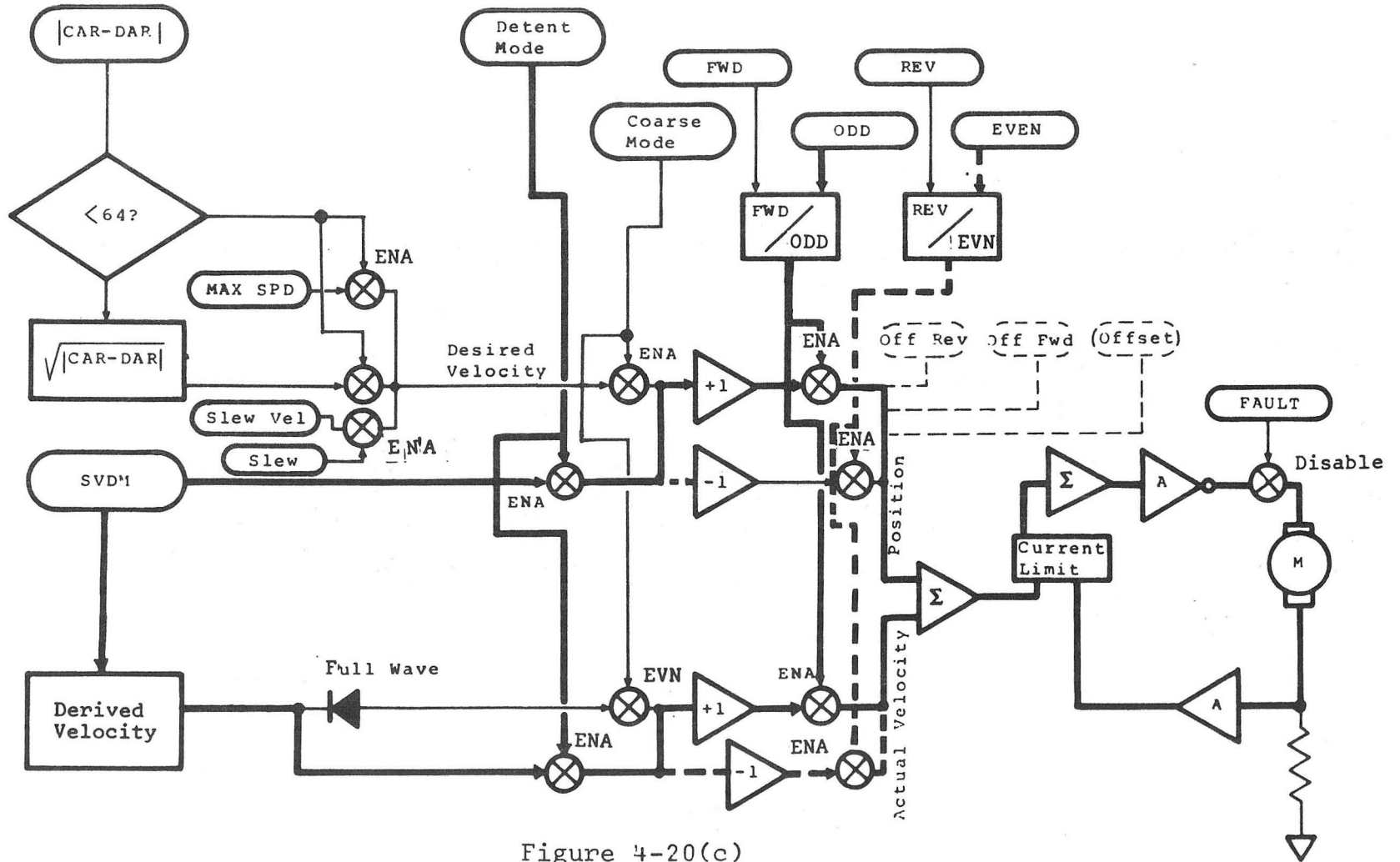
Figure 4-20(c)
Head Positioning Servo-Position Mode

4.3.13   Fault Logic

Figure 4-21 is a block diagram of the Servo Logic Board
fault lines. Transistor packages 3U30 and 3U23 are con-
nected to monitor the 5 volts, 12 volts, -2 volt, -5.2
volt and -12 volt power supplies. If all monitors are
ok, the status line power okay (PWR OK) is set true.

The RC network 3R82, 3C52 form a pulse at power turn-
on that is amplified by 3U30 and triggers 3U22. Timer
3U22 is an approximate 15 second timer that generates
system restore functions at turn on and sets the status
line; inverted power restore (PWRST).

The system restore signal is used to set or hold Flip-
Flops 3U48, 3U33 and 3U59 in the proper state during
start up and prior to energizing the positioner motor.

If the power amplifier heatsink should overheat, thermal
switch S1 opens up and Flip-Flop 3U33 is faulted. This
faults the ready line and disables the positioner motor.

If the positioner motor is above approximately 2 amps
DC for longer than 1 second, the positioner motor cur-
rent monitor 4U45 sets Flip-Flop 3U33 to a fault condi-
tion. This faults the ready line and disables the
positioner motor.

A transducer on the blower pulley generates a pulse
for each spindle revolution. The pulse is amplified
and triggers retriggerable monostable 3U40. If the
spindle slows down, the monostable will "time out" and
3U58 will be faulted. This faults the ready line and
disables the positioner motor. Also, the monostable
timing out will set 3U26 and in turn set 3U33 to cause
an inverted seek late (SKLATE) to disable the positioner
motor. A manual restore is required even if the spindle
should return to speed. Loss of a motor to spindle belt
or spindle to blower belt will also disable the positioner
motor and make the drive go not ready.

If the phase locked loop loses phase lock, or, if sync
is lost, 3U32 sets 3U26 and sets SKLATE low to disable
the positioner motor. A restore is required to clear
the system.

The Flip-Flop 3U26 is also used to detect track cross-
ings after detent on a track has been achieved. Cross-
ing tracks after detent means that the positioner arm
is lost. If more than two tracks are crossed after
detent, the AMB is faulted to disable the positioner arm.
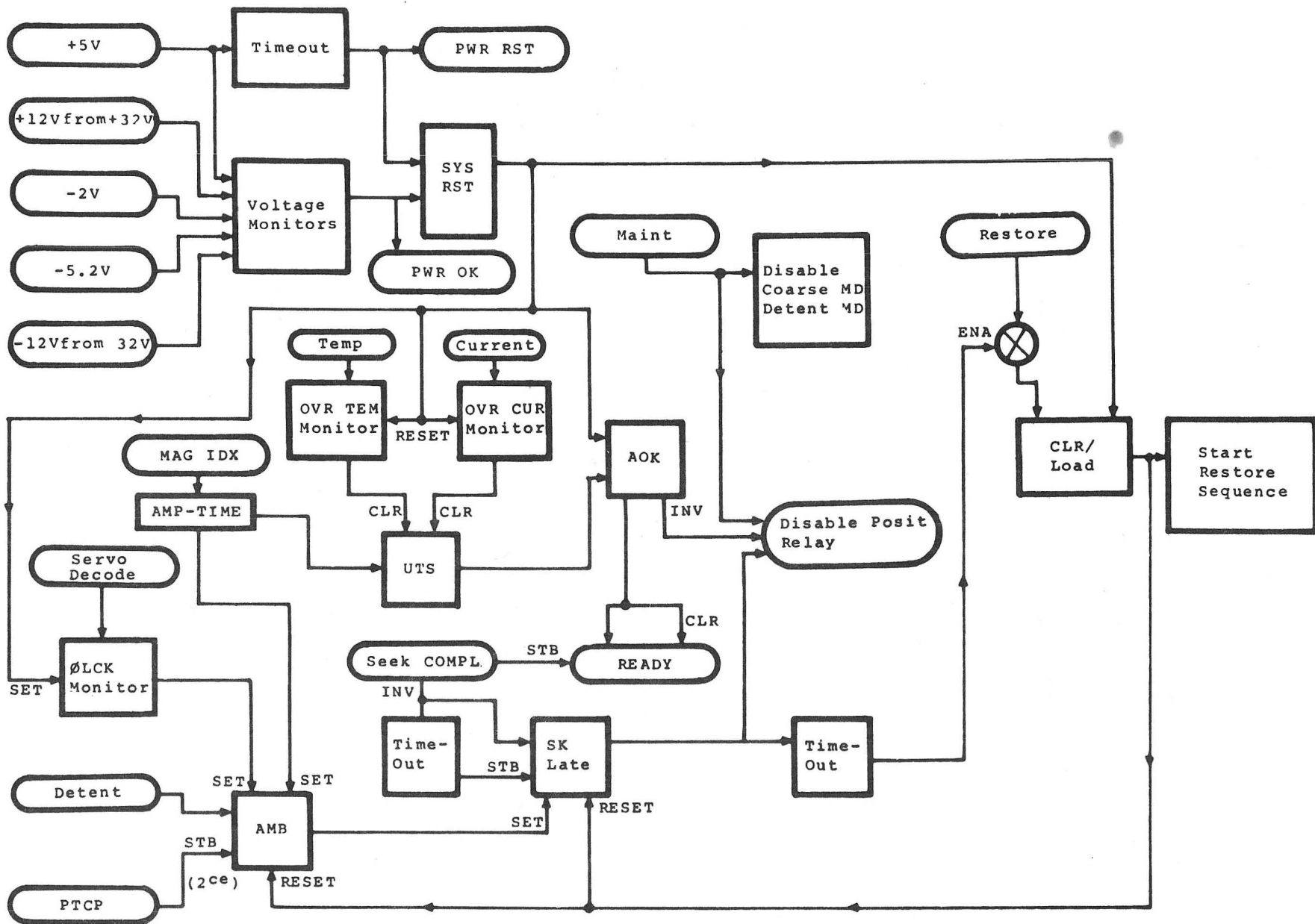
Figure 4-21
Fault Logic

A restore command is required to reset the system. Seek Complete is a term that is set when a successful seek has been completed. On track delay ONTRKDLY normally sets 3U48 to generate the seek complete term. If this time is too long, monostable 3U27 times out and sets SKLATE and at the same time disables the positioner arm. When the system is powered on a seek, complete follows restore and sets the ready line true.

The loss of "up to speed" (UTS) or SYSRST will fault "all is ok" (AOK) and drop the ready line. The ready line must be reset by a manual system restore for a UTS fault. The completion of a successful restore sequence will reset the ready line true.

A low level on inverted maintenance mode $\overline{\text{MAINT}}$ will disable the FET switches for both velocity and position on the analog circuitry. The low level of $\overline{\text{MAINT}}$ will also hold the positioner arm on magnetic detent and the positioner motor disabled.

The disabling of the position motor relay is controlled by 3U34 and 1Q10 on the power amplifier board. The disabling of the positioner motor applies -32V to the motor through a current limit resistor. This drives the positioner arm into the head landing zone and against a permanent magnet. The heads are now safely held by the magnetic latch assembly.

The monostable 3U40 times out after a seek late (SKLATE) for a time long enough to allow the positioner arm to return to magnetic detent prior to accepting a restore command. Seek late delayed (SKLTDL) is used to hold 3U31-2 low and prevent a restore from being started prior to the arm resting on the magnetic detent.

4.3.14   High Ambient Temperature Protection

To prevent damage to the enclosure internal parts in the event that the disc is operated above its specified ambient temperature while positioning frequently, seek times are allowed to degrade. The thermistor sensor amplifier and bias circuit 4U51 and related components sense the resistance change of a thermistor located inside the enclosure. The circuit controls DAC REF which, in turn, controls the output magnitude of the DAC 2U70. The DAC output level sets the system access time. As the enclosure warms up to above 120°F, the thermistor starts to lower DAC RED and, in turn, increases the access time to reduce position motor heat

load in the enclosure. The circuit is designed to
reduce positioner heat load enough to prevent the
enclosure ambient from exceeding 150°F.

4.4   DATA SYSTEM

4.4.1   General

The disc drive includes as various options 1 to 6 disc
surfaces for 2 to 12 moving heads and 1 to 2 disc sur-
faces for 20 to 120 (actually 126 heads, 120 guaranteed
operational) fixed head tracks. The moving heads are
positioned to the desired data track by the servo system.
Fixed heads, of course, do not move. The first group of
up to 40 fixed heads (actually 42 heads, 40 guaranteed
operational) share the bottom surface of the bottom disc
with the servo head. The servo uses the outer band and
the fixed heads the inner band (Fig. 4-4). The second
group of up to 80 fixed heads (actually 84 heads, 80
guaranteed operational) occupy the top surface of the
top disc. The heads are selected by a diode switching
matrix of similar design for both the fixed and moving
heads. The same diode switch is used to read or write
using the head selected.

Figure 4-22 is a data system block diagram. The moving
heads and fixed heads with diode switch matrix are lo-
cated inside the enclosure. The moving head matrix
switch and preamplifier board (P/N 30100) is plugged
directly into the rear of the enclosure to minimize
head lead length (Fig. 5-6). The fixed head amplifier
board (P/N 30104) is located on the side of the disc
drive near the fixed head cable outlet (Fig. 5-9). The
data board (P/N 30102) is located on the top surface of
the disc drive unit (Fig. 5-9). The general signal flow
from the selected head to NRZ input or output is covered
by Figure 4-22; the operation of each block is covered
in the following sections.

4.4.2   Moving Head Preamp and Switch Matrix

Figure 4-23 shows a simplified schematic of the diode
switch matrix. The matrix is located with the moving
heads inside the enclosure. The control switches S_0---
S_{11} are located on the matrix board. Switches S_0---S_{11}
are integrated circuits 1U11 and 1U14.
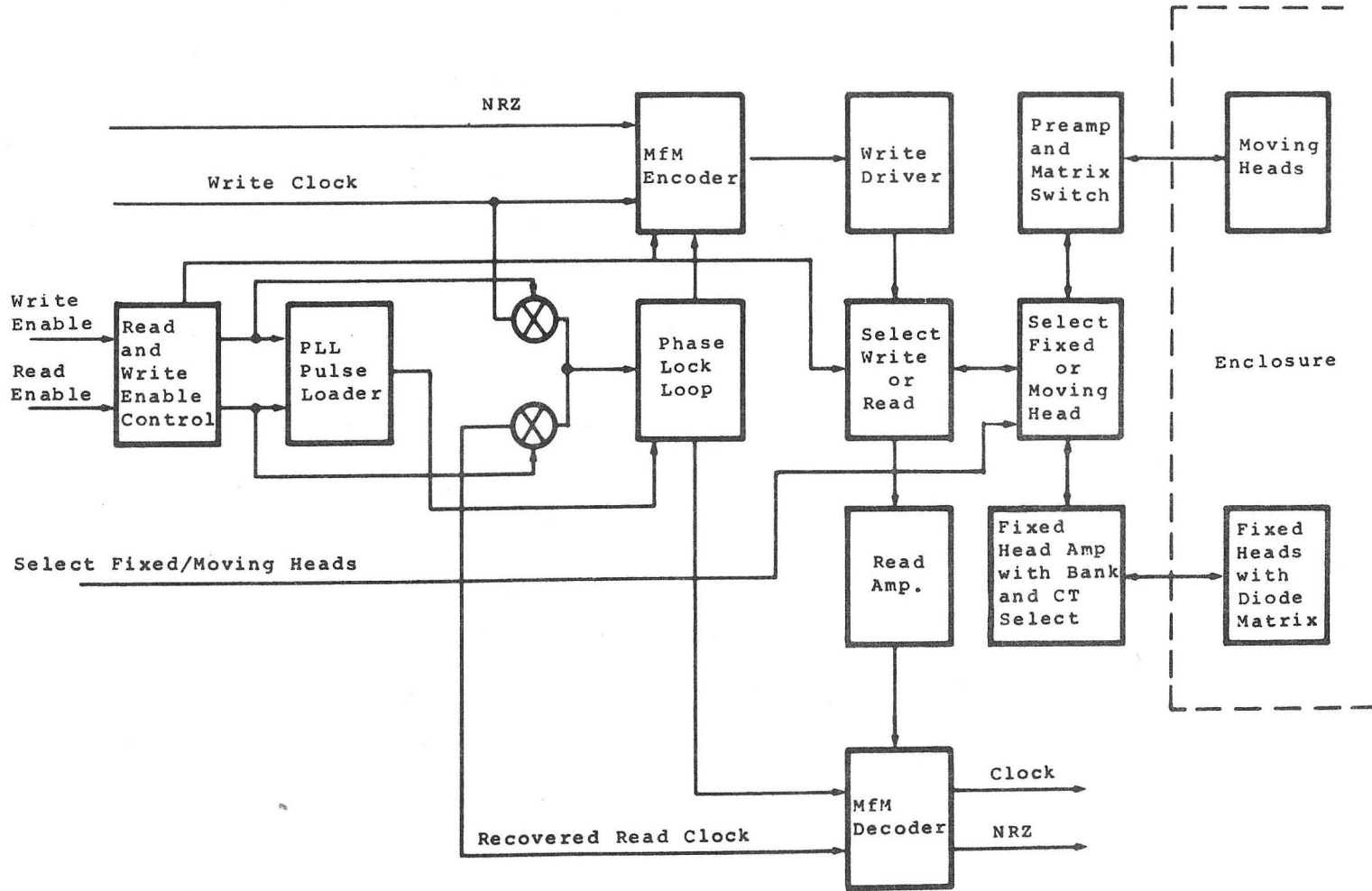
Figure 4-22
Data System
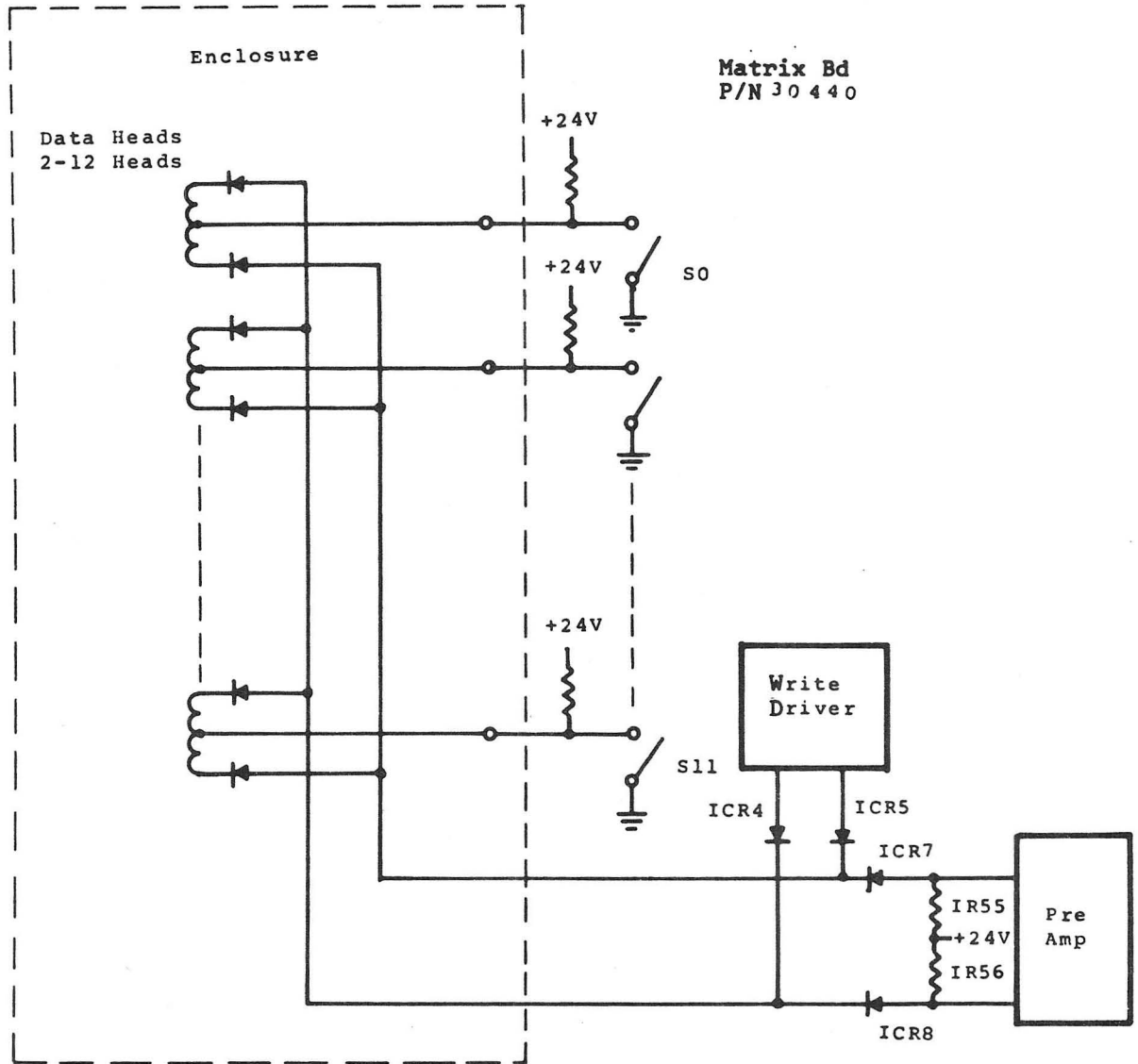
Figure 4-23
Moving Head Preamp and Switch Matrix
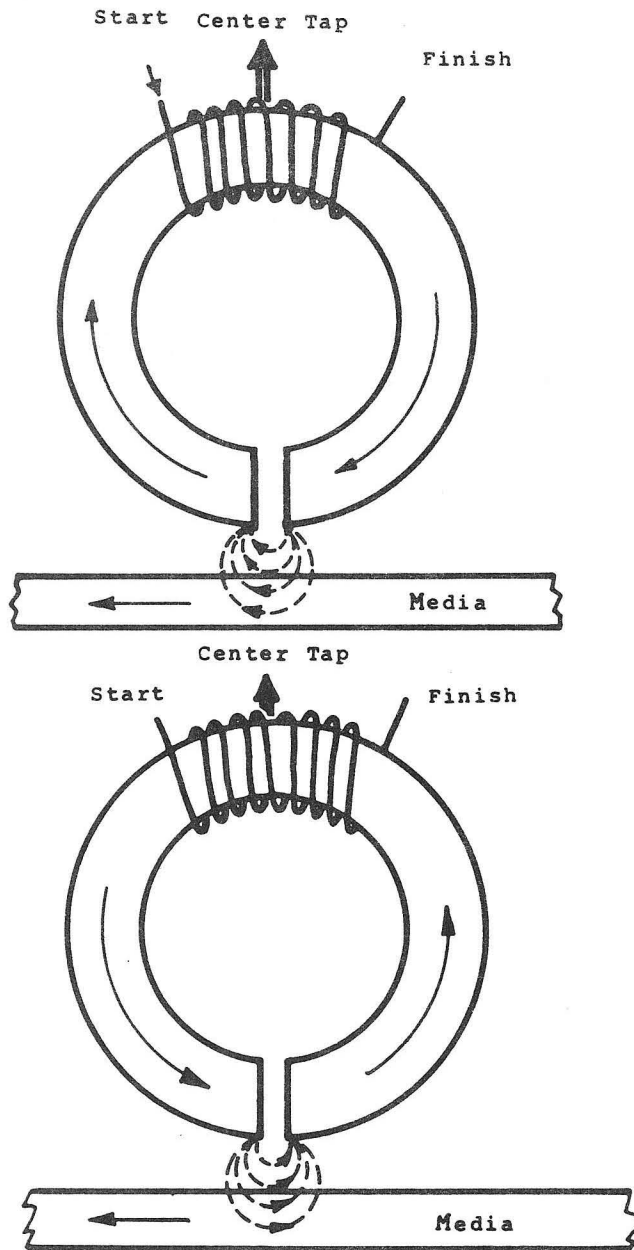
Figure 4-24
Data Head Magnetic Field

U11 decodes heads 0-9 and 1U13, 1U14, and 1U16
decode heads 10,11. Only one switch is closed at
a time, and when closed, that head is selected by
providing a current path to ground thru current
source 1R55, 1R56, turning on 1CR7, 1CR8 and the
diodes of the selected head. The "on" diodes have
a low resistance and couple head signals to or from
the selected head. During Write the write transistors
1Q6 & 1Q5 act as a current switch to steer the
current set by current setting resistors 1R17 and
1R25 thru 1CR4 or 1CR5 thru selected head diodes to
the head to produce flux reversals, see Figure 4-24
and 4-25. During a "write" diodes 1CR7 and 1CR8 are
overridden and 1CR9 and 1CR10 limit the maximum
signal into the preamplifier. The matrix board
preamplifier is a low noise amplifier using
negative feedback. Transistors 1Q7 and 1Q8 set the
preamp noise level and are of a low noise design.
Integrated circuit transistors and discrete components
are used for the remaining preamp circuitry. The
design is similar to the Ua733 integrated circuit
design. Components $1L_1$ -$1L_4$, $1C_3$ and $1C_{16}$ form a
low pass-phase linear filter. The filter is buffered
by emitter follower circuit composed of 1U1 and
related components.
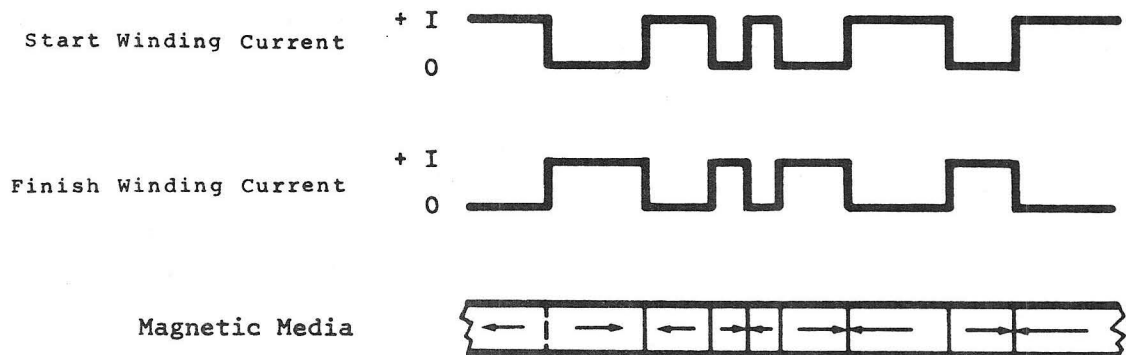
Figure 4-25
Magnetic Field on Media

Enclosure
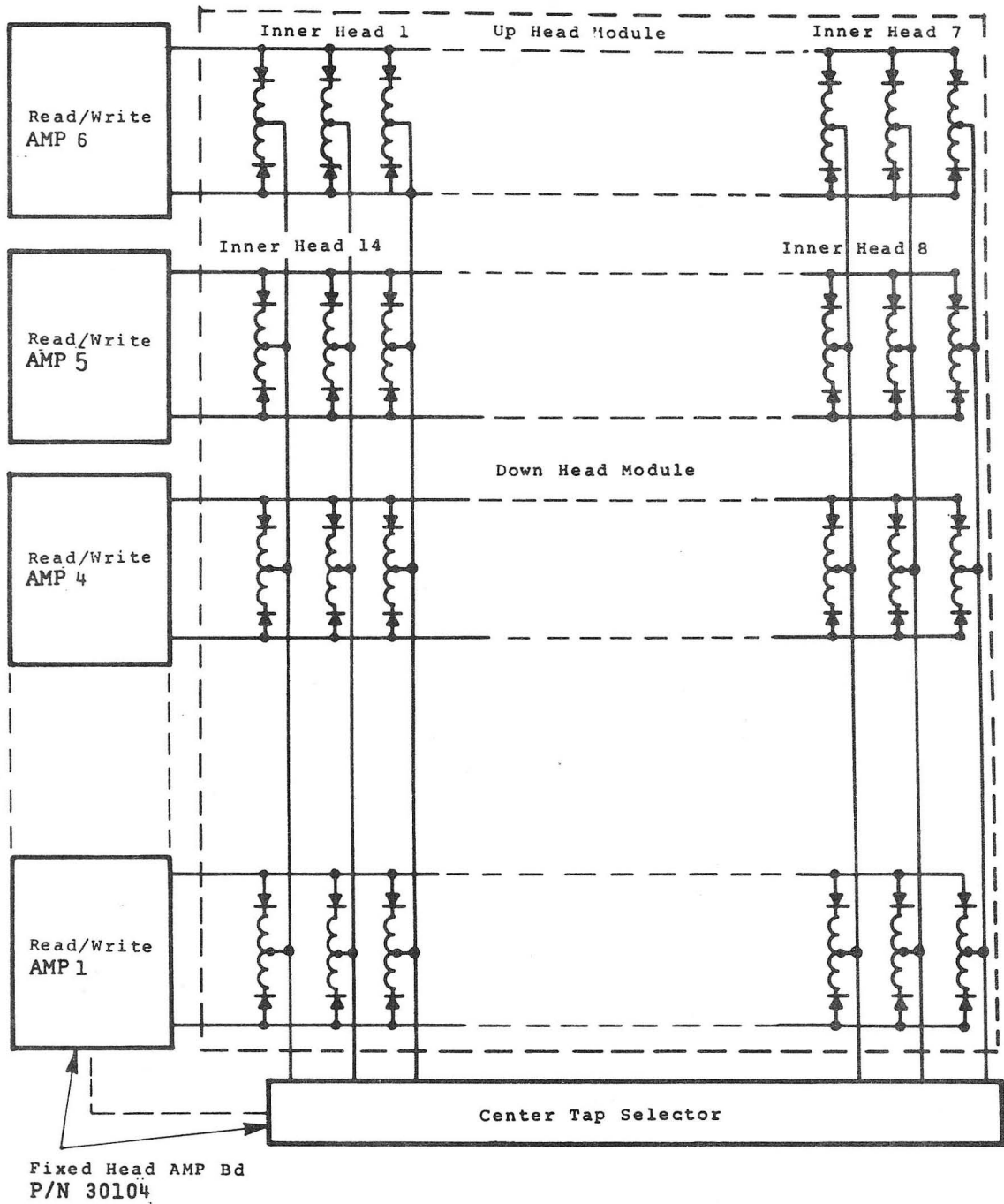
Figure 4-26
Fixed Head Select Matrix

4.4.3   Fixed Head

The fixed head module operation is nearly identical
to the moving head module except for a more complex
head switching array. Figure 4-26 illustrates the
fixed head selection circuitry. One of six read/write
amplifier circuits can be selected to service 21 heads.
Also one of 21 center taps can be selected on up to
6 banks of heads. When a center tap and a read/write
amplifier are selected a definite head is selected.

The fixed head amplifier board preamplifier is an
integrated circuit. The higher amplitude output from
the fixed heads does not require as low noise
preamplifier design as the moving head preamplifier.

The low pass filter and buffer design are the same
as the matrix board unit.

The fixed head signal or moving head signal is
selected on the data board (P/N 30102) by integrated
circuits 1U3 and 1U4. The lower transistors of 1U3
and 1U4 are current sources that can be switched
off or on. When the current source is on, the upper
portion of that integrated circuit is active and
the desired channel is selected. Integrated circuits
1U52 and 1U6 turn on or off the current sources
as required.

4.4.4   Data (MFM Encoding)

Data is written on a track by using modified frequency
modulation (MFM). A magnetic flux change is written
in the center of each "1" cell and between "0" cells.
No flux change is written on a "0" cell/"1" cell
boundary. See Figure 4-27 for an example of MFM
encoded data.

The data board converts NRZ data received to MFM by
following MFM encoding rules. The flip flop 2U17 part 1
is connected as a shift register. Write clock is
phase locked to the PLL and serves to frame incoming
NRZ data and shift it through the shift register. Dual
flip flop 2U23 is connected to toggle on each positive
going input. The outputs of U23 drive the write drivers

Bit Cell	1	1	0	1	0	0	0	1	1	1	0

Encoded Data
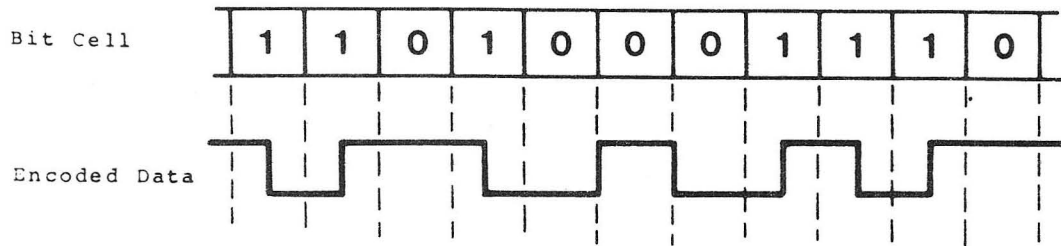
Figure 4-27
MFM Encoding

on the matrix board and fixed head amplifier board.
If a "1" is shifted to the second stage of shift
register (2U17 part 2) then at time T3 both inputs to
2U14 part 2 are low and 2U14-2 goes high to toggle U23.
This causes a change of state on U23 to create a flux
change in the center of a "1". If both sections of 2U17
have zero's stored. Gate U14 pins 12 and 13 are low and
at time T7 U14 pin 15 will go high to toggle U23. This
causes a change of state on U23 to create a flux change
between zero's. Fig. 4-28 shows the timing for the MFM data.

The write drive circuitry for the matrix board and fixed
head amplifier board are nearly identical. Transistor
1Q1 and 1Q2 on the matrix board and transistors 3Q3 and
3Q4 on the fixed head amplifier board are driven by the
MFM generation flip flop U23 on the data board. Tran-
sistors 1Q1, 1Q2 on the matrix board and 3Q3, 3Q4 on the
fixed head amplifier board in turn drive current steering
transistors 1Q5 and 1Q6 on the matrix board and tran-
sistor switch banks 2Q102--2Q602 and 2Q103--2Q603 on the
fixed head amplifier board. Transistor 2Q101-2Q601 is
selected to write on the desired bank. Since either
write transistor has a constant emitter voltage regard-
less of which transistor is turned on by the MFM gene-
ration flip flop U23, a constant voltage will result
across write current setting resistors 1R17 and 1R25
on the matrix board. Resistors 3R4 and 2R 112--612
have a constant voltage across them and function the
same way for the fixed head amplifier board.

A constant voltage across a resistor results in a
constant current to the current steering transistors.
Resistor 1R17 on the matrix board and resistor 3R4 on
the fixed head amplifier board are adjustable to set
the write current magnitude. Figure 4-24 shows the
resultant magnetic field due to write current and
Fig. 4-25 shows the resultant magnetism of a disc for a
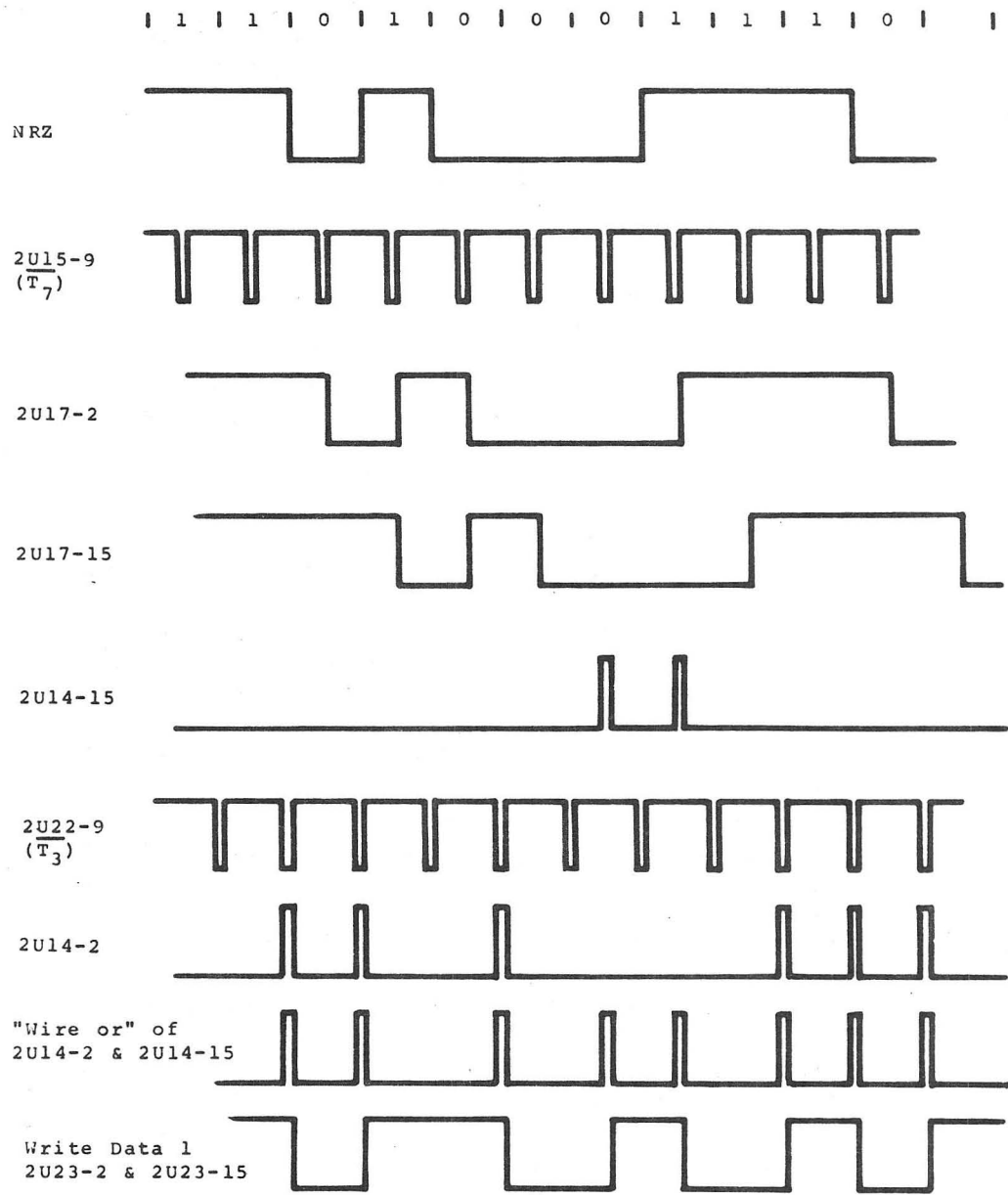
Figure 4-28
MFM Timing
IV-44

given word pattern.

4.4.5   Data (Phase Locked Loop)

The data board flip flops 3U28 and 3U29 and related gates serve to clear and synchronously load shift registers 3U36 and 3U37.

Synchronously loading the shift register reduces the phase error in the phase locked loop to a maximum of 1/8 of a cell time, this minimizes the loop settling time. Figure 4-29 shows the timing of this loop. Important outputs are 3U30-9 which clears the shift register and the wire "or" of 3U31-15 and 3U31-2 which loads the shift register.

The shift register when loaded "shifts" the loaded " 1 " around the loop continuously to produce a divide by 8 function. A data cell is broken into 8 time intervals. The voltage controlled oscillator (VCO) oscillates at 8 times the cell frequency and is phase locked to the cell frequency by the phase locked loop.

The phase locked loop is similar to the loop used on the servo board. Transistors 3Q1 and 3Q2, and integrated circuit 3U43 and 3U44 plus related components function as the voltage controlled oscillator (VCO). Figure 4-30 shows the ideal waveforms expected by the VCO. Since actual operating frequency (about 56 MHZ) approaches the rise and fall times of the gates, the actual waveforms are rounded and somewhat sinusoidal.

The phase detector is made up of individual IC's 3U40, 3U41 and 3U42. Functionally it is similar to the Motorola 4044 IC, except being ECL and therefore faster.

The phase detector is both phase and frequency sensitive and responds only to positive transitions. Wave shapes have no effect on operation. Figure 4-31 shows operation for the four possible states of operation which are:

1. Reference signal (R) with phase lead over the variable (V) signal of the voltage controlled oscillator.
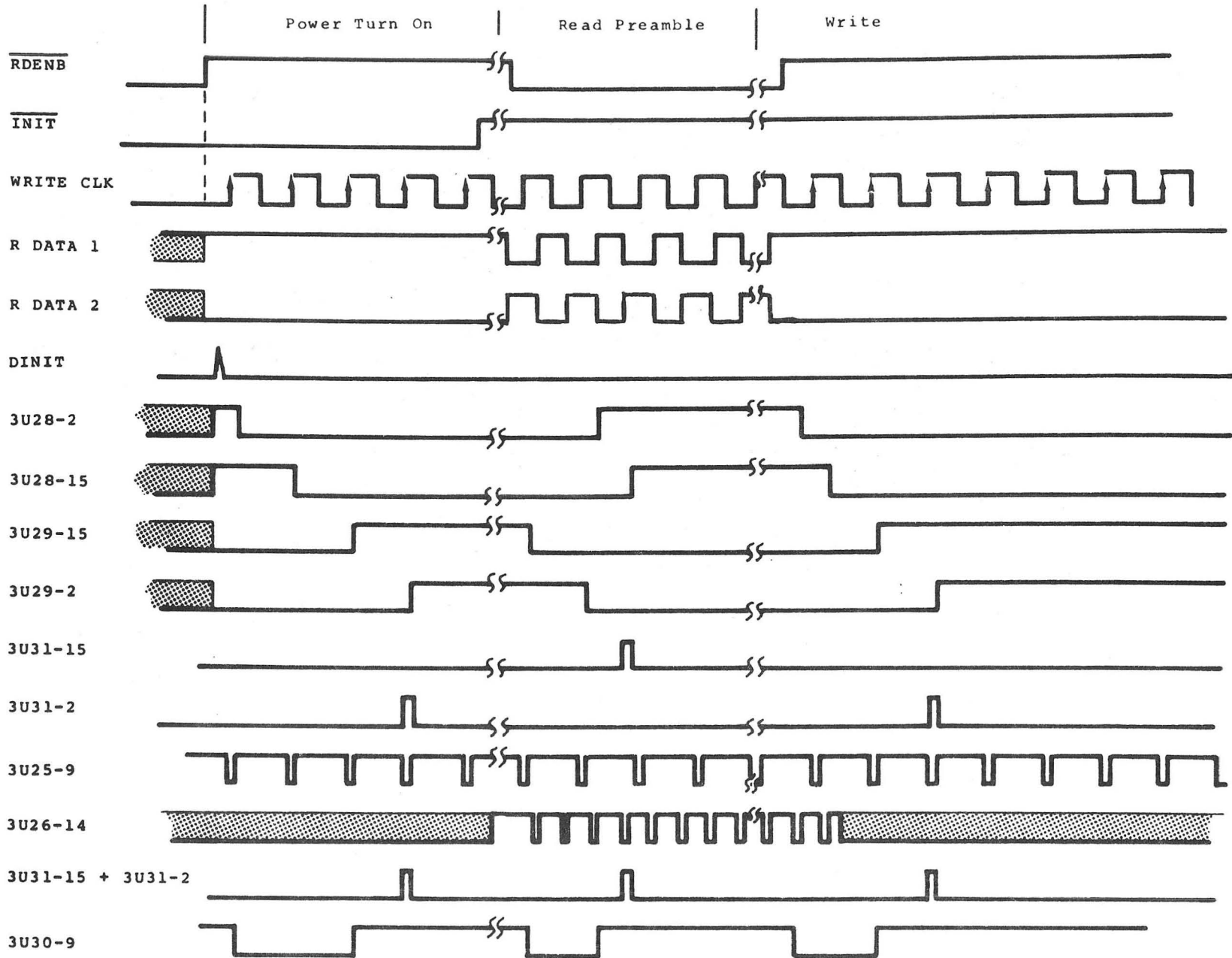
Figure 4-29
Phase Locked Loop Timing
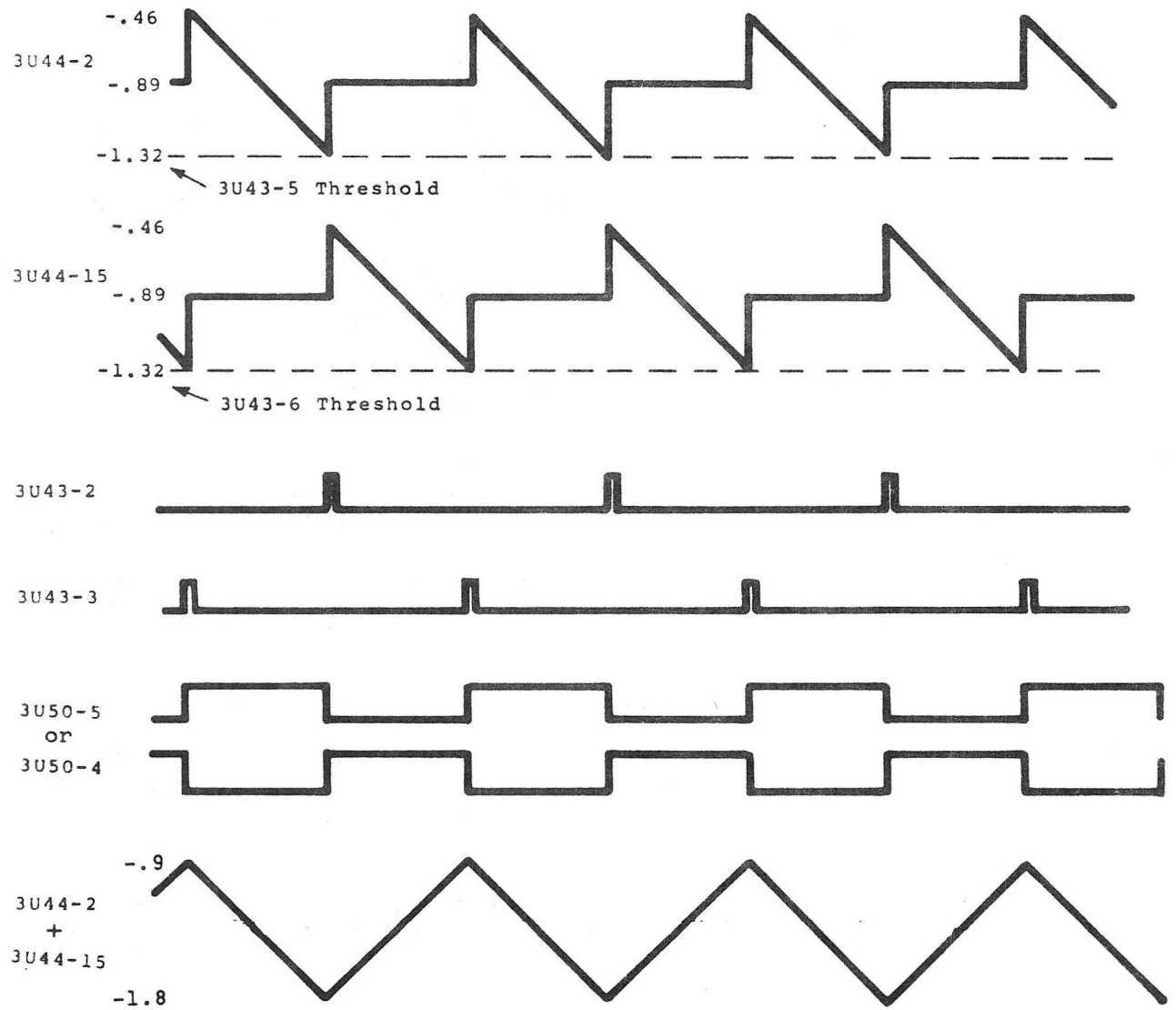
Figure 4-30
Voltage Controlled Oscillator

2. Reference signal with phase lag.

3. Reference signal at a higher frequency than the variable signal from the VCO.

4. Reference signal at a lower frequency than the variable signal from the VCO.

The output pulses from the output up (U) or output down (D) are filtered and subtracted to produce an error signal that is amplified by 3U39 and fed to the VCO to correct the phase or frequency error. Capacitors 3C27, 3C28 and resistors 3R49 and 3R51 stabilize the negative feedback loop and prevent oscillation. Also they add electrical momentum to the PLL, to prevent minor disturbances from affecting frequency of operation.

The VCO oscillates at 8 times the clock frequency. The shift registers 3U36 and 3U37 divide the VCO frequency by 8 and serve as the variable (V) input to the Phase comparator. Either write clock or recovered read clock are used as the reference signal (R).

For finer resolution in setting data recovery and margin windows, phase 1 and 2 of the VCO are split. This allows a PLL running at 8 times the reference frequency to produce 16 time intervals. Integrated circuit 3U51 generates the 1/16 of a cell time intervals required.

During write or standby (not reading) the PLL is synchronized with the write clock. Time T4 is gated to the phase detector through gates 3U34 and 3U35 and is in positive going edge phase lock with write clock.

During a "read" cycle operation of the phase locked loop becomes more involved. Clocks between cells occur only between "0" cells. During "1" cells clocks occur at the center of each cell. During a "0" cell/"1" cell boundary no clock is received. Provisions must be made to keep both phase and frequency constant to both the (V) and (R) input of the comparator for all of the above cell conditions.

CONDITION 1

R

V

$\overline{U}$

$\overline{D}$

CONDITION 2

R

V

$\overline{U}$

$\overline{D}$

CONDITION 3

R

V

$\overline{U}$

$\overline{D}$

CONDITION 4

R

V

$\overline{U}$

$\overline{D}$
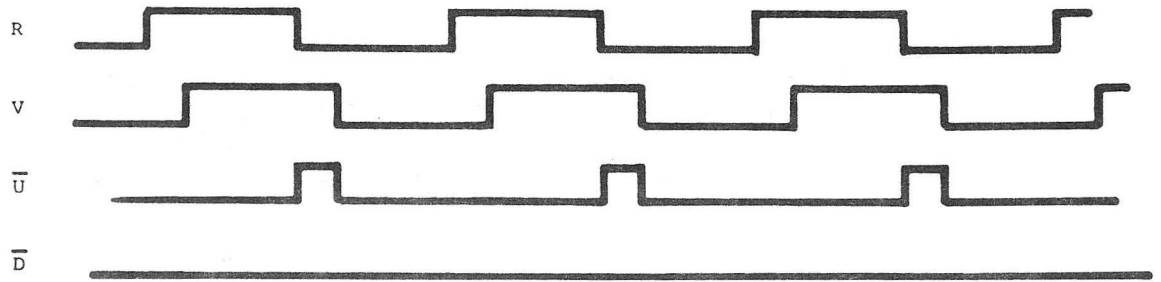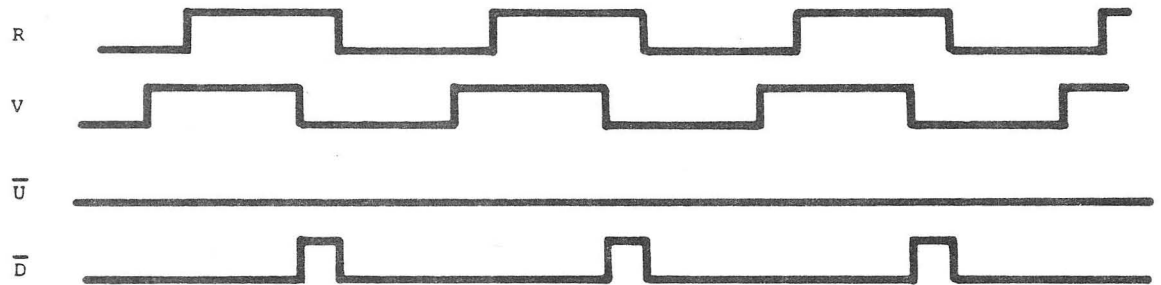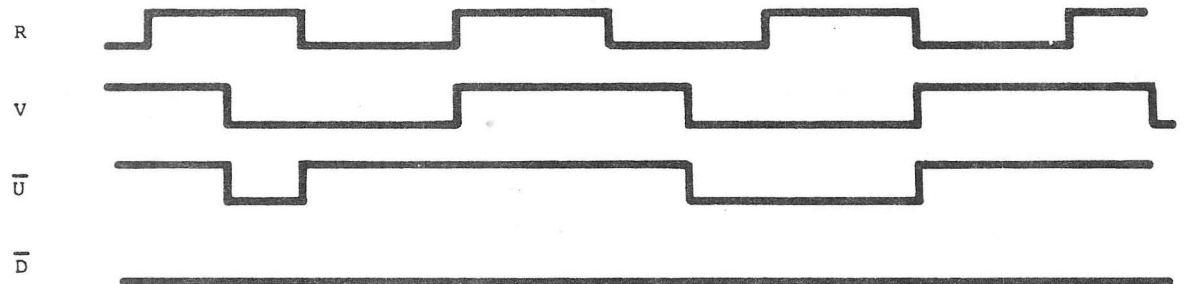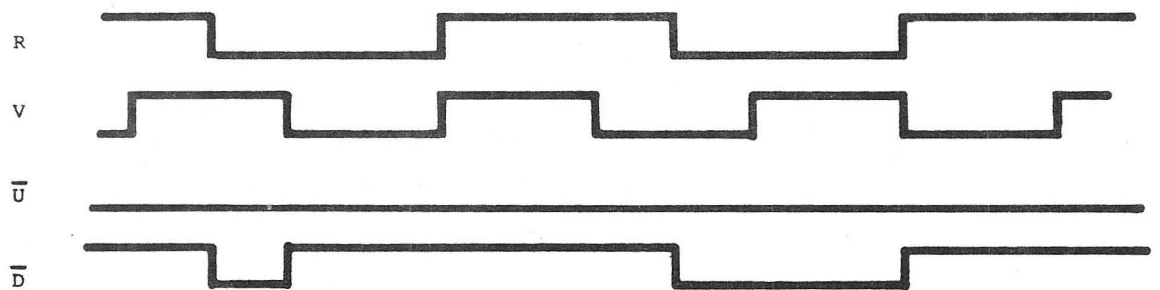
Figure 4-31
Phase Detector

IV-49

If phase or frequency to the phase comparator is
altered, the phase locked loop (PLL) would have a
transient error condition. This is undesirable as
"window" timing would be altered. Corrections are as
listed below.

Correction for phase locking on "1's" versus "0's"
is accomplished by altering the "T" time the PLL is
locked on for "1's" or "0's". "0's" gate 3U33 part 1
and "1's" gate 3U33 part 2 decode the received data
to determine if a "1" or a "0" has been received, the
PLL locks to "T" time T4. If a "1" has been received
the PLL locks to "T" time T_0. The net result is that
the PLL is phase locked to a cell boundary regardless
of receipt of "1's" or "0's".

The remaining problems of missing transitions on a
1/0 boundary to reference (R) is compensated for
by also deleting a transition on variable (V).
Since both (R) and (V) have deleted the same tran-
sition, no phase or frequency disturbance occurs to
the PLL. Figure 4-32 shows the timing of the PLL
system upon receipt of a typical data pattern.

Gates 3U35-15 and 3U35-2 feed the V and R signals to
the phase comparator during all normal operation.
Only during system turn on or test, are gate 3U35-14
and 3U35-3 enabled to allow BCLK reference and T_0 to
be fed directly to the PLL so that initial PLL
adjustments can be made.

4.4.6   Read Data Signal Processing

The MFM data from either fixed or moving heads is
selected as desired. Desired information is contained
in the peaks of the MFM data. By differentiation of
the MFM data, peaks become zero crossings and are
easier to detect. The MFM low frequency pattern
(10101---) may produce erroneous zero crossings which
must be corrected for. (A later section covers the
operation of the circuit.) A delay line (1DL1) is
used to differentiate the MFM data received. Delay
line 1DL1 can be thought of as two separate delay
lines, each 35 NS in length with the ends shorted.
After a time delay of 70 NS (time to end of delay
line and back) a signal on the delay line output
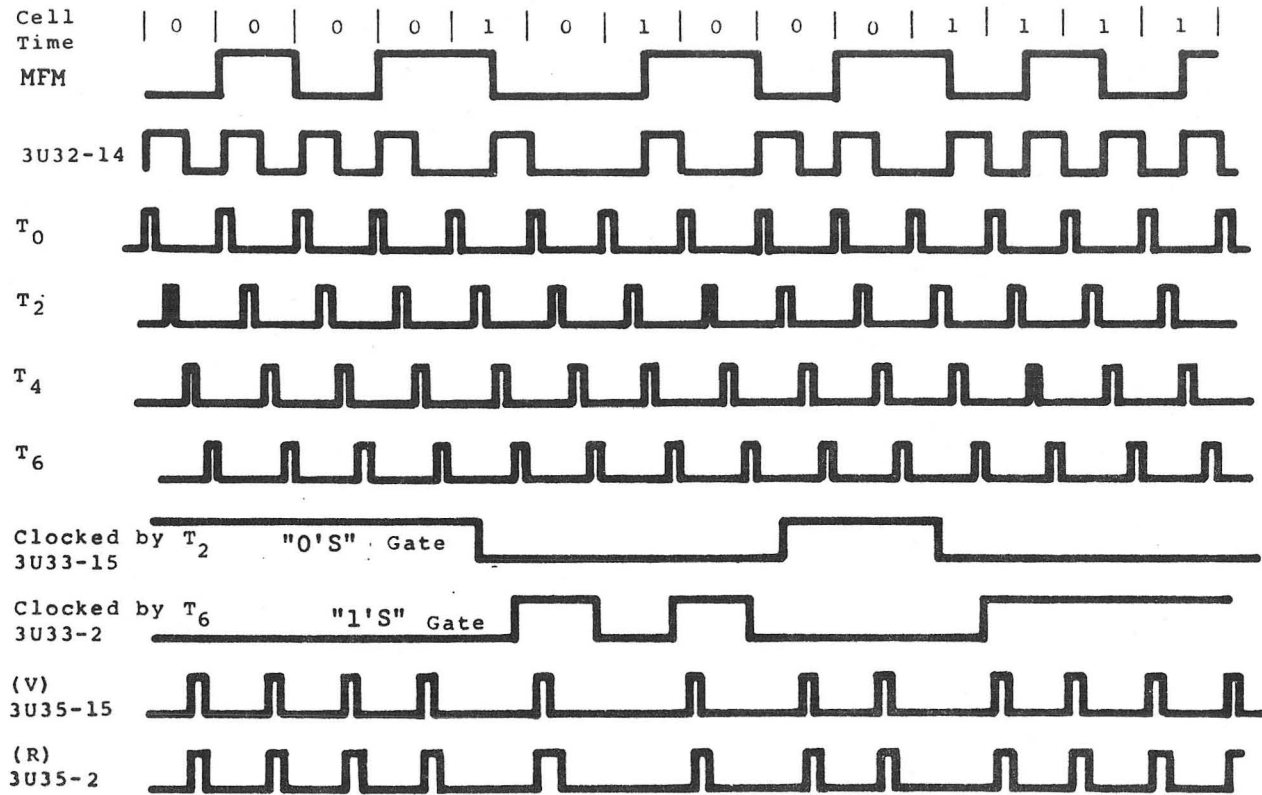
Figure 4-32
PLL Timing With Data Pattern

reflects back as an inverted signal of equal
amplitude to cancel the initial signal. Figure 4-33
shows the resultant output signal for inputs produced
by an all "0's" or all "1's" pattern or an
alternating "1" and "0" pattern.

The output from the delay line drives an emitter
follower buffer 1U5. The buffer drives the final
Lowpass filter composed of inductors $1L_1$ -- $1L_4$,
capacitors $1C_{8-9}$ and related termination resistors.
Integrated circuit 1U8 serves to "square up"
the signal and convert it to ECL logic levels.

The threshold of the "squaring up" circuit is
adjusted by adjustable divider 1R34 so as to "square
up" the noise when no input signal is present.

As an option, an automatic threshold adjust circuit;
1U10, 1U11 and related circuitry is installed.
Resistors 1R34 and 1R35 are deleted with this option.

The Auto threshold adjust functions on system turn on
when the term MINIT is low. At turn on, 460kHz clock is
fed to up-down counter 1U10. If 1U8-6 were high and
1U8-7 were low, the counter would start to count up.
Integrated Circuit 1U11 and related resistors act as
a digital to analog converter. As count up continues,
an increasing current is steeped into 1U8-5 until
1U8-6 goes low and 1U8-7 goes high. At this time the
counter will start to count down. As soon as a one
count down occurs the system will start to count up
again oscillating about the point where the
"squaring up" circuit is biased to threshold value.
When MINIT goes away, Counter clock stops and the
counter is locked with the threshold adjust value
stored in the counter.

As discussed earlier, the problem of an erroneous
zero crossing must be detected and eliminated from
the data pattern. The lower frequency pattern known
as an "1F" pattern may have enough resolution that
the head output voltage due to a flux reversal may
return to zero volts prior to another flux reversal.
If this happens, the derivative of both the peak
output voltage and the zero volts condition could be
zero resulting in an extra output. The output, due to
the zero volt condition, is erroneous and must be
eliminated.

All "0'S" or
all "1'S" pattern

Delay Line
Reflected Pattern of
Above

Resultant Signal
IU3-11 or IU3-8

Alternating
"0"-"1"
Pattern

Reflected Pattern
of Above

Resultant Signal
IU3-11 or IU3-8
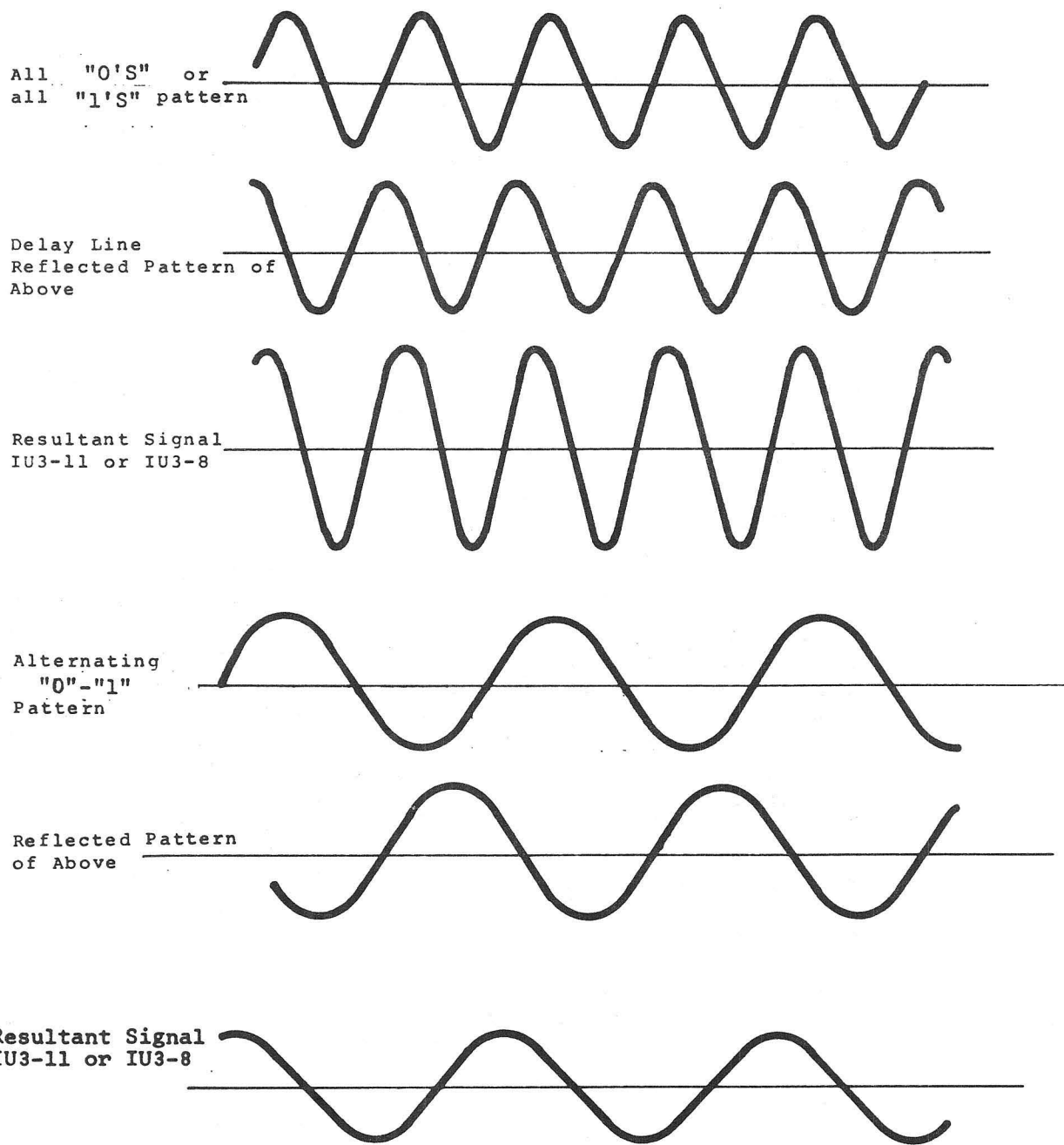
Figure 4-33
Read Data Signal Processing

Figure 4-34 shows the timing of the erroneous zero
crossing deletion circuit. Any erroneous signal
occurring in the center of the "1F" pattern ± 1/4
of a cell time will be rejected. The timing of 1U12-11
is adjusted by the delay line 1DL2 so that on an
all "1's" or all "0's" pattern, known as a "2F"
pattern, a pulse is in the center of the cell.

4.4.7   Read Data (Decoding to NRZ)

The conversion of MFM data to NRZ and related read
clock is done by 3U45, 3U48 and related circuitry.
Figure 4-35 shows the waveforms related to MFM
decoding. Signals RDATA1, and RDATA2 are shaped
into pulses and "NOR'ed" to produce a negative
transition for either a positive or negative MFM
transition. Figure 4-35, 3U27-9 show the waveform
expected. Times T2 and T6 are derived by the PLL
(see Figure 4-32) set and reset 3U45 pins 2 & 3
as shown. Signal DLCORP is a delayed (by delay line
3DL3) and inverted by 3U32-3 signal whose delay time
is one half of a cell time. In actual practice the
leading edge of DLCORP is adjusted by the delay line
3DL3 to be the center of 3U45-3 waveform on an all
"1's" or "0's" pattern. Integrated circuit 3U48 part 2
latches the signal from 3U45-3 as clocked by DLCORP.
Integrated circuit 3U48 part 2 forms recovered NRZ
"0's" and pulses for NRZ "1's". Integrated circuit
3U48 part 1 shifts data from U48 part 2 to develop
recovered NRZ. Integrated circuit 3U49 converts NRZ
and Read Clock (RDCLK) to TTL levels for the I/O
board interface.

A test mode exists where window timing can be
altered to check system margins. Integrated circuits
3U38 and 3U47 are one of 8 decoders. During normal
operation control lines A, B and C are all zero and
time T2 is gated to S and time T6 is gated to R to
form normal windows. Table 4-1 shows the other window
timings possible.

Terms $\overline{\text{STR EARLY}}$ and $\overline{\text{STR LATE}}$ move cell boundaries
about 9NS early or late, respectively. Term $\overline{\text{M MODE}}$
moves cell boundaries 9NS in on both edges. For
combinations of these terms refer to Table 4-1.
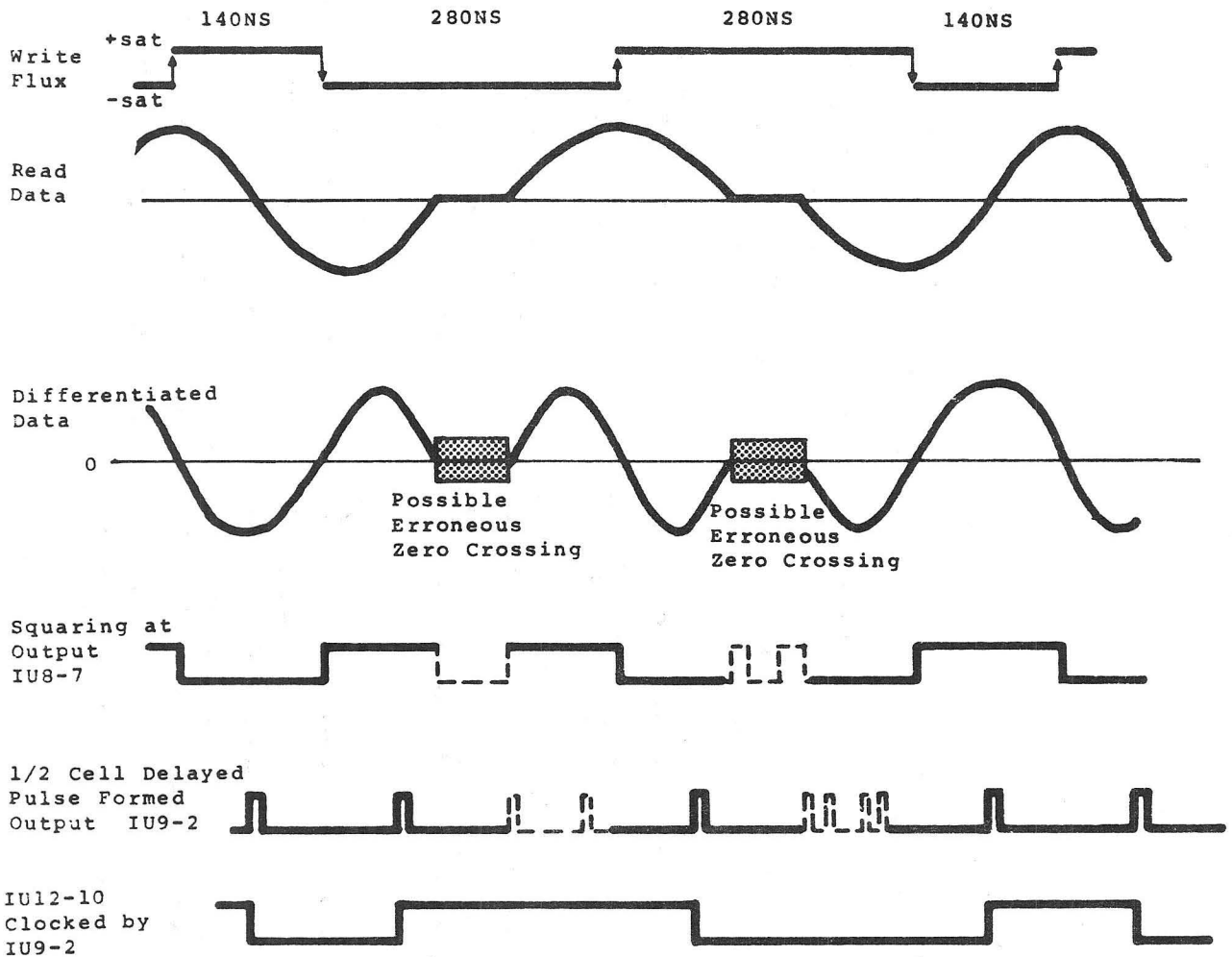
Figure 4-34
Erroneous Zero Crossing
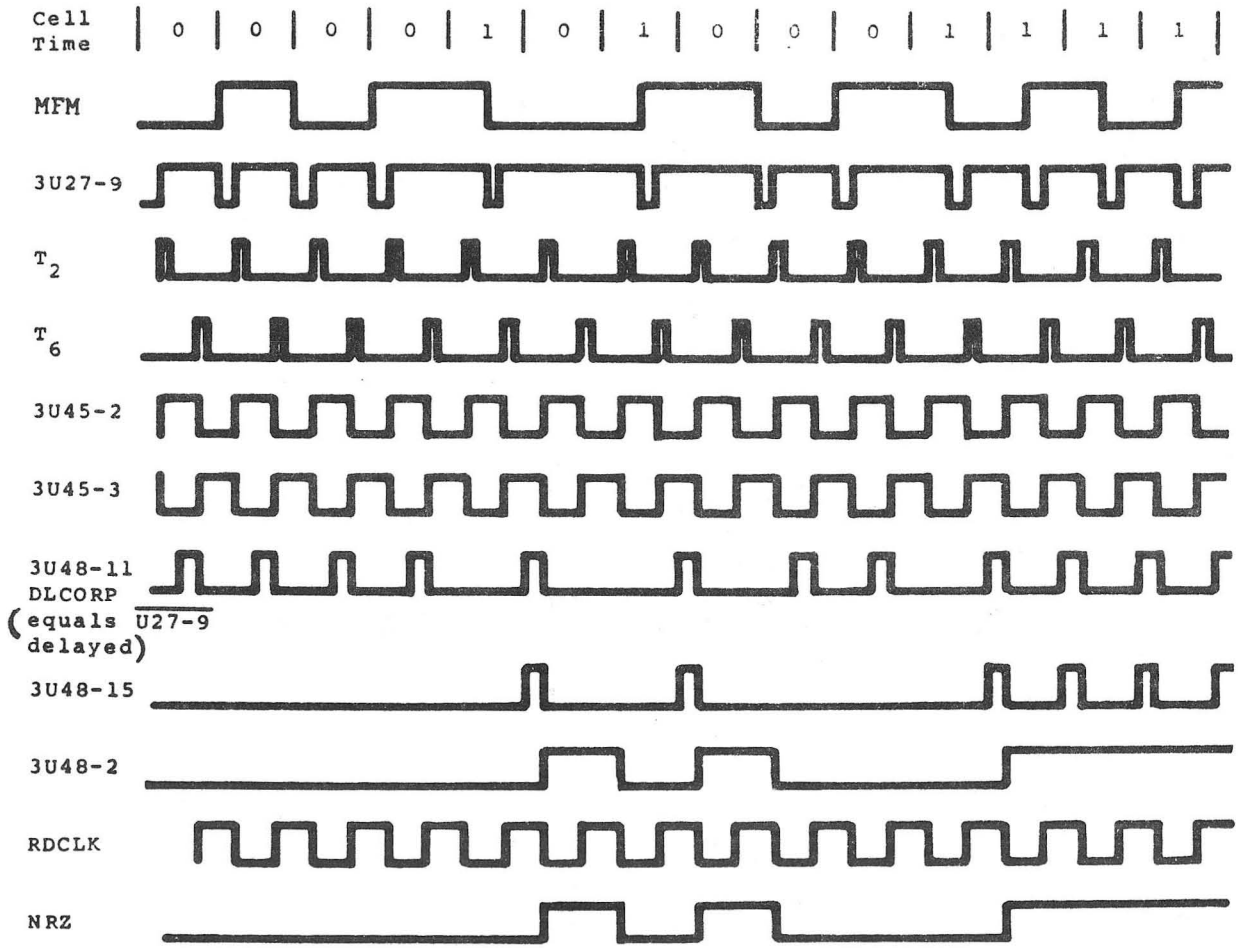
Figure 4-35
Read Data Decoding

Table 4-1
Early/Late Data Strobe

$\overline{STR-}$ EARLY	STR LATE	M MODE	C 2^2	B 2^1	A 2^0	WINDOW TIMES S	R
1	1	1	0	0	0	T2	T6
0	1	1	0	0	1	T1 Ø2	T5 Ø2
1	0	1	0	1	0	T2 Ø2	T6 Ø2
0	0	1	0	1	1	T2	T6
1	1	0	1	0	0	T2 Ø2	T5 Ø2
0	1	0	1	0	1	T3	T5
1	0	0	1	1	0	T1	T5
0	0	0	1	1	1	T3	T7

4.5   INTERFACE (P/N 30115)

4.5.1   General

The 3300 CDC-9760 compatible I/O Board generates the
External CDC Interface (Section 3) from the Internal
3300 Internal Interface (at P11 & P12). The I/O
Board is organized into a set of logic modules,
see Fig.4-36, which perform the CDC to Internal
Interface operation. These modules and their theory
of operation are discussed in the following para-
graphs. Complete signal timing is covered in Section II.

4.5.2   Transceivers (Refer also to 2.4 and 2.5)

4.5.2.1. A Cable Transceiver

The A-Cable Transceiver consists of differential
drivers and receivers which interface to headers
J31 and J34. These drivers and receivers are
comprised of 75110 and 75107B transmitters and
receivers, respectively. The A-Cable receivers
1U59, 1U60, 1U64, 1U69, 1U71, 1U73, 1U75, 1U78,
1U79, 1U80 are disabled to prevent oscillation during
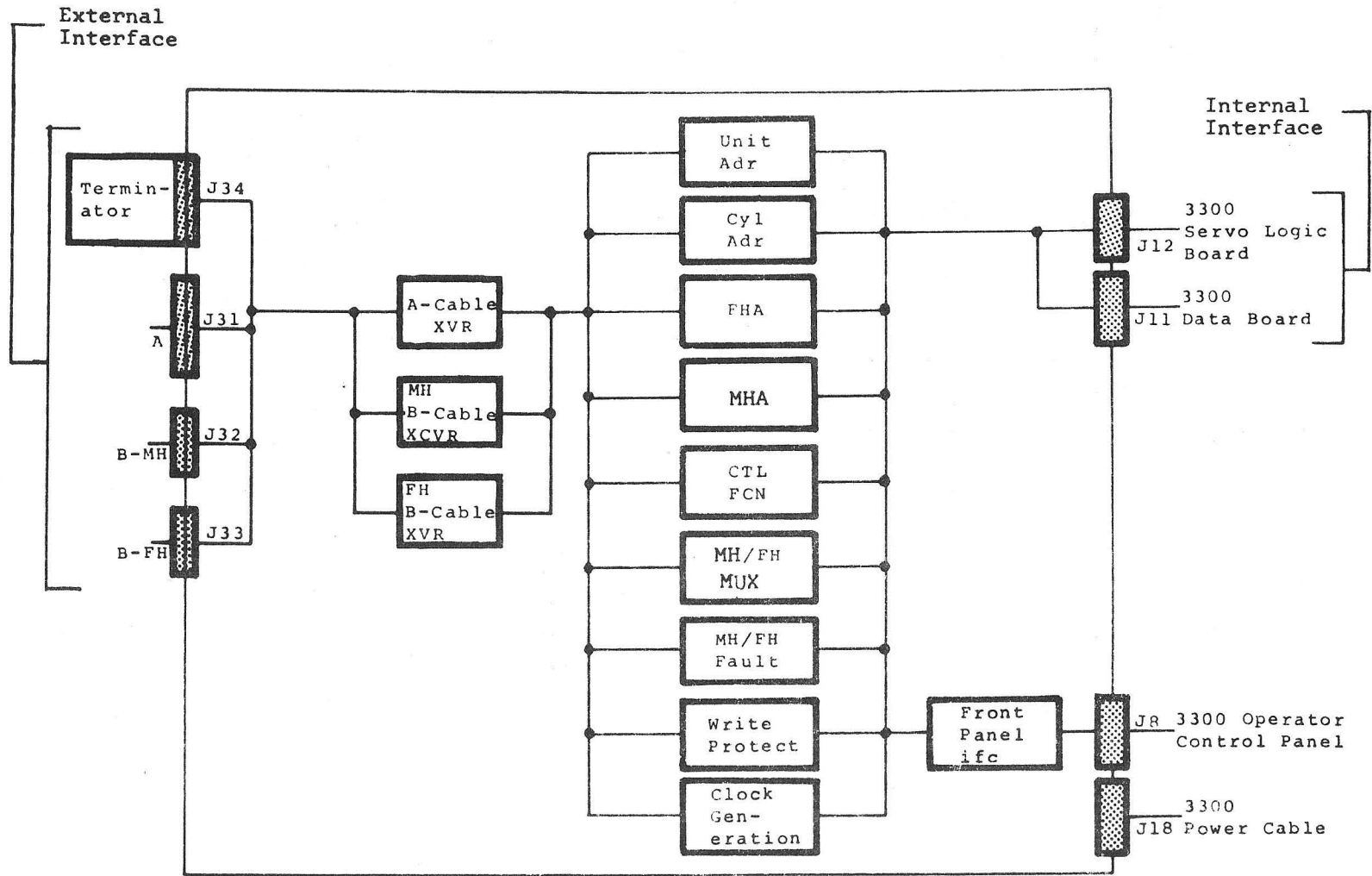
Figure 4-36
Interface Block Diagram

during an open cable condition; this is ____
accomplished by means of terms $\overline{DSA0}$ and $\overline{DSA1}$,
and $\overline{DSA2}$ (1U66). The A-Cable transmitters 1U61,
1U65, 1U70, 1U74, 1U77, 1U84 are only enabled
when either the moving head or fixed head unit is
selected; this is accomplished via signals USEL
and USEL2.

4.5.2.2 Differential Signal Characteristics

For a given differential signal pair, only one side
of the pair is conducting at a time. The non-
conducting side should be at 0VDC. The conducting
side should be at approximately -0.5VDC.

4.5.2.3 Cable Termination

All the A and B Cables must be terminated. The
A-Cable is terminated by a separate board, P/N
30116, which plugs into J34. This terminator
board connects each line to ground through 56
ohms except for pins 29 and 59 which are open,
and pins 30 and 60 which are ground. The A-Cable
may be daisy chained via J34 in which case the
terminator is plugged into the last drive of the
chain. The B-Cables are terminated to ground through
82 ohms on the I/O board; they may not be daisy
chained.

4.5.2.4 Moving Head B-Cable Transceiver

The Moving Head B-Cable Transceiver consists of
differential drivers and receivers which interface
to header J32. The transmitters (1U83, 1U85, 1U86)
are always enabled. The moving head write clock
receiver (1U67) is always enabled except during
open cable. The moving head write data receiver
(1U68) is only enabled when the moving head unit
is selected.

4.5.2.5 Fixed Head B-Cable Transceiver

The Fixed Head B-Cable Transceiver section
interfaces to J33. The transmitters (1U76, 1U81,
1U84) are always enabled. The receivers for fixed
head write data (1U68) and fixed head write clock
(1U67) are only enabled when the fixed head unit
is selected.

4.5.3   Unit Address Detection

The unit address from the A-Cable (UNIT SEL 0, UNIT
SEL 1, UNIT SEL 2), is strobed into a 4-bit latch
by UNIT TAG (2U50). The latched address is compared
(2U52, 2U63) against a preset moving head address and
a preset fixed head address (2U51). The preset unit
addresses may be specified by the Unit Address
Jumper (2U51) or by front panel hexadecimal
thumbwheel switches via J8 in which case the Unit
Select Jumper is a terminator to +5VDC. A thumb-
wheel switch bit is asserted by being connected
to switch common; otherwise it is pulled up to +5 volts.

Moving heads selected (MHSEL) is generated with
the following: the output of the moving head
address comparator (2U52) is high, an open cable
condition ($\overline{OPNCBL}$) does not exist, and the jumper
"MAINT" is not inserted (2U25, 2U26, 2U12). F/M
SEL to the Data Board is low when moving heads
are selected.

Fixed heads selected (FHSEL) is generated when
the output of the fixed head address comparator
(2U63) is high, $\overline{OPNCBL}$ is high and MAINT is high.
The fixed head disable jumper, "FHDSA", should only
be inserted when the fixed option is absent, where
2U63 is not loaded.

4.5.4   Cylinder Addressing

The Cylinder Address logic module involves the
cylinder address lines, cylinder address strobe,
servo offset, on cylinder, seek end generation
and seek error detection.

4.5.4.1 Cylinder Address Lines

The cylinder address lines are presented to the
Servo Board at connector J12 via signals BUS∅
thru BUS9 (1U73, 1U64, 1U79, 1U60, 1U59).

4.5.4.2 Cylinder Address Strobe

Seek strobe (SKSTR) is transmitted to the Servo Board
when the following conditions are present: moving head
unit selected (MHSEL), cylinder address strobe (TAG1),
and the unit is ready with no fault condition (URDY)
(2U25, 2U22, 2U8).

A test point, TP1, is provided which divides SKSTR
by two (2U2).

4.5.4.3   Servo Offset

Servo offset plus (SOFFP) or minus (SOFFM)
are generated in conjunction with signals BUS1,
BUS2, TAG3, RDY and USEL (3U12, 3U47, 3U33, 3U48).
The servo offset is sent to the Servo Board when the
moving head unit is selected (MHSEL) and offsets are
enabled (TOFFENA) (3U46, 3U30).

4.5.4.4   Track Offset Enable

The track offset enable signal (TOFFENA) is
generated by either SOFFP or SOFFM being issued
when the servo is on cylinder (ONCYL). TOFFENA
is cleared when servo offset is no longer asserted
or with seek strobe, moving head restore or power
reset (2U13, 2U28, 2U40, 2U57). In addition a
pulse (TPULS) is generated with either transition
of TOFFENA (2U14, 2U13).

TPULS triggers a 3 msec one-shot (2U38) which is
used to suppress on cylinder when the servo arm
is moving to/from the track offset.

4.5.4.5   On Cylinder

Moving head on cylinder (MHONCY) is generated
when both on cylinder time-outs (2U38) have elapsed,
when there is no moving head seek error (MHSKERR)
and when seek complete (SKCOMP) is true or when
TOFFENA is true (2U13, 2U38, 2U37, 2U28).

Fixed head on cylinder (FHONCY) is generated when
the 30 µs time-out (TMO) has elapsed, and when there
is no fixed head seek error (FHSKERR) (2U37, 2U38).

The on cylinder time-outs are triggered by any of
the following: seek strobe (SKSTR), fixed head strobe
(FHSTR), fixed head restore (FHRTZ), or moving head
restore (MHRTZ) (2U22, 2U23, 2U90).

4.5.4.6   Seek End Generation

Seek end is generated for both the moving and fixed
heads with either on cylinder or seek error when the
seek end time-out has elapsed.

Moving head seek end is generated with either
$\overline{\text{MHSKERR}}$ or $\overline{\text{MHONCYL}}$ when the moving head seek end
time-out ($\overline{\text{MHTMO}}$) is not in effect (3U87, 3U89).
$\overline{\text{MHTMO}}$ is generated by MHSEL and the 30 μs
on-cylinder time-out (TMO) (2U88).

4.5.4.7 Seek Error Detection

Moving head seek error ($\overline{\text{MHSKERR}}$) is generated
when either seek late (SKLATE) or illegal address
(ILL ADD) is detected from the Servo Board (2U9,
2U10, 2U11, 2U14). $\overline{\text{MHSKERR}}$ may only be cleared
by power on initialize (PWRRST) or moving head
restore ($\overline{\text{MHRTZ}}$) (2U25).

Fixed head seek error, $\overline{\text{FHSKERR}}$, is generated when
an illegal fixed address (ILLFHA) by the contiguous
fixed head address option (2U11, 2U14). $\overline{\text{FHSKERR}}$
may only be cleared by $\overline{\text{PWRRST}}$ or $\overline{\text{FHRTZ}}$ (2U25).

4.5.5   Head Addressing

4.5.5.1 Fixed Head Addressing

The fixed head address presented to the Data Board
must be latched on the I/O Board (3U4, 3U18); the
fixed head address may also be mapped through a
PROM (3U6) to provide contiguous addressing and
illegal address detection. In the event a PROM is
not used, a replacement jumper must be loaded at
U6 to pass the address to the 8-bit latch.

The fixed head address is received via signals
"BUS∅ thru BUS7" and passed thru the mapping PROM
or replacement jumper (3U6) to the 8-bit fixed
head address latch (3U4, 3U18). The fixed head
address latch is strobed by fixed head address
strobe (FHSTR), and is cleared by fixed head
restore ($\overline{\text{FHRTZ}}$). FHSTR is generated with TAG1
when FHSEL is true (3U32).

Illegal fixed head address ($\overline{\text{ILLFHA}}$) is only supp-
orted with the contiguous fixed option. $\overline{\text{ILLFHA}}$
may also be generated in the non-contiguous mode
if an illegal fixed head amplifier is selected.
$\overline{\text{ILLFHA}}$ is generated when two illegal PROM bits are
present with TAG1 and FHSEL (3U6, 3U58).

4.5.5.2 Moving Head Address

The moving head address on signals BUS0 thru BUS3
is strobed in a 4-bit latch (2U5) when TAG2 and
MHSEL are present (2U30). This latch is cleared
by MHRTZ. The outputs of the moving head address
latch are sent to the Data Board and are also used
to detect when head 0 is addressed, HD0 (2U23).

4.5.6 Control Functions

The following control functions are initiated via
signals BUS0 through BUS9 in conjunction with TAG3:
read, write, servo offset, fault clear, address mark,
restore, data strobe offset and release which is used
in margin mode.

The control functions may pertain to the moving head
unit only, the fixed head unit only or both units.
The enabling of the particular control functions
requires the presence of the following: TAG3;
disc ready (RDY) and either MHSEL or FHSEL (3U12,
3U32, 3U30, 3U33, 3U47). A by-product of these
control function enable signals are the unit select
signals, USEL and USEL2, which are used to enable
differential transmitters (1U61, 1U65, 1U74, 1U82,
1U77).

4.5.6.1 Write Control Function

Two write request signals, WTREQ1 and WTREQ2,
are generated in response to BUS0 and control
function enable (TAG3) (3U19, 3U16, 3U33).

Write enable (WRT ENA) is generated if the write
mode signal (WRT MODE) is true and an address mark
is not being written (ADRMK) (3U32, 3U33).

The write mode signal (WRT MODE) is generated in
response to the WTREQ1 signal in combination with
one of three possible conditions. One condition is
the presence of margin mode (MMODE) which overrides
all interlocks in creating WRTMODE in response to
WTREQ1. The second condition is moving head write
where the following is required: the unit must be
ready with no fault condition (URDY), the moving
head unit is selected (MHSEL) and no moving head seek
error (MHSKERR) nor moving head fault clear (MHFCL)
is present. The third condition is fixed head write

where URDY and FHSEL must be present and
FHSKERR and FHFCL must be absent, i.e. logic
high (2U35, 2U39, 2U16).

4.5.6.2 Read Control Function

Read enable (RDENA) to the Data Board and the
read request signal RDREQ are generated in
response to BUS1 and control function enable
(TAG3). RDENA is suppressed during address mark
detect (3U19, 3U33).

4.5.6.3 Servo Offset Control Function

Servo offset plus and minus (SOFFP) and (SOFFM)
are generated by BUS2 and BUS3, respectively,
in combination with control function enable (TAG3)
(3U48). Track offset to the Servo Board is
generated in response to SOFFP or SOFFM, MHSEL
and TOFFENA (3U30, 3U46); TOFFENA is discussed in
paragraph 4.5.4.4.

4.5.6.4 Fault Clear Control Function

Moving head fault clear (MHFCL) and fixed head
fault clear (FHFCL) cause the associated fault
latch to be cleared. MHFCL and FHFCL are
generated in response to BUS4 in combination with
the appropriate control function enable signal
(3U19, 3U34).

4.5.6.5 Address Mark Control Function

The address mark control causes address marks to be
generated when issued in conjunction with write
control function. When the address mark control is
issued in conjunction with the read control function,
detection of address marks is enabled while RDENA
to the Data Board is disabled. The address mark
control (ADRMK) is generated in response to BUS5
in combination with the control function enable
signal (TAG3)(3U48).

4.5.6.5.1 Address Mark Generation

Address marks are written by issuing write address
mark (WRTADDMK) to the Data Board while write enable
(WRTENA) is absent. This is accomplished by
combining WRTMODE with ADRMK to generate WRTADDMK
and WRTENA (3U46, 3U32, 3U33).

4.5.6.5.2 Address Mark Detection

Address mark detection is enabled when address mark
control ($\overline{\text{ADRMK}}$) is present in combination with read
request (RDREQ) (3U31). Address mark found (AMKFND)
is generated following detection of the address mark
gap. If the optional address mark detection circuit
is not implemented, AMKFND is grounded via the "AMK"
jumper.

The differential read analog signal (RD ANALOG DATA)
is low-pass filtered and amplified to approximately
6 volts peak-to-peak differentially (U91). The ampli-
fied signal is then converted to a series of pulses
(DPLS) corresponding to the presence of detected flux
changes on the amplified analog data; this is ac-
complished by setting a DC bias on one leg of the
differential input to the high speed comparator (U92),
see Figure 4-37. During an absence of flux changes,
which is the case during an address mark, DPLS is
high as illustrated in Figure 4-37. To detect a 16-
bit gap of missing flux changes, DPLS is used to pre-
set a 4-bit counter at each detected flux change
(U93). This same counter is clocked down by bit
clock (BIT CLK) to zero in which case a latch (U95)
is set to indicate that a gap of at least 16 bits has
been detected. Due to the exponential turn-on and
turn-off properties of RD ANALOG DATA, the counter is
set to count 8 clock transitions for qualifying the
presence of an address mark gap. The first transition
of DPLS following the detected gap causes the next
latch to be set high (U95) which initiates the 9 micro-
second one-shot (U94) to issue the address mark found
pulse (AMKFND), see Figure 4-37.
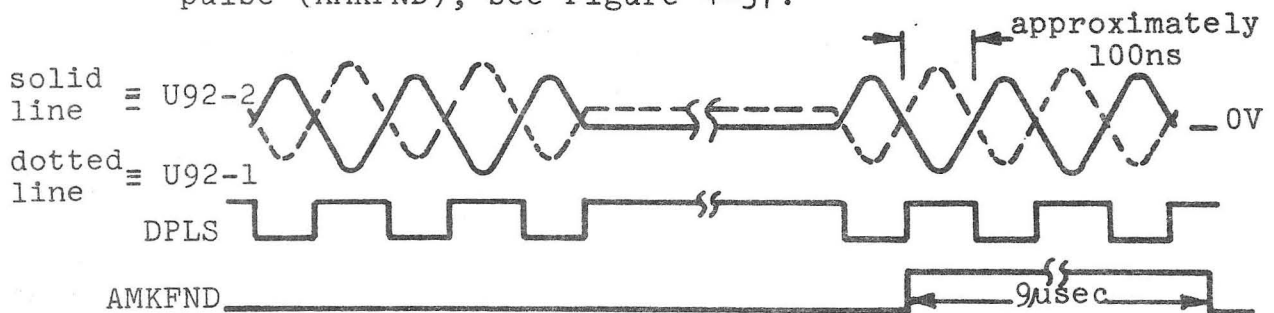
Figure 4-37
Address Mark Detection

4.5.6.6   Restore Control Function

Moving head restore ($\overline{\text{MHRTZ}}$) and fixed head restore ($\overline{\text{FHRTZ}}$) are generated in response to BUS6 in combination with the appropriate control function enable signal (3U7, 3U34). $\overline{\text{RESTORE}}$ is issued to the Servo Board in response to $\overline{\text{MHRTZ}}$ (3U8).

4.5.6.7   Data Strobe Offset Control Function

Data strobe early ($\overline{\text{STR EARLY}}$) and data strobe late ($\overline{\text{STR LATE}}$) are issued to the Data Board in response to BUS7 and BUS8, respectively, in combination with the control function enable signal (3U34).

4.5.6.8   Release Control Function (Margin Mode)

The release control function (RLS) is generated in response to BUS9 in combination with the control function enable signal (3U48).

The release function, normally intended for use with dual port disc drives, is used to generate margin mode (MMODE) when unit addresses 15 or 16 are selected (UNIT SEL1 through UNIT SEL3) (2U58, 2U8). MMODE is issued to the Data Board to cause narrow data windows during read. MMODE is used to override fault conditions and allow write enables.

4.5.7   Moving/Fixed Head Multiplexer

Certain signals from the fixed and moving head unit must be multiplexed onto the A-Cable. These multiplexed signals are as follows: MHSKERR and FHSKERR to SKERR: MHFLT and FHFLT to FLT: and MHONCY and FHONCY to ONCYL (3U72).

Write clock (WRITE CLOCK) and write data (WRITE NRZ) to the Data Board must be multiplexed from moving head write clock (MHWCLK) and fixed head write clock (FHWCLK) and from moving head write data (MHWDAT) and fixed head write data (FHWDAT) (3U62), respectively. The moving head signals are disabled only when the fixed head unit is selected.

4.5.8   Moving/Fixed Head Fault

Faults are latched for the moving head unit and for the fixed head unit (MHFLT) and (FHFLT) (2U11, 2U9). Unit ready (URDY) for the selected unit indicates that the drive is ready (RDY) and that no fault exists for the selected unit (FLT) (3U32, 3U33).

Faults into the moving head fault latch (2U11) are gated thru an 8-input gate (2U21) whose output is gated to the moving head fault latch only when the moving heads are selected (MHSEL) (2U22, 2U10). Powerfail ($\overline{PWRFLT}$) and moving head write current error are enabled to the moving head fault latch at all times (2U10). The moving head fault latch is cleared by power on initialize ($\overline{PWRRST}$) or moving head fault clear ($\overline{MHFCL}$) (2U11).

Faults into the fixed head fault latch (U11) are gated thru an 8-input gate (2U49) whose output is gated to the fixed head fault latch only when the fixed heads are selected (FHSEL) (2U7, 2U10). $\overline{PWRFLT}$ and fixed head write current error are enabled to the fixed head fault latch at all times (2U10). The fixed head fault latch is cleared by power on initialize ($\overline{PWRRST}$) or fixed head fault clear (FHFCL).

4.5.9   Fault Conditions

There are a number of different fault types which set the moving and fixed head fault latches. These are discussed in the following paragraphs.

4.5.9.1   Control Fault

This fault condition ($\overline{CTLFLT}$) is generated if the fixed head unit (FHSEL) and moving head unit (MHSEL) are simultaneously selected (2U40) or if multiple tags (TAG1) (TAG2) (TAG3) are received while either unit is selected (USEL) (2U36, 2U37). This fault condition is monitored by both fault latches only when a unit is selected (2U21, 2U49).

4.5.9.2   Power Fault

This fault condition ($\overline{PWRFLT}$) is generated when a DC power error (PWROK) occurs not coincident with power on initialize (PWRRST) (2U7). This fault condition is monitored by the fault latches independent of a unit select (2U10).

4.5.9.3   Read While Write Fault

This fault condition is generated when read (RDREQ) and write (WTREQ2) are on simultaneously (2U22). This fault condition is monitored by the fault latches only when a unit is selected (2U49).

4.5.9.4 Write While Track Offset Fault

This fault condition is generated when write
(WTREQ2) is attempted during track offset (TROFF).
This fault condition is suppressed during margin
mode (MMODE) (2U47). Track offset write fault is
monitored by both fault latches only when a unit
is selected (2U21, 2U49).

4.5.9.5 Read or Write While Off Cylinder Fault

This fault is generated when read (RDREQ) or
write (WTREQ) is attempted when the selected unit
is not on cylinder (ONCYL) (2U8, 2U6). This con-
dition is monitored by both fault latches only
when a unit is selected (2U21, 2U49).

4.5.9.6 Multiple Moving Heads Selected

This fault is generated in response to a Data
Board signal (MHD MULTI SEL) (2U16). This con-
dition is only monitored by the moving head fault
latch when the moving head unit is selected (2U21).

4.5.9.7 Moving Head Write Current Fault

This fault is generated when moving head write
current (MHD CUR SENS) is detected and there is
no write to the moving heads. It will also be
generated if there is a moving head write and no
write current is detected (2U3, 2U9, 2U30). Resistor,
2R6, and capacitor, 2C3, filter out the time lag be-
tween write enable and current sense. This condition
is monitored by the moving head fault latch at all
times. (2U10).

4.5.9.8 Multiple Fixed Heads Selected

This fault is generated in response to the Data
Board (FHD MULTI SEL) (2U16). This condition is
only monitored by the fixed head fault latch when
the fixed head unit is selected (2U49).

4.5.9.9 Fixed Head Write Current Fault

This fault is generated when fixed head write
current (FHD CUR SENS) is detected and there is
no write to the fixed heads. It will also be
generated if there is a fixed head write and no

write current is detected (2U3, 2U9, 2U37).
Resistor, 2R7, and capacitor, 2C2, filter out the
time lag between write enable and current sense.
This condition is monitored by the fixed head
fault latch at all times (2U10).

4.5.9.10 Write Fault

Fixed head and moving head write faults are also
detected ($\overline{\text{FHWFLT}}$) and ($\overline{\text{MHWFLT}}$) (2U41). These con-
ditions are monitored by the moving and fixed head
fault latches only when a unit is selected (2U21,
2U49). For a further discussion see paragraph
4.5.11.2.

4.5.10 Write Protect

Write protect consists of reporting when a write
protected section of the drive is addressed, WPROT,
and of indicating when a moving head or fixed head
write fault occurs ($\overline{\text{MHWFLT}}$) and ($\overline{\text{FHWFLT}}$). The def-
inition of write protected areas is received from
the optional front panel interface section WPHØ,
WPFH or WPED.

4.5.10.1 Write Protect Status

The write protect status, WPROT, is generated when
a write protected section of the drive is selected.
Write protected sections are: fixed heads ($\overline{\text{WPFH}}$),
moving head zero (WPHØ), or the entire drive ($\overline{\text{WPED}}$)
(2U40, 2U42). This logic (2U42) is optional and
may not be loaded. If it is not used, the "WPD1"
jumper must be inserted; if it is used, "WPD1"
must be removed.

4.5.10.2 Write Fault Detection

Write fault detection ($\overline{\text{MHWFLT}}$) and ($\overline{\text{FHWFLT}}$) is
determined during a write (WTREQ1) if a write pro-
tect violation occurs. This is accomplished by
monitoring: the write protect definition signals
(WPFH), (WPED) and (WPHØ), the write request signal
(WTREQ1), and head address zero (HDØ) (2U41). A
write fault status may be generated during a write
but it is only latched into the moving head or fixed
head fault latch if the appropriate unit is selected.
Write fault detection is optional, and is included
in the write protect option. If 2U41 is not loaded,
jumpers "WPD2" and "WPD3" must be inserted. Con-
versely, "WPD2" and "WPD3" must be removed if 2U41
is loaded.

4.5.11   Control Panel Interface

The front panel interface connects to header, J8,
and receives write protect definitions, controls
the write protect displays, receives unit address
definitions and controls the ready indicator.

4.5.11.1 Write Protect Interface

The write protect momentary push button switches
and indicators are optional and are included in
the write protect option. These switches and
indicators are labelled: "Write Protect Moving
Head Zero", "Write Protect All Fixed Heads",
"Write Protect Entire Drive". Each switch input
is filtered (2R25, 2R26, 2R27, 2C60, 2C61, 2C62),
buffered and levelled (2U53), and latched (2U56,
2U57). The latches, WPHØ, WPFH, WPED are D-type
flip-flops which change state each time the asso-
ciated switch is depressed; all the write protect
switches are initialized at power-on to the non-
write protect condition.

The outputs of the latches are used in write pro-
tect status and in write fault detection. The
write protect indicators reflect the state of the
associated latch, ie., if WPHØ is true, then the
"Write Protect Moving Head Zero" indicator is lit.
The write protect indicators are controlled by
peripheral interface drivers (2U54, 2U55) which
sense the output of the appropriate write protect
latch and conditionally provide a current path to
ground for the associated 28 volt lamp. 32 VDC
is provided to the lamps from the I/O board through
J8. The output of each peripheral driver has a
series resistor (2R28, 2R29, 2R31) for current
limit and a bleeding resistor (2R32, 2R33, 2R34)
to increase lamp life.

4.5.11.2 Unit Select Interface

The front panel may optionally contain a moving
head unit address thumbwheel switch and a fixed
head unit address thumbwheel switch. These
switches are 16 position switches, each with four
outputs and a common; for a given output, a true
condition is indicated by a connection to the switch
common. The switch output lines are terminated by
the Unit Address Jumper (2U51) if the unit address
option is provided. For further details refer to
paragraph 4.5.3.

4.5.11.3 Ready Indicator Interface

The front panel ready indicator provides the operator with the status of the drive. The light remains off until the RDY signal from the Servo Board goes true and no fault exists at which time the light comes on. If RDY drops or a fault condition exists, the light will flash at ten times per second until RDY returns high or the fault is cleared (2U35, 2U8, 2U27). Jumpers "FLT1" and "FLT2" determine which fault conditions may flash the ready light. If only "FLT1" is inserted, then either a fixed head or moving head fault will flash the ready light. If only "FLT2" is inserted, then only a moving head fault will flash the ready light. Inserting both "FLT1" and "FLT2" is not permitted. The 10Hz oscillator is a free-running oscillator whose output is used to flash the light (2U24, 2U26).

The ready lamp is controlled by a peripheral interface driver (2U55) which provides a path to ground when the lamp is to be on. The ready light is a 28V lamp running on 32V and is switched to ground through a limiting resistor (2R30) when on, and bled by 2R35 when off, to increase the lamp life.

4.5.12 Clock Generation

The following clock signals are derived from Servo Board signals and transmitted to the controller interface: BITCLK, SECT and INDEX.

4.5.12.1 Bit Clock Generation

The double frequency clock signal, 14MHZ, from the Servo Board is used to generate the 7.97 MHZ BITCLK. The signal is terminated by 3R4 and 3R5, Schmidt triggered (3U16) and divided by two (3U2) to become BITCLK.

4.5.12.2 Sector and Index Generation

Transmitted sector marks and index marks are derived from the Servo Board signals, 460KHz and INDEXA. 460KHz is 1/16 the frequency of BITCLK and is used in conjunction with INDEXA to generate sector marks. Each cycle of 460KHz corresponds to 16 data bits or 2 data bytes; thus, the spacing between sector marks is controlled in 2-byte increments. Sector spacing is controlled by a 12-bit down counter (3U29, 3U15, 3U1) which counts down the number of 16-bit words per sector as defined

by the Sector Mark Jumper (3U43). Index A is
used to resynchronize the sector marks and to
derive a skewed index for the controller allow-
ing for an oversized sector at the end of the
revolution if the number of sectors do not exact-
ly occupy one data track.

INDEXA is synchronized with 460KHz to cause the
12-bit counter to be preset with the number of
words per sector (3U8, 3U47, 3U31, 3U45). Like-
wise, the carry-out of the 12-bit counter is
synchronized with the 460KHz clock to cause the
counter to be preset. Each carry-out of the 12-
bit counter also triggers two one-shots (3U44).
However, only one of the one-shots is enabled
(3U45) as determined by INDEXA. The first carry-
out after INDEXA becomes INDEX to the controller,
all subsequent carry-outs become sector marks,
SECT, to the controller.

SECTION V

MAINTENANCE AND ADJUSTMENTS

5.0   <u>INTRODUCTION</u>

Before any 3300 disc drive leaves the factory,
each of its components has been thoroughly tested
and all adjustments have been made to ensure
reliable operation. However, rough handling in
transit or the effect of long use may necessitate
the replacement of some parts or the adjustment
of some components.

This section provides instructions for replacements,
readjustments, and trouble shooting that can
effectively be done while the disc drive remains
installed in the customer's system. Some repairs
will require test equipment or tools not normally
available in the field. Instructions for repairs
of this more complex nature are <u>NOT</u> included in
this section.

5.1 PRECAUTIONS

The 3300 uses heads which remain in contact with the disc surface when the discs are not rotating. A "landing zone" is provided on the discs for each head and the head positioner will automatically position the heads to this zone and hold them there with a permanent magnet when power is removed from the drive. (Fig. 4-4.)

The strength of the permanent magnet is such that the disc drive can be removed from its cabinet and placed in its service position (Fig. 5-1) without danger of the heads leaving the "landing zone" providing the machine is not allowed to experience shock or vibration.
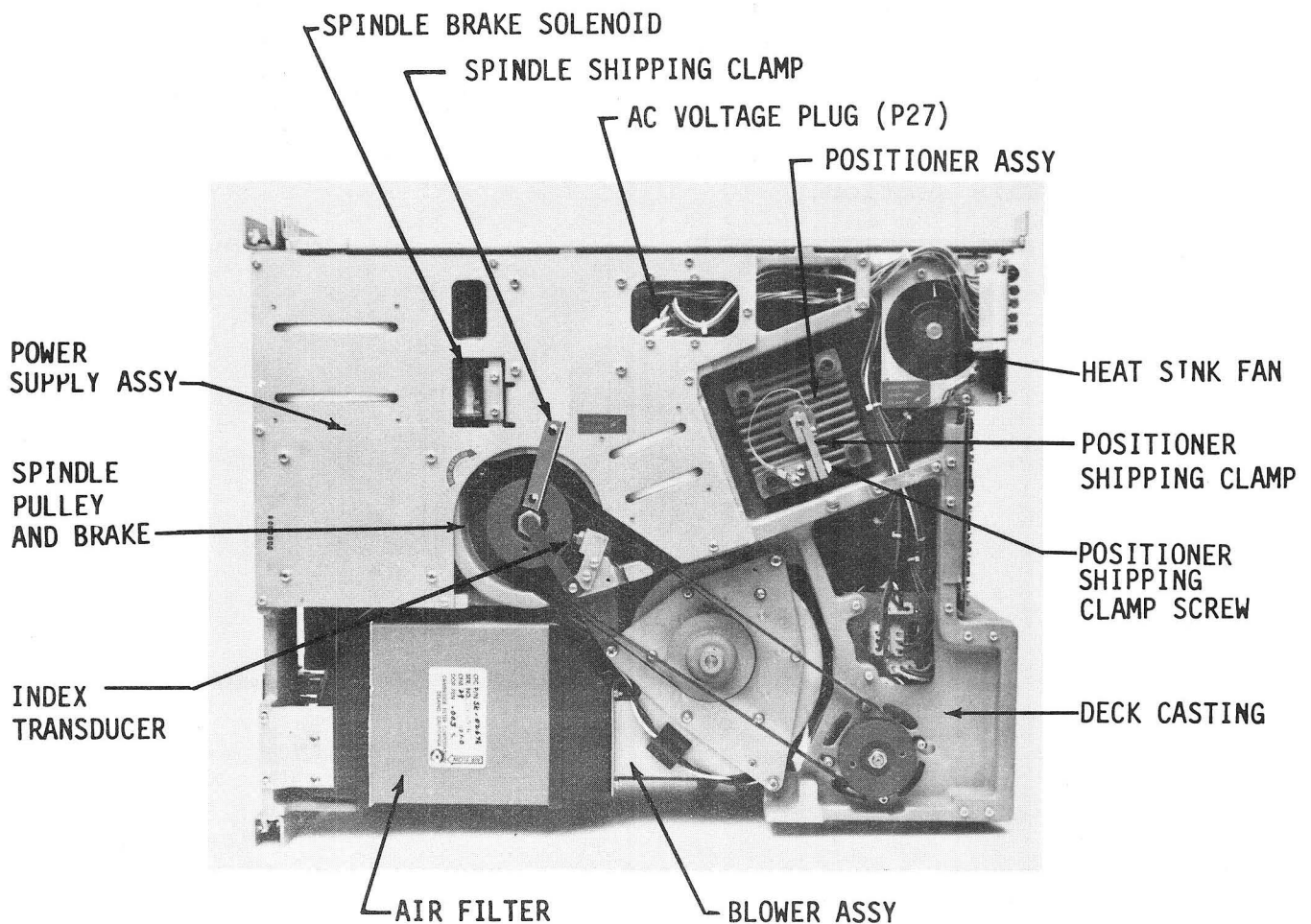
Figure 5-1
Machine in Service Position

NOTE: Serious damage to heads and discs can occur if:
(1) The positioner is moved off of the "landing zone" when the discs are not up to speed.
(2) Discs are rotated counter clockwise as viewed from the bottom at any time.

It is therefore recommended that for any maintenance operation requiring removal of the machine from its rack or enclosure that the positioner shipping clamp and spindle shipping clamp first be fastened (Fig. 5-1).

If the machine is to be shipped to another location these clamps must first be fastened.

5.2 TOOLS AND EQUIPMENT

The following tools and equipment will allow all adjustments and repairs covered in this section to be completed efficiently.

EQUIPMENT	MODEL OR TYPE
Voltmeter	50mv Accuracy
Potentiometer Screwdriver	
Pin Extractor Tool	Molex P/N 11-03-0015
Clip on Jumper Wire	
Oscilloscope	Tektronix 465 or Equiv.
Scope Probes (2)	
Dip Clip	14 Pin & 16 Pin
Soldering Iron	<20W
Phillips Screwdriver	#1 & #2
Spring Scale	Chatillon DPP-5
Hex Driver Set	Bondhus
Silicone Rubber	RTV 162
Steel Scale	18" & 6" 10th & 100ths Grade
Hypodermic Syringe	
Open End Wrench (2)	5/16
Spin Tite	1/4 in
Socket & Ratchet Set	3/8 Drive
Pulley Spanner	Okidata 30244
Pulley Puller	Okidata 30282
Current Probe	Tektronix P6021 with terminator or equivalent

TOOLS AND EQUIPMENT (Continued)

EQUIPMENT	MODEL OR TYPE
Pliers	Needle Nose & Plain
Retaining Ring Pliers	#2 Milbar or Equiv.
Gear Puller	2 Jaw Williams GP-240
Locktite	271
Cotton Swabs	
100% Isopropyl Alcohol	
Shim	.020 & 040 THK.
Switch Lamp Remover	3/16 diameter shrink tube 1" long - PVC-105 preferred

5.3   POWER SUPPLY (Set Transformer Taps)

a) Tools Required: Molex P/N 11-03-0015 extractor

b) The power supply input taps are accessible from
    bottom of drive. See Fig. 5-2 (A/C Voltage Plug).
    These taps can be selected to match as nearly as
    possible the line voltage. Figure 5-2 shows how
    to select the taps for the line voltage in a
   given application.

NOTE: 1. Do not switch the transformer taps from
          105, 110, 115, 120 to 210,220, 230, 240
          or vice versa. This change requires a
          spindle motor and AC Distribution Box
          change (P/N 30337), in addition to the
          change of transformer taps.

       2. Verify power supply revision - Revision
          A and B have no revision level marked
          on power supply. Revision C is marked
          with revision level C on bottom of power
          supply assembly.

5.3.1   Power Supply Removal

To remove the power supply assembly from the drive,
the following procedure is to be followed:

a) Tools Required: #2 phillips screwdriver

b) Remove drive from cabinet and position vertically
    on left hand side of drive as shown in Fig. 5-3.

c) Disconnect AC voltage plug (P27) and power ampli-
    fier connector (P15) where shown in Fig. 5-1.
    NOTE: Remove cable clamps before removing
           power amp. connector (P15).

d) Remove the ten power supply mounting screws
    circled "A" in Fig. 5-3. The power supply
    can now be removed from the drive. (Fig. 5-4).

e) Re-install power supply assembly in reverse
    order of removal.

f) Check to see that no binding or interference
    with the spindle brake operation exists.
    Install drive in cabinet.
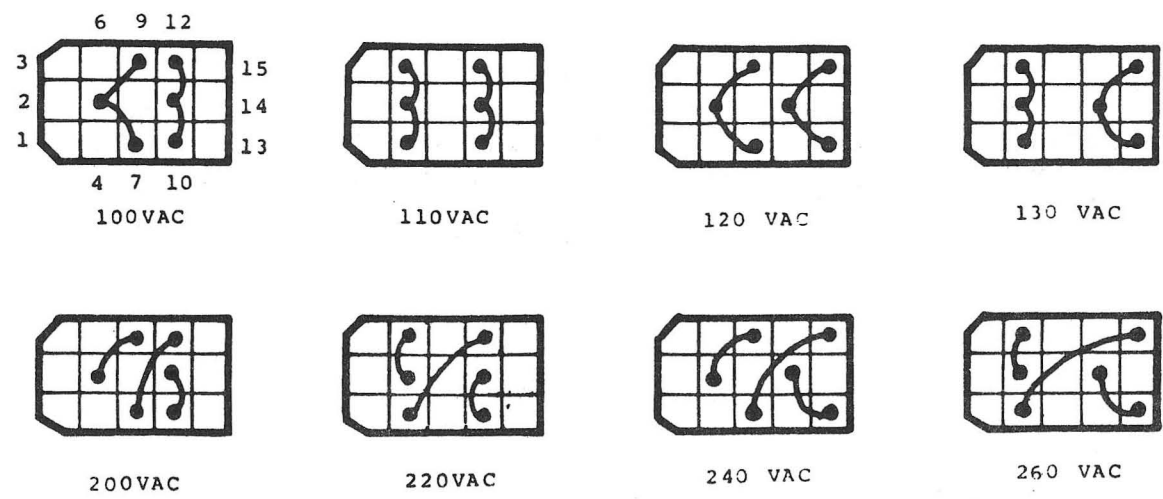
Rear of P27 Shown

Figure 5-2
Transformer Tap Wiring
Revision A, B Power Supplies

```
        6   9  12
    3  ┌─────────┐  15
    2  │  ><  >  │  14
    1  └─────────┘  13
        4   7  10
         105VAC          110VAC          115VAC          120 VAC


         210VAC          220VAC          230VAC          240 VAC
```
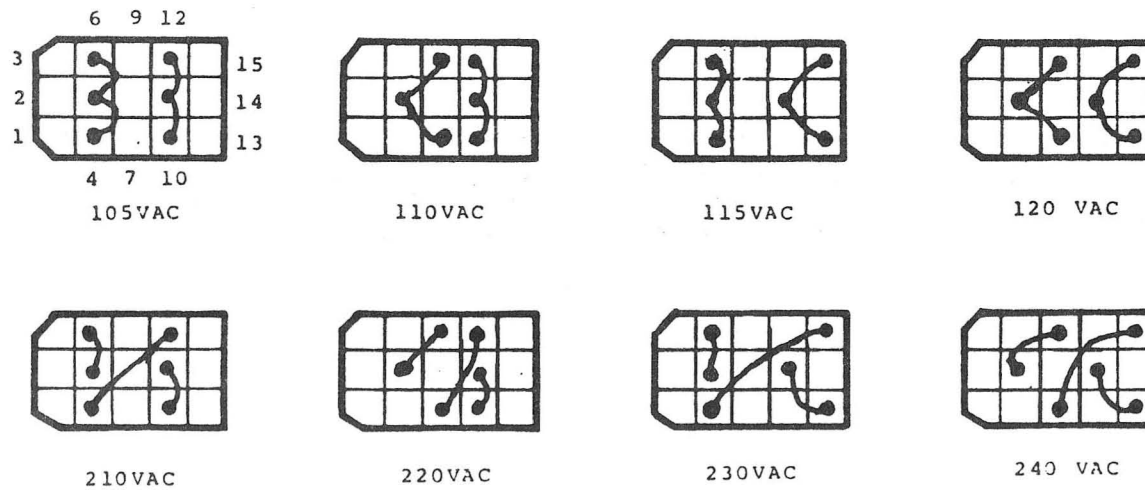
Rear of P27 Shown

Figure 5-2
Transformer Tap Wiring
Revision C and Later Power Supplies

POWER SUPPLY ASSY — A/C VOLTAGE PLUG P27 — CABLE CLAMP

PWR AMPLIFIER CONNECTOR (P15)

PWR SUPPLY MOUNTING SCREWS (10 PLCS)

SOLENOID PLUG P17

Figure 5-3
Power Supply

POWER SUPPLY ASSY

Figure 5-4
Power Supply Removal

5.4   POWER AMPLIFIER (SET ±5V.)
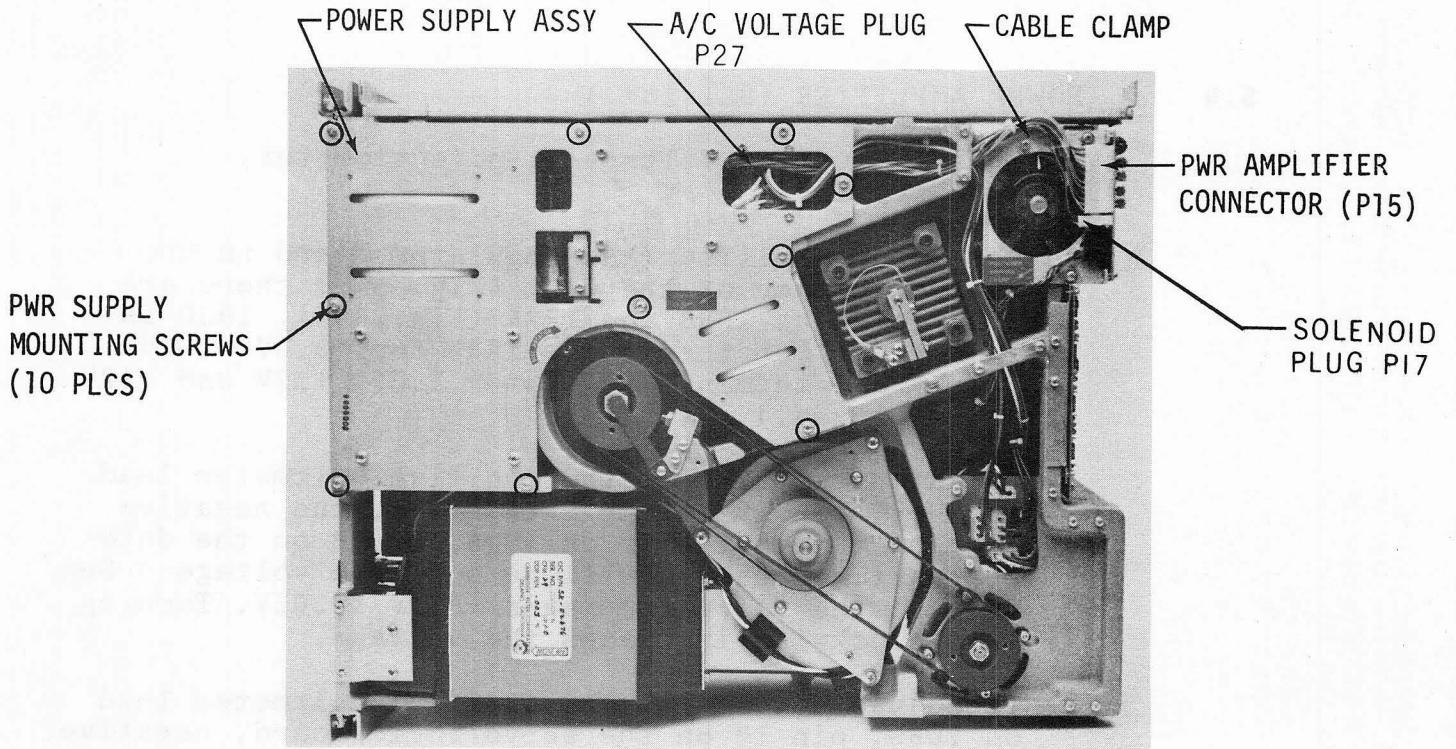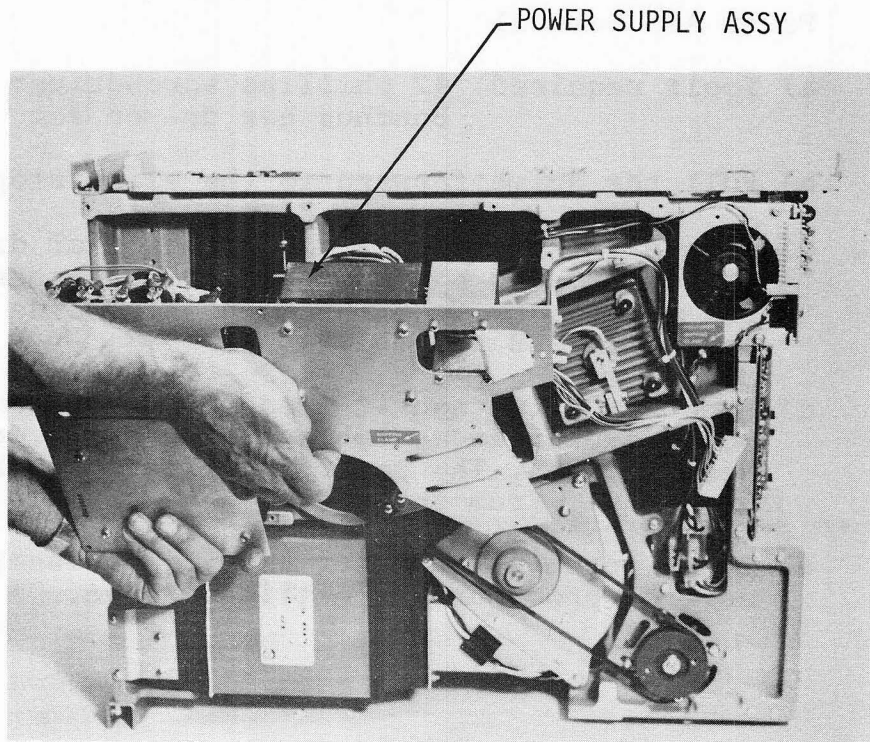
a) Tools required: Voltmeter, potentiometer, screwdriver

On the power amplifier and regulator board on the right rear corner of the unit (Fig. 5-9) there are 2 potentiometers 1R30 and 1R35 (Fig. 5-5). 1R30 is an adjustment for the -5.2V, 1R35 for +5.0V. (-2V is set by a 3 terminal regulator I.C., +32V and -32V are unregulated.)

b) To adjust -5.2V: Put the positive voltmeter lead on 3U48, pin 16 on the data board, the negative lead of the voltmeter on 3U48, pin 8 on the data board. (The reading will be positive voltage.) Set 1R30 so the voltmeter reads +5.2V ±0.05V. Turning 1R30 clockwise increases the voltage.

c) To adjust +5.0V: Put the positive voltmeter lead on 2U69, pin 14 on the servo/logic board, negative lead on 2U69, pin 7. Adjust 1R35 so the voltmeter reads +5V ±.05V. Turning 1R35 clockwise increases the voltage.

5.4.1   Power Amp Removal

a) Tools required: #2 phillips screwdriver
                   Bondhus hex driver set

b) Pull the drive forward to the slide stops.

c) Remove the connectors (from bottom of drive) that connect to the power amplifier PCB assembly. Remove the connectors from the right hand side of the power amplifier PCB assembly.

d) Remove the two socket head screws that mount the power amplifier assembly to the drive deck casting. See Fig. 5-6. The power amplifier assembly can now be removed from the drive.

e) To re-install the power amplifier assembly follow reverse procedure as outlined above.

R30 POTENTIOMETER ————————————

R35 POTENTIOMETER ————————————

PWR AMP PCB MTG SCREW ————————————
(MOUNTS TO FAN MTG BRACKET)
2 PLCS

F4 FUSE (10 AMPS) ————————————
F3 FUSE (10 AMPS) ————————————
F2 FUSE (4 AMPS) ————————————
F1 FUSE (5 AMPS) ————————————
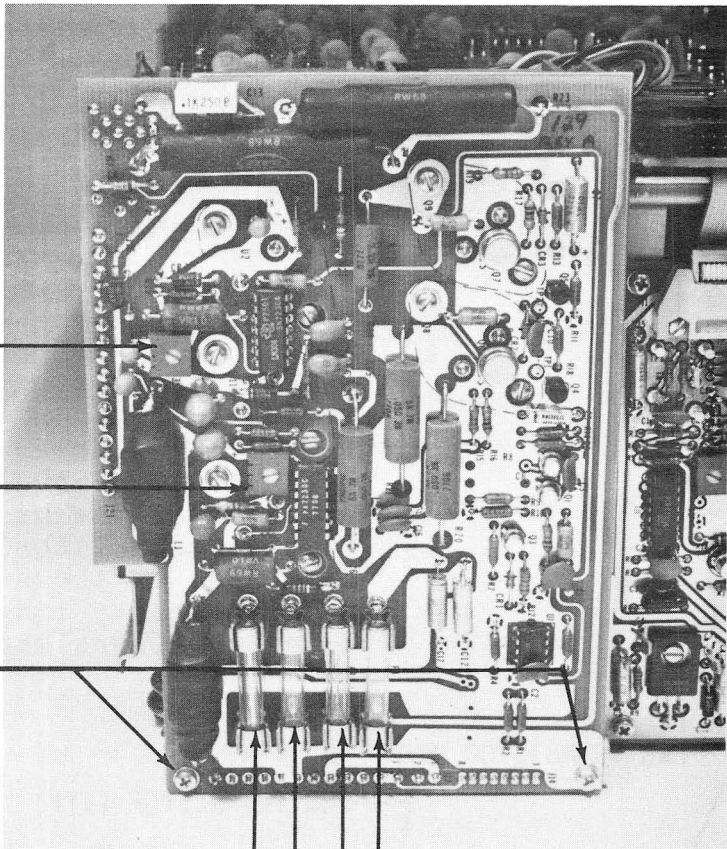
Figure 5-5
Power Amplifier Board

BONDHUS HEX DRIVER ————————————

POWER AMP ASSY
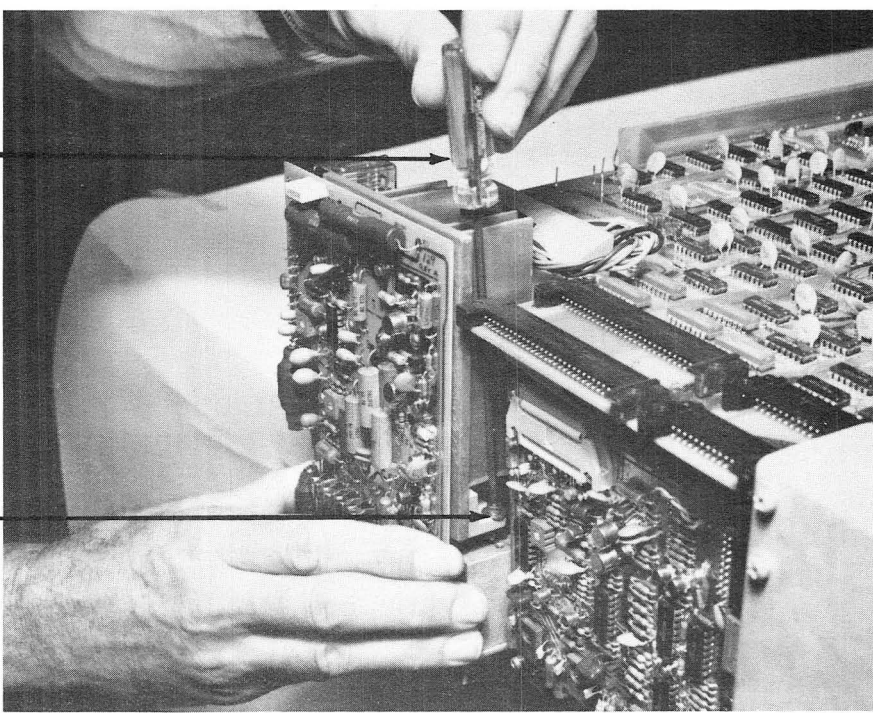MOUNTING SCREW (2 PLCS) ————————————

Figure 5-6
Power Amplifier Removal

5.4.2   Power Transistor Replacement

   a) Tools required: #1 phillips screwdriver
                         Bondhus hex driver set
                         Kimwipe tissue or equivalent
                         Silicone heat sink compound

   b) Remove power amplifier assembly from driver per
      sec. 5.4.1.

   c) To replace a power transistor (1Q8, 1Q9, 1Q11,
      1Q12, 1U2), remove the two mounting screws from
      PCB side of the assembly which removes the de-
      fective transistor's mounting plate on the heat
      sink side of the assembly. See Fig. 5-7. With
      mounting plate and screws removed, remove the
      defective transistor.

PWR TRANSISTOR MTG PLATE (TYP)
                    PWR TRANSISTOR (TYP)

PWR TRANSISTOR MOUNTING
    SCREWS (TYP 5 PLCS)

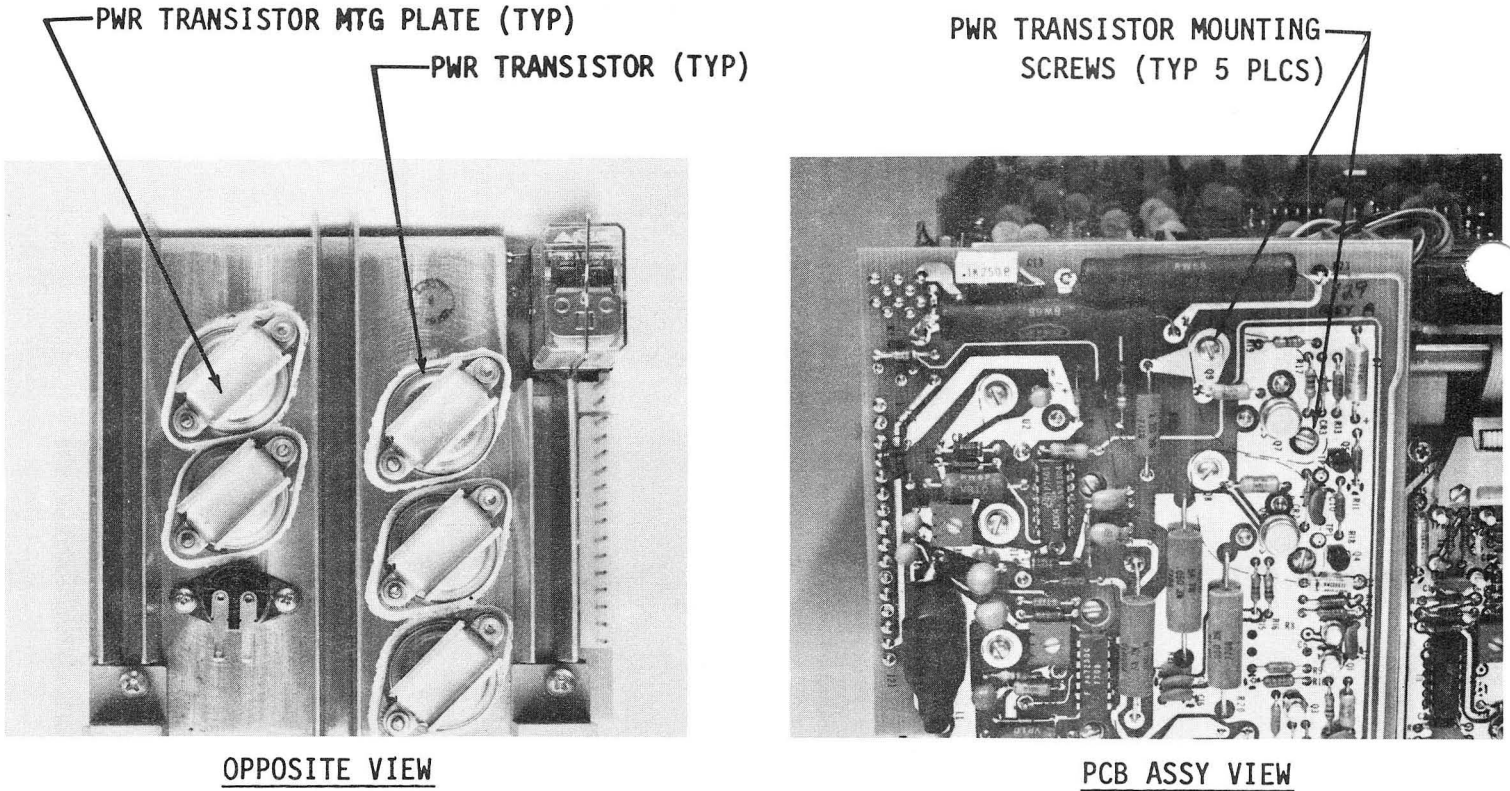OPPOSITE VIEW   PCB ASSY VIEW

Figure 5-7
Power Transistors

Also remove the mica insulating washer and all
silicone grease using the kimwipe tissues.

Install the new mica insulator (Thermalloy part
no. 56-03-2AP) after coating both sides with silicone
heat sink compound. Install the new transistor into

the sockets in the power amplifier PCB assembly.
NOTE: Make sure the leads on the transistor are
straight and not bent. If the leads are not straight
they will not line up with sockets in the PCB.

d) Re-install the mounting plate screws previously
removed and mount the assembly to the drive deck
casting per 5.4.1.

5.4.3   Pwr Amp PCB Removal (P/N 30105) (Fig. 5-8)

a) Tools required: #1 phillips screwdriver

b) Remove the two screws which mount the Pwr amp PCB
to the fan mounting bracket. See Fig. 5-5.
Disconnect all connectors from PCB.

c) Remove the five screws which are on top of the
PCB which mount one end of each power transistor
to the heat sink.
NOTE: DO NOT REMOVE OR LOOSEN THE SCREWS WHICH ARE
LOCATED BELOW THE PCB AT EACH TRANSISTOR LOCATION.

d) Remove the PCB from heat sink.
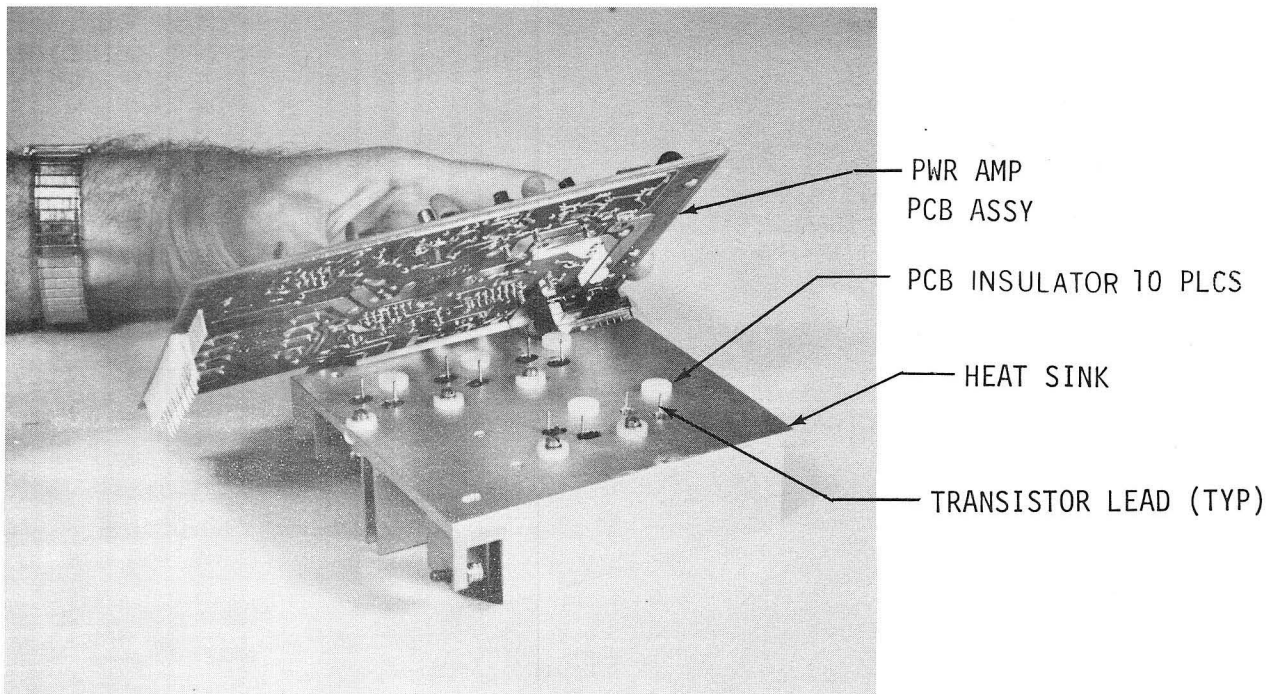
e) Re-install in reverse order as noted above.

Figure 5-8
Power Amplifier Board Removal

5.5   <u>PCB ASSEMBLY REMOVAL</u>

a) Tools required: #1 phillips screwdriver
                     #2 phillips screwdriver

b) Pull the drive forward out of the cabinet to slide
   stops. Remove the top cover by removing the five
   top screws and the two screws on each side of
   the drive.

c) With the top cover removed the mounting screws
   which mount the PCB assemblies are accessible
   for removal. If the drive has fixed head modules,
   the FHA PCB assembly is accessible from the right
   hand side of the drive. To remove the matrix PCB
   assembly access to the rear of the drive is
   necessary. This assembly is mounted with four screws.

   Removal of the power amplifier PCB assembly is
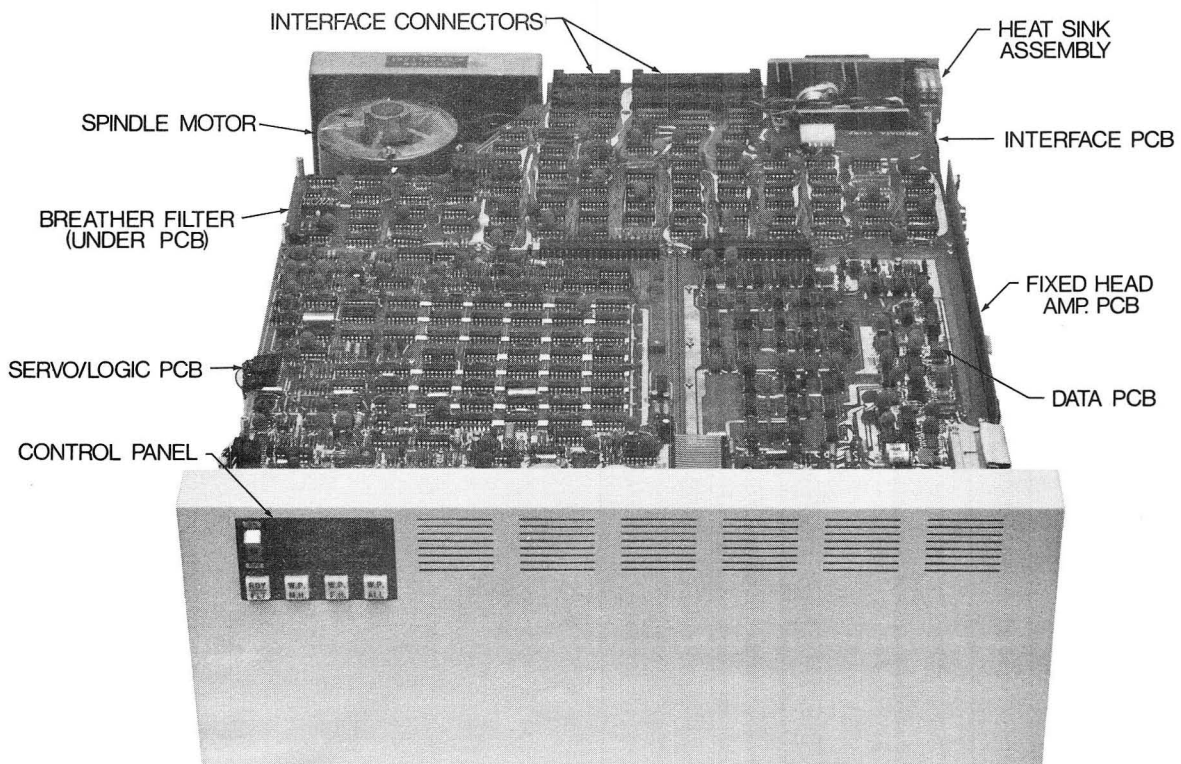   covered in Section 5.4.

Figure 5-9
Printed Circuit Boards

5.6   SERVO ADJUSTMENTS (P/N 30103)

The servo logic board has six adjustment potentio-
meters. They are 1R1, Servo AGC; 1R76, Voltage
Controlled Oscillator (Low Frequency) Limit; 3R132,
Up to Speed; 2R157, Access Time; 4R170, Velocity
Loop Gain; and 4R172, Servo Offset. The location
of these potentiometers can be found on the assembly
drawing in Section 6. 2R157, 4R170, 4R172 require
that one can make seeks between tracks 0 and 339.
One must take off the top cover to access the servo
board (See 5.5.b).

CAUTION

Never attempt to remove 1P16 on the Power Amplifier
board with power on. 1P16 drives the positioner
motor and high peak currents can occur creating an
arc and damage to 1P16, and possibly, the positioner.

5.6.1   R132; Up To Speed

This potentiometer adjusts monostable, 3U40, time-
out, to check that the spindle assembly rotation is
up to speed.

To adjust: turn off drive, put oscilloscope probe
on TP20 and set scope to trigger on positive going
edge. Unplug position motor plug 1P16 from power
amp board. Turn on drive and while unit is coming
up to speed, adjust 3R132 so that TP20 signal stays
high for 20 ms prior to going back low. When the
unit comes up to speed, TP20 will stay high, shut off
unit and allow disc to stop. Turn on power and verify
the TP20 stays high for 23 ms prior to going back low.
Adjustment of UTS is now correct.

5.6.2   1C7, 1R76; Phase Locked Loop

5.6.2.1   1C7 is a factory selected capacitor to set the maxi-
mum frequency of the voltage controlled oscillator
(VCO). 1R76 sets the minimum frequency of the VCO
(U8).

To adjust: Turn off drive. Put oscilloscope on
1U18 pin 4. Unplug 1P16 from power amplifier board.
Use clip on jumper from 1U18 pin 14 to 1TP7. Turn
on drive. After drive is up to speed, one should
see high going pulses (TTL High) on scope. Trigger
on rising edge. The time between rising edges should
be 1.71 μs to 1.78 μs. This represents the highest
VCO frequency. Adjust 1C7 to meet above timing. 1C7
should range from 0 to 10 pf (picofarads). The larger
1C7, the longer the time.

5.6.2.2   When the high limit is set correctly, take the jumper
off of 1U18 p 4 and put it on 1U18 p 7 (and 1TP7).
Trigger on rising edge and adjust potentiometer 1R76
so that rising edges are 2.63μs to 2.78μs apart. Turn-
ing 1R76 ccw increases the time. This is the low
frequency limit.

These adjustments set up the VCO and the phase locked
loop correctly. Turn off drive, remove jumper and
oscilloscope probe. Plug 1P16 back into power
amplifier board.

5.6.3   1R1; Servo AGC

1R1 sets the level of the automatic gain control
(AGC) circuitry, hence, the amplitude of the
demodulated servo signal (SVDM) at 4TP21.

To adjust: Turn off drive. Unplug 1P16 from power
amplifier board. Put oscilloscope probe on 4TP21,
turn on drive. 4TP21 gives a signal that should vary
from +8V to -8V. When drive is up to speed, find the
position motor shipping clamp. See Fig. 5-1. The
clamp will be used to move the head assembly. The arm
should be full ccw, and will travel about 30 degrees
clockwise. Note there is a magnetic detent holding
the arm in its full ccw position. Pull the shipping
clamp, hence, the arm, off the magnetic detent. SVDM
(TP21) will appear as a sine wave as the arm is moved
across the servo tracks. If SVDM does not appear,
calibrate the VCO (see 5.6.2). If still no signal,
or 2-4 volt noise, replace servo board. At the extreme
cw position 4TP21 will go to +9V, this is the guardband.
Move the arm back and forth in the outside region (cw).
4TP21 should be 15Vp-p +1/2V. Now move the clamp (and
arm) back and forth in the inside (ccw) region. 4TP21
should be about 17Vp-p +1/2V. I.e., the average value
of SVDM should be 16Vp-p. Turning 1R1 clockwise in-
creases the signal at 4TP21. This is a critical adjust-
ment and one should check carefully the amplitude at
4TP21 both inside and outside. This completes the AGC
level setting.

Push the shipping clamp full ccw into the magnetic
detent. Turn off drive and remove oscilloscope probe.
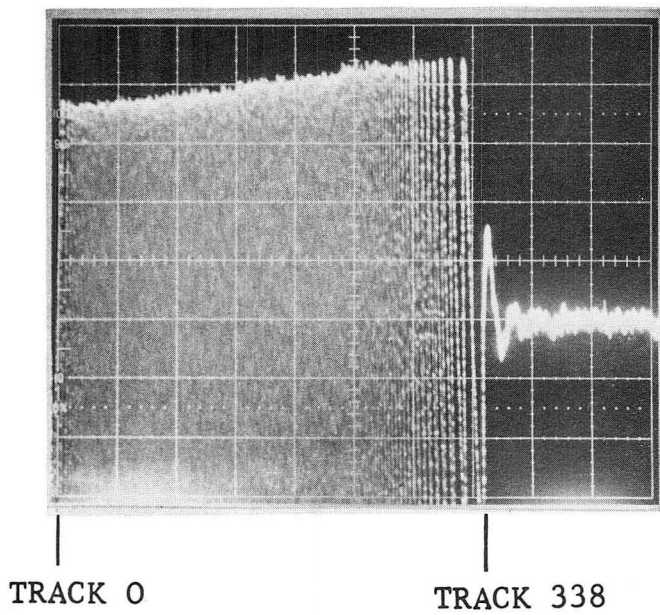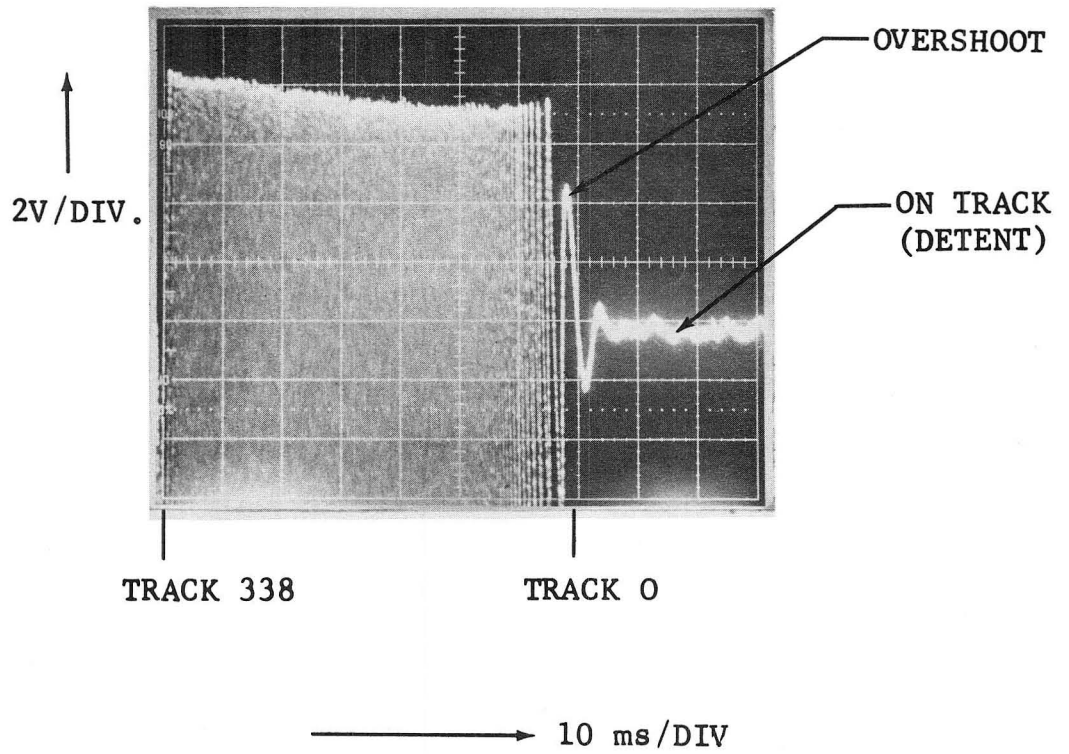Plug 1P16 back into Power Amplifier Board.

2V/DIV.

OVERSHOOT

ON TRACK
(DETENT)

TRACK 338　　　　　　　　　TRACK O

10 ms/DIV

TRACK O　　　　　　　　　TRACK 338

Figure 5-10
SVDM Signal

V-16

The remaining three potentiometers (2R157, 4R170, 4R172) on the servo logic board affect the performance of the drive as it seeks between cylinders. These potentiometers should NOT be touched unless one can make the drive seek between cylinders 0 and 337. If the facilities are not available to seek between cylinders 0 and 337, and if it has been determined that the servo logic board is defective, replace the servo logic board but do not adjust these potentiometers.

5.6.4   4R172 Servo Offset

4R172 adjusts the voltage for which the system strives, in position (detent) mode, refer to 4.3.10.

To adjust: Seek between tracks 0 and 337. Put one oscilloscope probe on 4TP21 and another oscilloscope probe on TP1 on the interface board, Direction Trigger. Trigger on the rising edge of 2TP1 on the Interface board and view 4TP21. One will see, at a sweep rate of 10ms per square, a very fast sine wave for approximately seven squares. (SVDM during a seek), this will be followed by a signal that is near ground with about 1/2 volt of noise (Fig. 5-10). This second portion of the signal is SVDM during detent. Note its DC level. Trigger on the falling edge of 2TP1 (Interface board). Note the DC level of SVDM (4TP21) during detent. Adjust 4R172 so the levels of SVDM during detent are as near to equal and as near to ground as possible when triggered on both the rising and falling edges of 2TP1 on the Interface Board. This optimizes the servo offset potentiometer.

5.6.5   2R157 Access Time and 4R170 Velocity Loop Gain

2R157 supplies a reference voltage to the DAC (U70). This voltage controls the current that the DAC supplies to the main summing junction, controlling the maximum velocity thereby controlling the seek or access time.

4R170 controls the gain of the servo system. If the gain is too low, the servo system will not have enough signal to control the arm and head assembly. If the gain is too high, the system, the arm in particular, will break into oscillation.

2R157 and 4R170 interact as follows: as 2R157 sets faster access times, more acceleration and deceleration are needed to move faster. The gain of the servo system

needs to be higher to control this acceleration and de-
celeration. The optimum is to have fast access times
with no oscillation.

To adjust: Turn on drive; seek between cylinders 0
and 337, after restore. Set up with on oscilloscope
probe on 4TP21 and another on 2TP1 on the Interface
board. Trigger on 2TP1 (Interface Board) on whichever
of the rising or falling edge that shows 4TP21 to be
decreasing in amplitude during the seek (See Fig. 5-10).
There should be a small, less than 8 volt, positive bump
on 4TP21 just before detent occurs. This bump is over-
shoot (Fig. 5-10A). Turn 2R157 clockwise to decrease
access time so the maximum overshoot is 68ms after the
seek starts. If, while turning 2R157 clockwise, the
overshoot exceeds 7V, turn 4R170 clockwise (more gain)
until the overshoot is less than 4V. When maximum over-
shoot occurs 64ms after the seek starts, take the probe
off of 4TP21 and put it on 3U48 pin 6 (SEEK COMPLETE).
The falling edge is the start of seek, the rising edge
is the end of seek. Turn 2R157 clockwise until SEEK
COMPLETE is low for 70^{+2}_{-6}ms. Remove the probe from 3U48
pin 6 and put it back on 4TP21. Turn 4R170 until the
maximum overshoot is 4.2V; make 4TP21 look like Fig. 5-
10A. Reverse the trigger polarity, 4TP21 amplitude
should increase during the seek, see Fig. 5-10B. Maxi-
mum overshoot should be about 2V $\pm$.4V. Take the probe
off 4TP21, put it on 3U48 pin 6. Seek complete should
be low for 75 ms maximum.

This completes the adjustment for 2R157 and 4R170.
Readjust 4R172 if necessary, per (5.6.4).

5.7   WRITE CURRENT

Write current is adjustable on both moving and fixed
heads. There exists one potentiometer, 1R17, on the
matrix board to adjust the write current of all moving
heads and on potentiometer, 3R4, onthe fixed head ampli-
fier (FHA) board to adjust the write current for all
fixed heads. These potentiometers are identical
functionally.

See assembly drawing 30100 and 30104 in Section 6 for
potentiometer and current loop locations.

Equipment required: a 60 MHz current probe, an
oscilloscope and a controller or the means to
write fixed data patterns on to the disc. The
fixed data patterns are 01010101... and either
all 0's or all 1's. Do NOT touch the write
current potentiometers unless all the above
equipment is available.

CAUTION
To adjust write current requires putting
information on the disc. This operation will
write over any data previously written on the
disc. Do not perform the write current
adjustments without making sure that no data
will be overwritten and lost.

5.7.1   To Adjust Moving Head Write Current:

In the upper, right-center of the matrix board
exists a twisted pair forming a current loop.
Engage both wires into the current probe. Write
an 010101... data pattern onto any existing
moving head (select the moving head unit), that
doesn't overwrite important data. (Any track
(sector) on the disc will serve for this
adjustment.) Observe waveform as shown in Fig. 5-11.
If no signal exists check the troubleshooting
guide. If a write protect switch is blocking
this head, namely head 0, do not switch write
protect off, rather find another permissible
track, sector and moving head to perform this
adjustment. Adjust R17 so the flat part of the
signal, after the overshoot, is 76-80mAp-p.
Turning R17 cw increases the write current. Write
all 0's or all 1's, peak to peak current should
not increase or decrease by more than 5mA. This
completes moving head current adjust.

5.7.2   To Adjust Fixed Head Current:

Write an 010101... pattern. Any sector will serve
for this adjustment. Put current probe on both wires
of one of the six current loops at the rear of the
board. Only one loop should have the signal. Try each
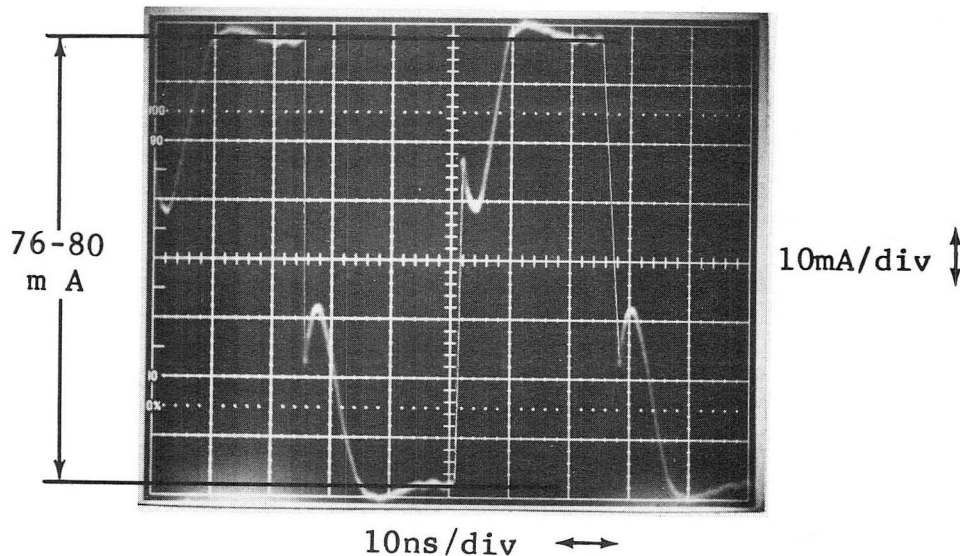loop to find signal. Observe signal as in Fig. 5-11.

76-80
m A

10mA/div

10ns/div

FIGURE 5-11

WRITE CURRENT

If no signal exists on any loop, see trouble-
shooting section. Adjust R4 so the flat section
(after the overshoot) is 76-80mAp-p. Turning R4 cw
increases current. Write all 1's or all 0's, peak
to peak current should not increase or decrease by
more than 5mA. This completes the fixed head
current adjust.

5.8   DATA BOARD

The data board is adjustable only in the data
recovery circuitry. The adjustments are: R34
threshold adjust (Note: adjust may be superseded
by an optional automatic threshold circuit),2 wired-
in taps from DL2, the "erroneous zero crossing"
adjust, 1 wired-in tap from DL3, Delayed Read
Pulse (DLRDP) adjust, and 1 other wired-in tap from
DL3, Delay Corrected Read Pulse (DLCORP).

Equipment required: A Tektronix 465 or equivalent oscilloscope, 2 identical 100MHz oscilloscope probes, 1 other oscilloscope probe, a scope hood, a small soldering iron to change taps, and a potentiometer adjustment tool, a controller, and a "jump" wire.
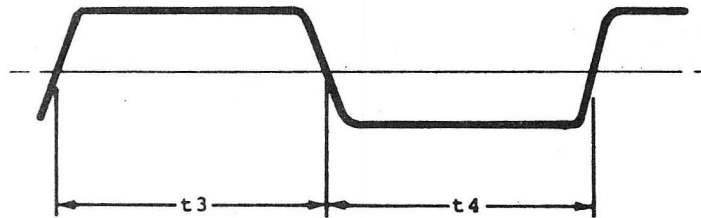
5.8.1 Threshold Adjust

Either 1R34 or 1U10 and 1U11 should be in the board. 1U10 and 1U11 comprise the automatic threshold control. The threshold control sets the level around which the analog read signal moves. This level is just before the clipping amplifiers (1U8) that make the analog read signal into the digital read signal, therefore the threshold level sets the symmetry of the read signal.

To Adjust: Put an oscilloscope probe on 1U12 pin 10, connect jumper from 1U52 pin 10 to 1U52 pin 7. The output levels at 1U12 pin 10 should be -0.9V (ECL High) and -1.8V (ECL low). At full cw on 1R34 the output will be high, and vice versa at full ccw. Near the center of 1R34's travel 1U12 pin 10 should have high frequency oscillation, adjust 1R34 for the maximum amplitude of the oscillation at 1U12 pin 10. Remove jumper from 1U52.

Write an all 1's or 0's pattern, then assert read with the controller. Look at 1U12 pin 10 during a preamble; trigger on read enable (3P11 pin 15 on the Interface board). Set delayed trigger on the rising edge of 1U12 pin 10, with variable sweep set consecutive rising edges on the extremes of the oscilloscope graticule (10 cm apart). The falling edge should be at 5cm ±0.1cm, see Fig. 5-12. Adjust 1R34 if necessary. Adjustment of 1R34 should not require more than 1/8 turn from the setting of 1R34 done in the paragraph above; repeat earlier paragraph above if necessary.

5.8.2 Erroneous Zero Crossing (set taps)

These two taps on 1DL2 form a pulse to clock the read data into a flip flop, to eliminate spurious data from detected due to "snaking" effects. See 4.4.6 for a more detailed explanation of this circuit and its function. The hood will be necessary on the oscilloscope.

Adjust t3 = t4 $\pm$ 2ns.
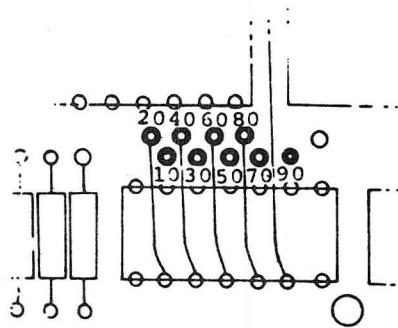
Figure 5-12
Threshold Adjust

Figure 5-13
Erroneous Zero Crossing Taps

To Adjust: 2 taps are necessary. The first tap should
go from "A" to 50 (see Fig. 5-13), the second from "B"
to 60. It does not matter if the first goes to "B" and
the second tap to "A". Put a probe on U12 p 11 and the
other (identical) probe on 1U12 pin 10. One should see
a pulse on pin 11 (10ns wide) that occurs at 55ns with
taps at 50 and 60. This pulse is to be in the middle
of two transitions at the highest read frequency 7.97
megabits/sec (125.5ns is the time between transitions).

5.8.3   DL3, Delayed Read Pulse (DLRDP) (Set Tap)

This tap controls the pulse time of the flip/flop
formed by U32. This pulse is used for the reference
signal for the data phase locked loop. This tap goes
from "C" in Figure 5-14 to a numbered terminal
NOTE: This tap must be connected to some numbered
        terminal for the phase-locked loop to work
        at all. If this tap is missing, the drive
        will neither write nor read.

To Adjust: Put oscilloscope probe on 3U32 pin 14.
Make adjustment with neither read nor write selected.
Move tap to make U32 pin 14 symmetrical (equal pulse
widths high, and low). Moving a tap to a higher
number increases the time 3U32 pin 14 is high (-0.9V).
This completes the adjustment of DLDRP.

5.8.4   Delay Corrected Read Pulse (DLCORP) (Set Tap)

This tap controls the timing of the MFM to NRZ decoder
circuitry. This tap goes from "D" in Figure 5-14 to
a numbered terminal. The hood and all three probes
are necessary for this adjustment.

To Adjust: Use the two identical oscilloscope probes;
put one on 3U48 pin 11, the other on 3U48 pin 10.
Make adjustment with neither read nor write selected.
See Figure 5-15. Move the tap until the rising edge
of the signal on pin 11 is in the middle of the signal
on pin 10's low level period. Higher numbers (see
Fig. 5-14) move pin 11 to the right. DLCORP and DLDRP
may share the same numbered terminal. Adjust the
average time to be as shown in Fig. 5-15. If DLCORP
is not optimized, sporadic read errors will result.
This ends the DLCORP adjustment.
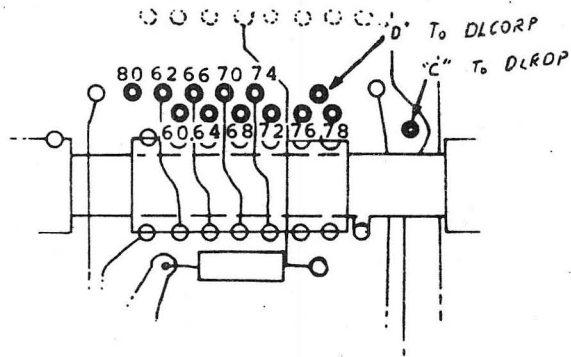
This is the end of Data Board adjustments.

Figure 5-14
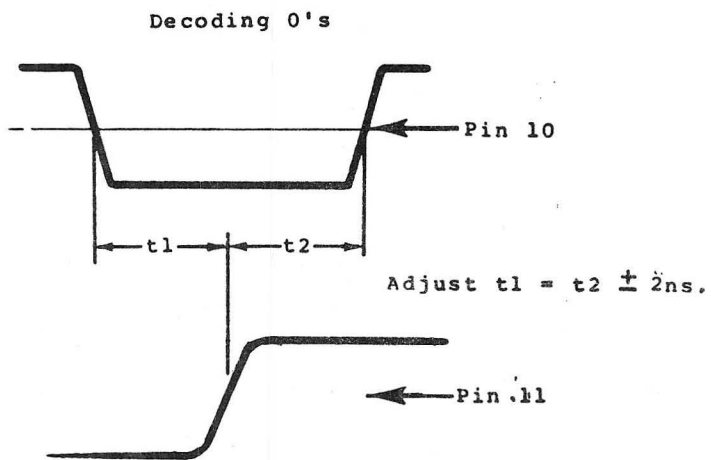Delayed Read Pulse Tap
Delay Corrected Read Pulse Tap

Figure 5-15
Delay Corrected Read Pulse

5.9   INTERFACE BOARD (OPTIONAL) P/N 30115

The interface board has no adjustments. However, it
contains two plug-in headers that affect (1) the unit
number of both the moving and fixed head and (2) the
number of sectors.

5.9.1   Unit Select Logic Plug (2U51)

This plug is used to select the unit number address
of the moving head and fixed head sections of the
drive. The moving head and fixed heads are treated
as separate units. If both units (fixed and moving)
have the same unit address, a fault condition occurs.

The header at 2U51 can be changed, or replaced, so
that moving head and/or fixed head sections of the
drive respond to a new unit address. If there are
thumbwheel switches on the front panel to change
the unit numbers, there is no need to change U51
(see Fig. 5-16). The fixed and moving head unit
addresses are specified via two 4-bit numbers; pin
12 is the 8's pin to select the fixed head unit
number; pin 11 is the 4's pin for fixed heads, etc.
These pins are active low; i.e., unit addresses are
expressed in one's complement form. For example, if
fixed heads are to be unit eleven (8+2+1), then pins
12, 10 and 9 are grounded and a pull up resistor is
connected to pin 11 (Fig. 5-17). If moving heads
are to be unit 4, then pin 15 is grounded, and pins
16, 14 and 13 are connected to pull-ups (Fig. 5-17).
If moving heads are to be unit 0, then pins 16, 15,
14 and 13 are connected to pull-up(s).

5.9.2   The Sector Logic Plug (3U43)

This plug selects the number of 16-bit words per sec-
tor and, therefore, the number of sectors. Reformat-
ting a disc by changing the number of sectors in the
field should be a very rare occurrence. This section
indicates how sector headers are made.

The numbered pins are active high (see Fig. 5-18).
Where the words per sector is specified in normal
form, the following formula is used to determine
the words/sector number:

$$\text{COUNT NO} = \frac{\left(\frac{\#bytes/2}{track}\right) - \left(\frac{index}{overhead}\right) - \left[\left(\frac{number\ of}{sectors}\right) \times \left(\frac{sector}{overhead}\right)\right]}{number\ of\ sectors}$$

#bytes/2 = words (16 bits)

number of sectors = #S (determined by customer)

$\frac{\#bytes}{track}$ = 20160   sector overhead = 2 words

index overhead = 2 words

The overhead parameters result from counters being re-
set and not counting during index and sector times.
Filling in the numbers into the words/sector formula
yields:

$$\frac{\frac{20160}{2} - 2 - \#S(x2)}{\#S} \quad \text{which reduced is} \quad \frac{10078}{\#S} - 2 = \text{count}\ \#$$

In example, if one wants 64 sectors, then

$$\frac{10078}{64} - 2 = 157.46 - 2 = 155.46$$

NOTE: The fraction is always dropped. 155.46 = 155.
The decimal number 155 is represented as:
1 2 8 + 16 + 8 +2 + 1. See Fig. 5-19. Pins 7(1), 8(2),
10(8), 4(16) and 13 (128) are connected to the PLUP
(pull up) pins (6 & 14). All other pins are connected
to the ground pins (3 & 11). The resulting header is
illustrated in Fig. 5-19.

For some sector numbers the connections for plup and
ground must cross, verify that shorts do not exist.
This concludes the sector header section and describes
the changes that can be made to the I/O board.
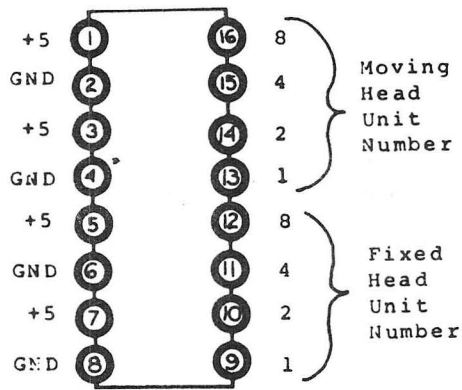
Unit Address Plug
Figure 5-16
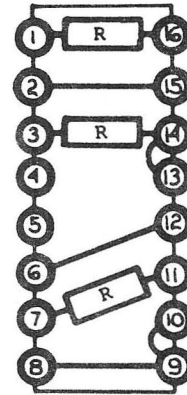
R is 1K Pullup Resistor
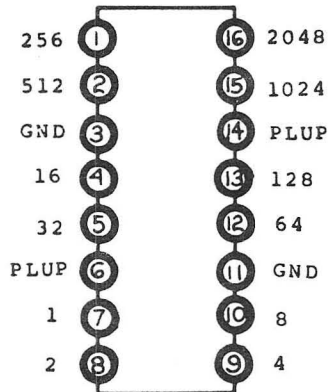
Unit Address Plug Connections
Figure 5-17

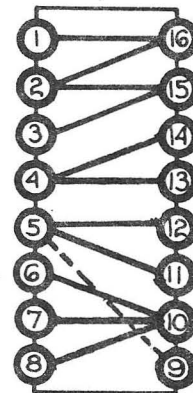Figure 5-18
Sector Plug

6060 bpi

Figure 5-19
Sector Plug (Example)

5.10   CLEAN AIR FILTERS & BLOWER ASSEMBLY

The drive clean air filters comprise a main filter
and a make up air breather filter. Figure 5-1 shows
the location of the main air filter and the blower assy.
The breather filter is mounted on the rear left hand
side of the drive (see Fig. 5-20).

The breather filter has a pre-filter which should be
checked for dirt buildup periodically depending on
the operating environment. A dirty pre-filter should
be replaced, and when the filter element is removed,
the breather element should be inspected for dirt
buildup, and also be replaced if necessary.

5.11   BREATHER FILTER & PRE-FILTER REPLACEMENT

a) Tools required: #2 phillips screwdriver

b) Pull drive forward out of cabinet to
    slide stops. Remove top cover by re-
    moving three screws from each side of
    drive.

NOTE: To replace pre-filter, it is not
       necessary to remove top cover.

c) To replace pre-filter element, remove
    old element and replace with new element.
    This part is removed with fingers and re-
    quires no tools, as shown in Fig. 5-20.
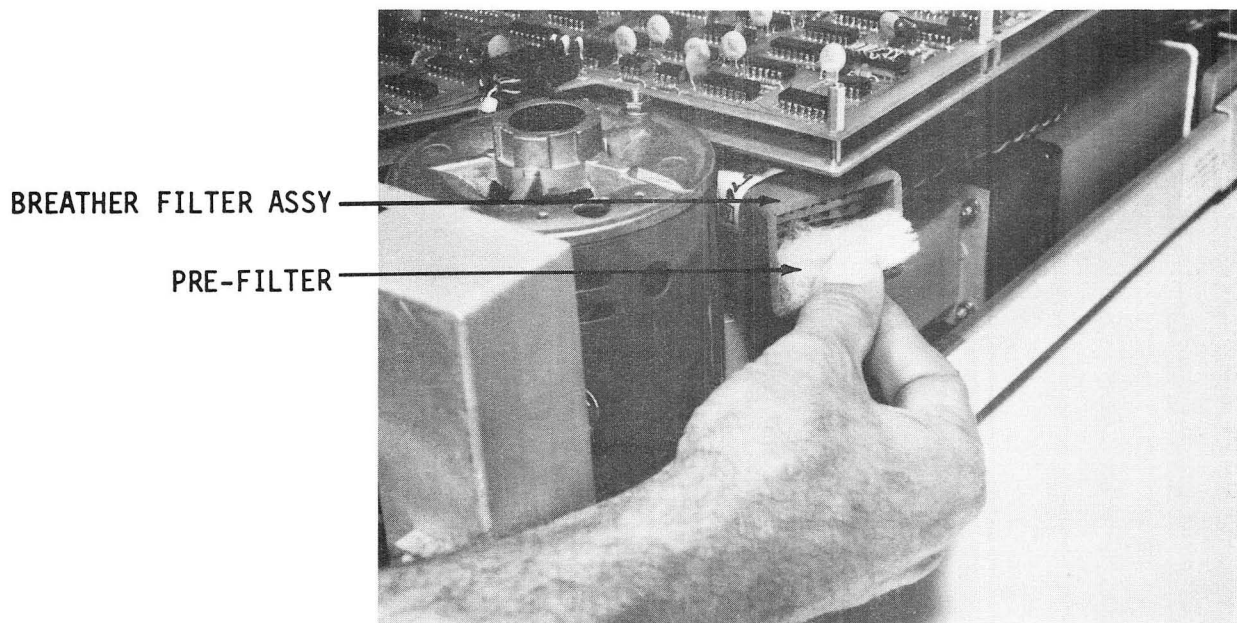

Figure 5-20
Replacing the pre-Filter Breather

d) To replace the breather filter assembly,
    remove the four filter mounting screws,
    remove filter and replace with new filter.

NOTE: The breather filter should not be left
       off the machine for extended periods
       of time. Remove only when replacement
       filter is available.

e) Re-install top cover.

5.12   BLOWER SPINDLE REPLACEMENT

NOTE: The blower spindle should not be replaced
in an extremely dirty environment, an office
cleanliness environment is required.

a) Tools required: #2 phillips screwdriver
                   Bondhus hex driver set
                   RTV 162 silicone rubber
                   hypodermic syringe

b) Remove drive from cabinet and position
   vertically on left hand side of drive as
   shown in Fig. 5-1.

c) Remove spindle and blower drive belts per
   sec. 5.1.6.1.

d) Remove the three blower assy mounting screws
   and the six screws which mounts the blower
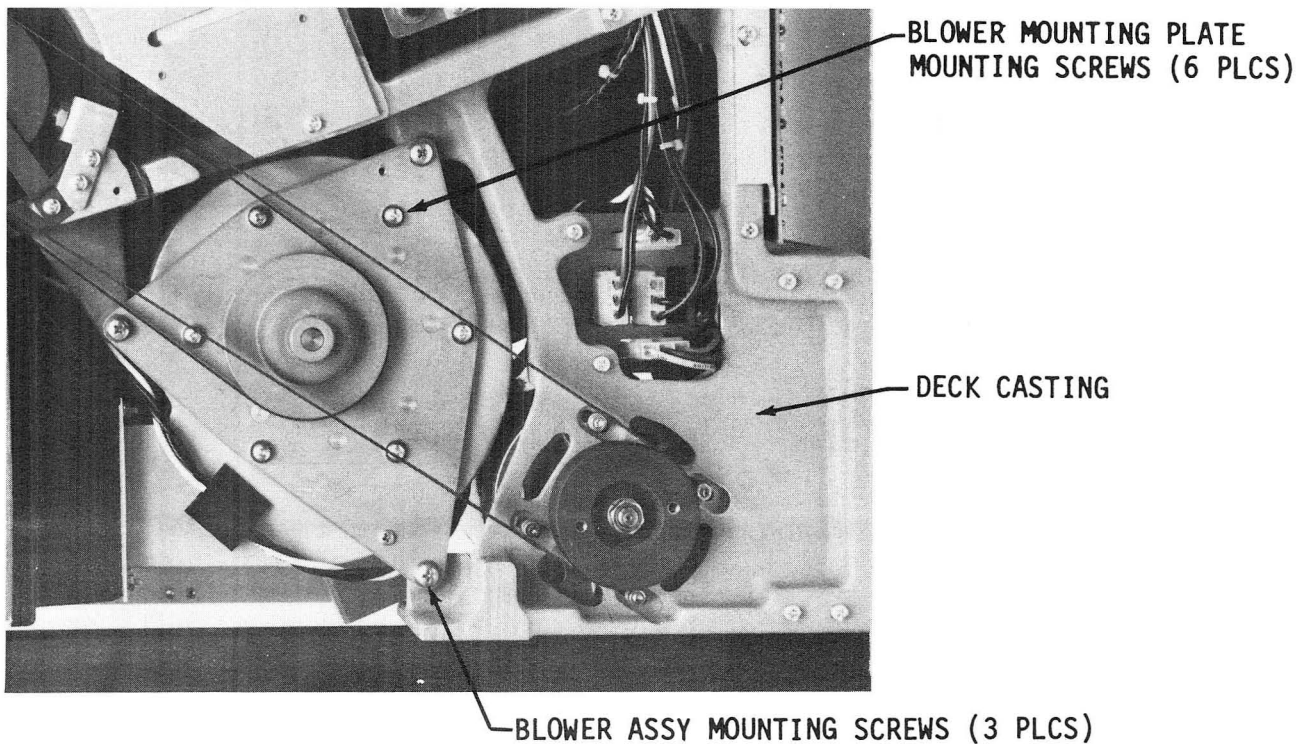   spindle to the blower scroll as shown in
   Fig. 5-21.

Figure 5-21
Blower Assembly

NOTE: The blower mtg plate is sealed with RTV 162
silicone rubber under the six screws and will
require pressure to separate the plate from the
blower scroll. Separation is accomplished by
lifting upward on the plate at the three corners
where the plate attaches to the deck casting. After
separation the plate assembly with the blower
spindle can be removed. The plate after removal
is shown in Fig. 5-22.
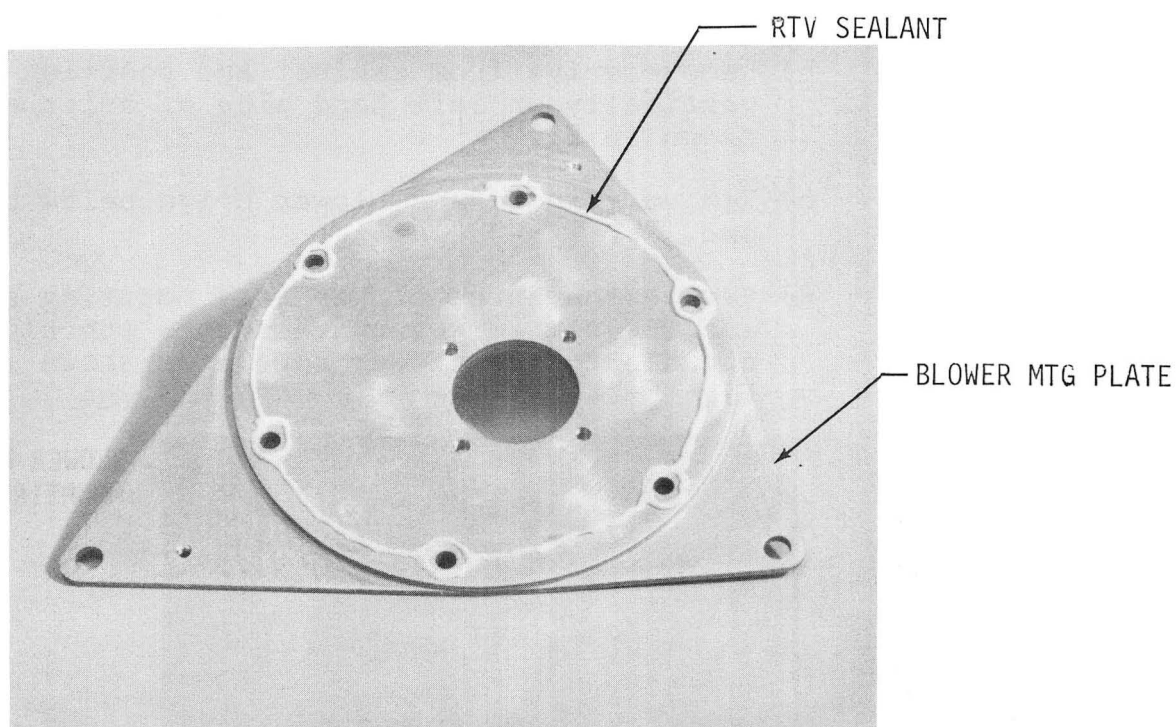
NOTE: SPINDLE OMITTED FOR CLARITY

Figure 5-22
Blower Mounting Plate

e) With assembly removed from the drive, remove
   the blower pulley and the blower wheel with the
   appropriate Bondhus hex drivers. Remove the four
   screws which mounts the blower spindle to the
   mounting plate. The spindle assembly can now be
   removed from the mounting plate.

f) Clean all excess silicone rubber from the blower mounting plate. <u>NOTE</u>: Do not allow loose silicone rubber particles to fall or remain in blower scroll. Apply masking tape over scroll opening to prevent contaminates from entering while replacing blower spindle.

g) Install new blower spindle to plate using the four screws previously removed. Re-install blower wheel and blower pulley and position to dimensions shown in Fig. 5-23.

BLOWER WHEEL HUB TO BF FLUSH WITH SHAFT
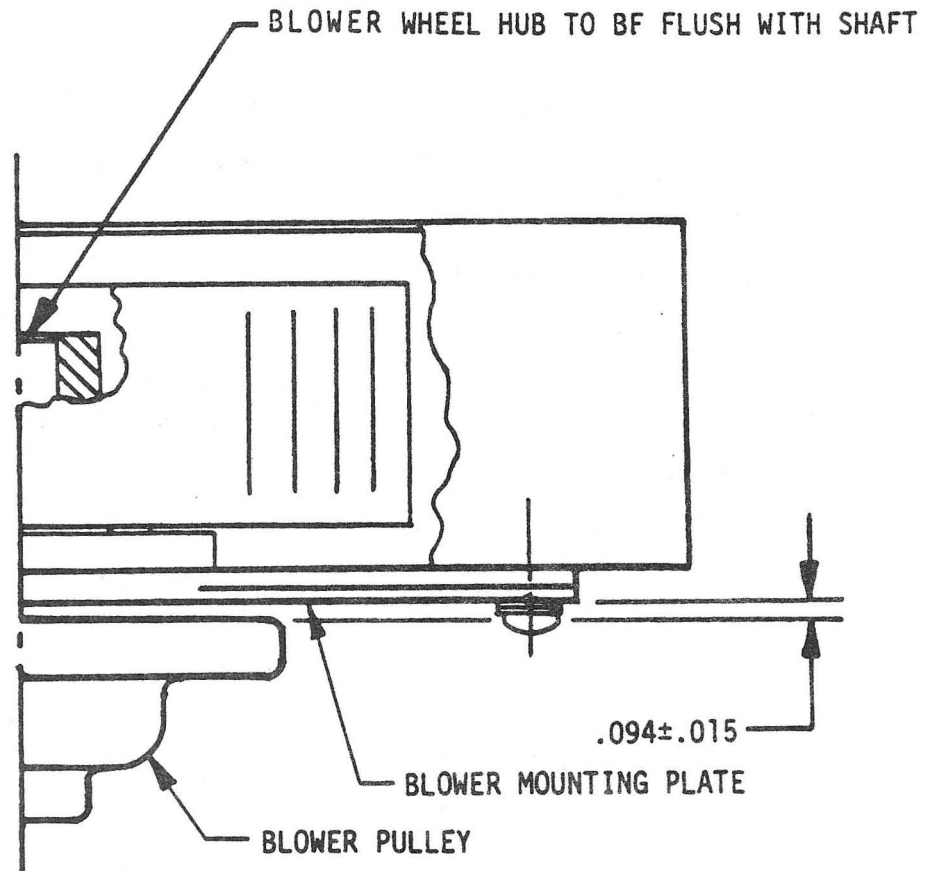
.094±.015

BLOWER MOUNTING PLATE

BLOWER PULLEY

Figure 5-23
Blower Fan and Pulley Spacing

h) Remove masking tape from scroll and apply bead of RTV 162 silicone rubber around the six screw mounting holes and inside perimeter as shown in Fig. 5-22 . Apply silicone rubber using the hypodermic syringe.

i) Install mounting plate assembly to scroll using the six screws initially removed. Re-install the three screws which mount the plate assembly to the drive deck casting.

j) Re-install blower and drive belts.

k) Install drive into cabinet.

5.13 BRAKE ASSEMBLY

To adjust or replace the brake band the drive must be removed from the cabinet and be positioned vertically on the left hand side of the drive as shown in Fig. 5-13.

5.13.1 Brake Band Adjustment

a) Tools required: Two 5/16 open end wrenches

b) With end wrenches loosen nuts on solenoid shaft through opening in power supply mounting plate as shown in Fig. 5-24.

NOTE
Be careful not to rotate solenoid shaft excessively or damage to the metal band will occur.

c) To decrease disc stopping time move hex nut nearest spring in direction which compresses spring. Move other nut down against nut moved and tighten using the two 5/16 open end wrenches.

d) Power up and down and check disc stopping time. Disc stopping time from brake on is not to exceed 6 seconds. Repeat above procedure till above specification is met.
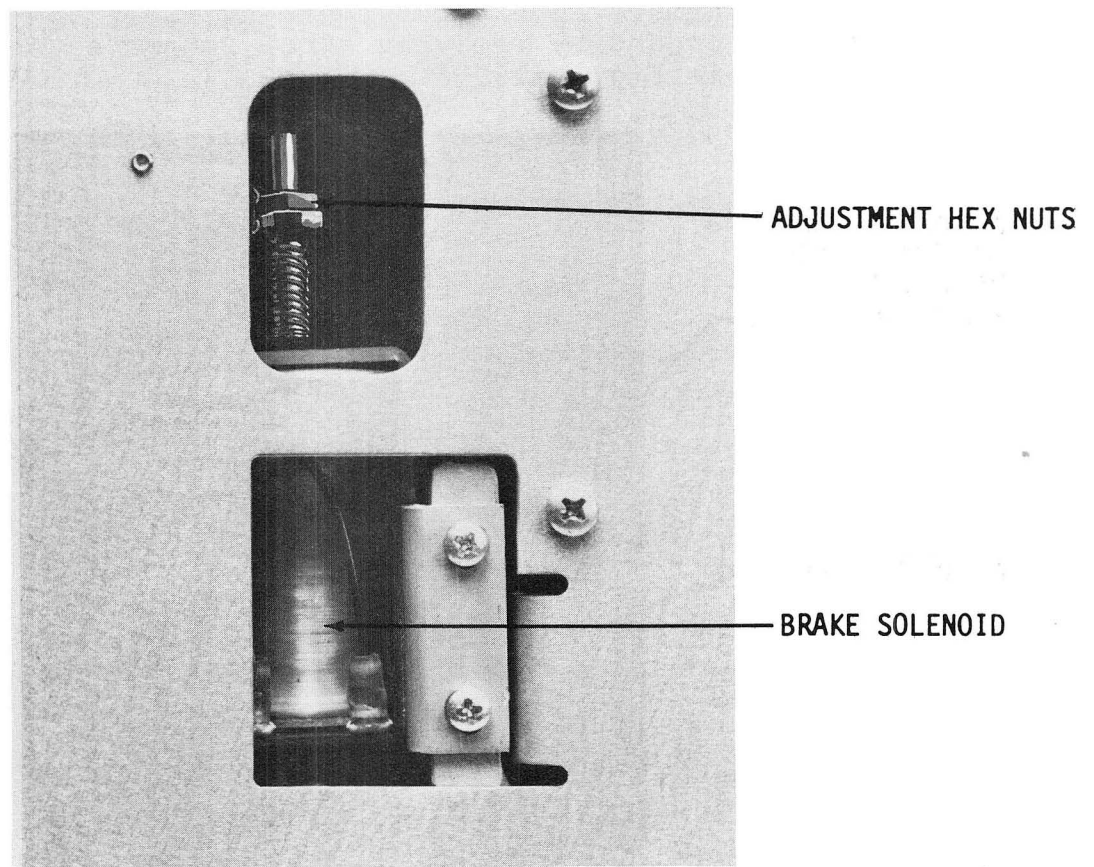
e) Re-install drive in cabinet.

ADJUSTMENT HEX NUTS

BRAKE SOLENOID

Figure 5-24
Brake Adjustment

5.13.2   Brake Band Replacement

   a) Tools required: #1 & #2 phillips screwdrivers
                      1/4 inch spintite
                      3/8 drive hex
                      Socket & ratchet set (Bonney
                        No. B-B0308 or equivalent)
                      Needle nose pliers

   b) Remove power supply assembly per sec 5.3.2.

   c) Remove spindle and blower belts per sec 5.16.

   d) Remove index transducer assembly and spindle
      ground by removing three screws as shown
      in Fig. 5-25.

BRAKE BAND PIVOT.
MOUNTING SCREW,
PIVOT & TOP
& BOTTOM WASHERS

BRAKE SOLENOID
ASSY MOUNTING
SCREWS (2 PLCS)

CHAMFER ON LINK
TO BE ON THIS SIDE

SPINDLE PULLEY

INDEX TRANSDUCER
MOUNTING SCREWS
(2 PLCS)

SPINDLE GROUND SPRING

SPINDLE GROUND
SPRING MOUNTING
SCREW
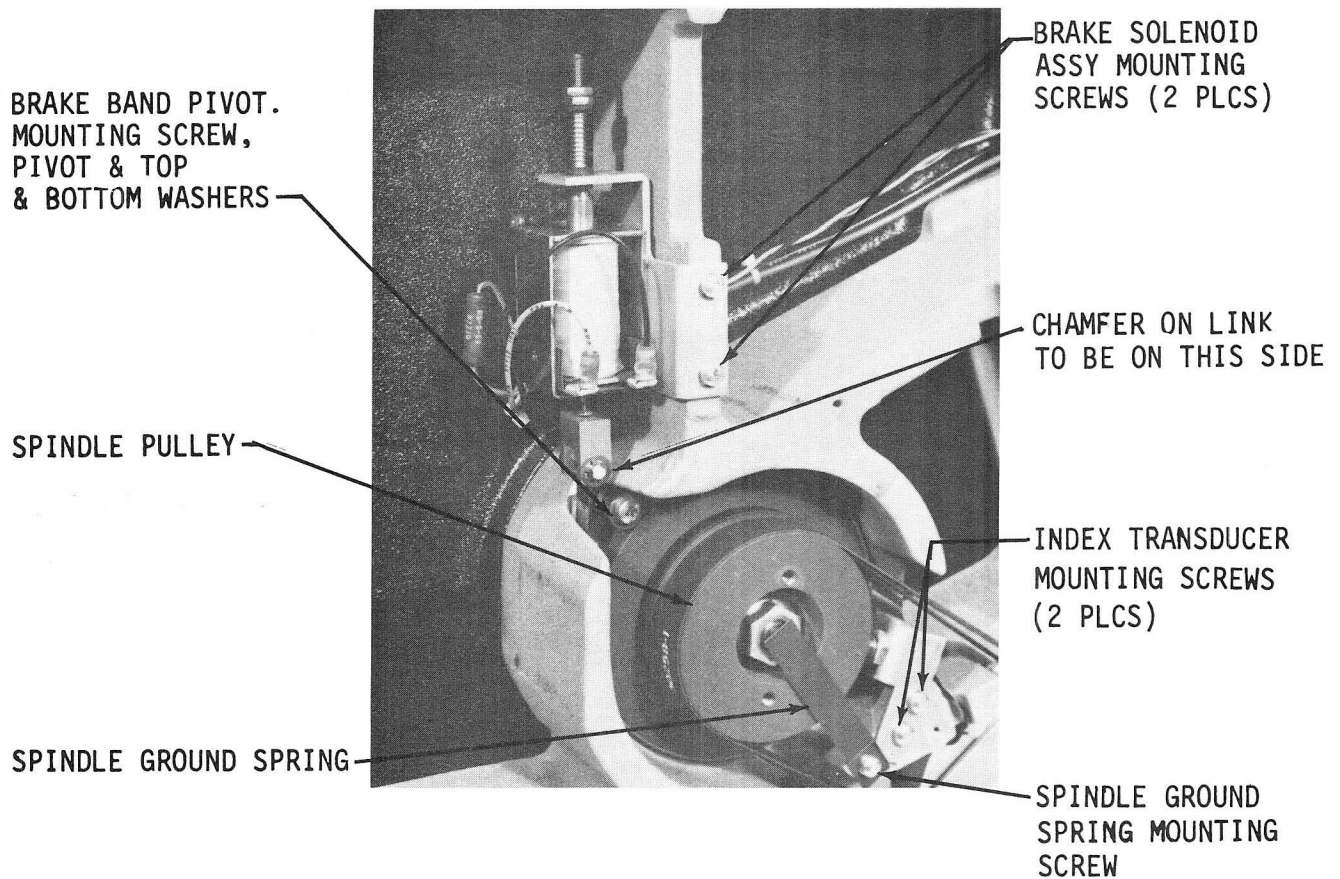
Figure 5-25
Spindle Brake Assembly

e) Remove brake band pivot screw, top and
   bottom pivot washers and brake band
   pivot. See Fig. 5-25.

f) Remove the brake assembly by removing
   the two mounting screws shown in Fig. 5-25.

NOTE

Electrical connections to solenoid and
solenoid switches do not have to be disconnected
unless brake assembly is totally removed
from the drive.

With needle nose pliers remove one retaining
ring from the link shaft and slide shaft out
of link. The brake band is now removed by
sliding the band carefully over the spindle
pulley.

NOTE

Do not allow spindle to rotate counter-
clockwise during this operation.

g) Before installing new brake band check
   situation of solenoid switches. Switches
   should actuate .06 ±.02 from solenoid plunger
   stop when solenoid is moved in forward
   direction (against compressor spring).
   If switches do not operate as outlined
   above, then loosen switch mounting nuts
   and adjust switches till the above
   requirements are met.

h) Place new brake band in link and replace link shaft. Install <u>new</u> retaining ring.

NOTE

Clean deck casting cavity where brake band seats prior to installing brake assembly.

Place brake assembly in drive and mount with the two mounting screws that were previously removed. Set solenoid mounting bracket in center of slotted holes.

NOTE

Make sure chamfer on brake band link is oriented as shown in Fig. 5-25.

i) Install brake band pivot, top and bottom washers and retaining screw.

j) With assembly installed push on end of solenoid shaft and verify that brake band conforms to the machined dia of the deck casting. It is especially important that the brake band conforms to the deck casting at the brake band pivot area.

Solenoid switches should actuate <u>before</u> the brake band seats in the aforementioned machine dia of the deck casting. Re-adjust the solenoid mounting bracket fore or aft till the above requirement is met.

k) Re-install drive belts.

l) Re-install power supply per sec. 5.10.

m) Re-install index transducer and spindle ground spring and adjust transducer gap per sec 5.1.7.

n) Check stop time adjustment per 5.13.1.

0) Install drive into cabinet.

5.14   POSITIONER MOTOR REPLACEMENT

NOTE: This operation should not be attempted in
the field unless it is done by properly trained
personnel.

To replace the positioner motor the drive must
have the shipping stands installed and the drive
orientated as shown in Fig.5-26 . With power off,
remove the positioner power connector (P-16).
Power on the drive and, using the positioner
shipping clamp, rotate positioner ccw to its stop.
Then remove power to drive. This will eliminate
possibility of moving positioner when removing
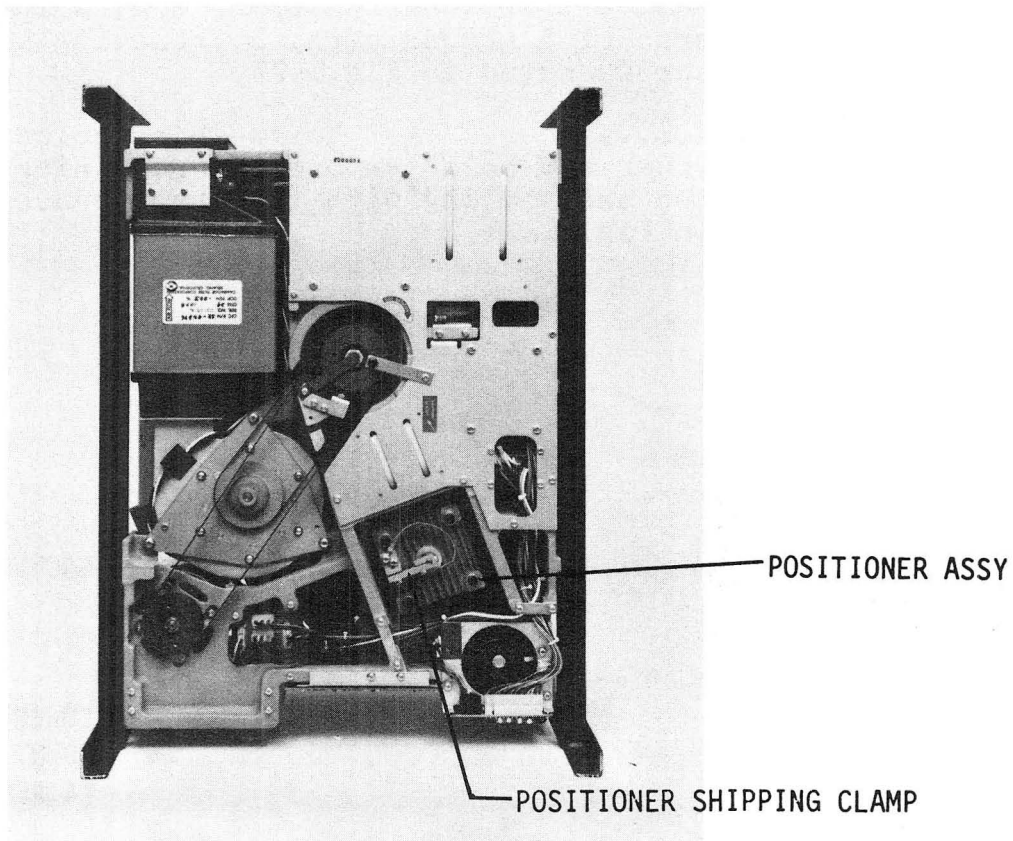motor rotor nut.

Figure 5-26
Positioner Removal (Machine Orientation)

NOTE: DO NOT MOVE POSITIONER SHAFT AT ANY TIME
       DURING POSITIONER MOTOR REPLACEMENT.

5.14.1   Positioner Motor Replacement

a) Tools required: #2 phillips screwdriver
Bondhus hex driver set
No. 2 external retaining ring
    pliers (Milbar or equal)
3/8 drive hex socket ratchet
    set (Bonney No. B-80308 or equal)
Large pliers
2 jaw puller (Williams No. GP-240
    or equal)
Torque wrench (Williams BTW-1RC
    or equal)
271 Loctite retaining compound
Cotton-tipped swabs
100% isopropyl alcohol
Lubriplate grease

b) Remove positioner shipping arm, shipping
bracket & ground strap by removing those
screws noted in Fig.5-27.

c) Remove four 1/4-20 bolts which holds the
lower end bell. Remove the retaining ring from
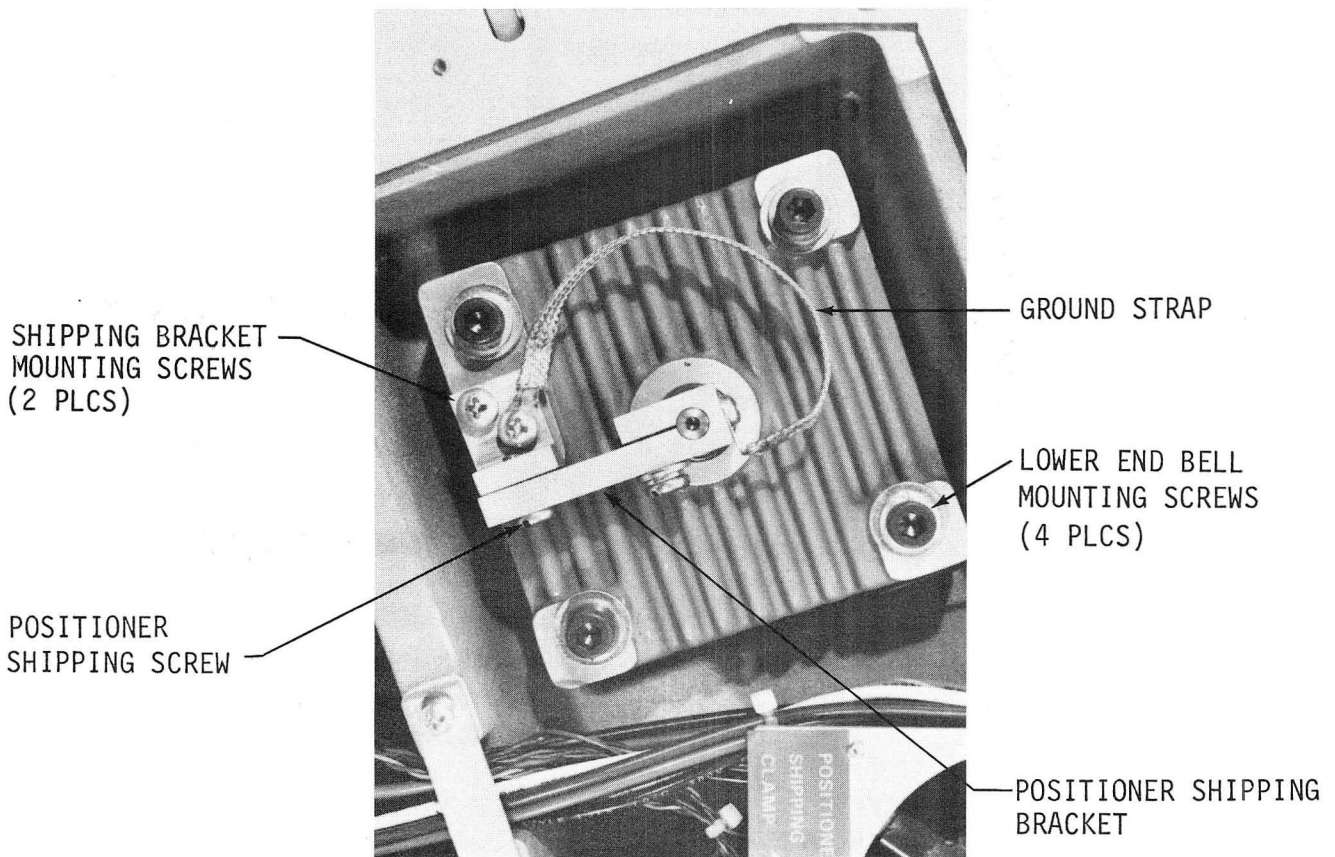the shaft along with the shaft spacers as shown
in Fig. 5-28.

SHIPPING BRACKET
MOUNTING SCREWS
(2 PLCS)

POSITIONER
SHIPPING SCREW

GROUND STRAP

LOWER END BELL
MOUNTING SCREWS
(4 PLCS)

POSITIONER SHIPPING
BRACKET

Figure 5-27
Positioner Motor Assembly

V-39

d) Place puller onto lower end bell as shown in
   Fig. 5-29.
   NOTE: Make sure that puller is centered and
   parallel to positioner shaft. Also, apply
   small amount of lubriplate grease in
   positioner shaft center prior to mounting puller
   to lower end bell so that positioner shaft will
   not rotate.

e) With appropriate socket and ratchet wrench
   jack lower end bell from positioner shaft and
   set aside. A sharp breakaway will occur due to
   the lower bearing locktite giving way. At this
   point note location of marks on positioner
   motor rotor and stator. This orientation must
   be maintained when new positioner motor has
   been installed. Mark these locations on
   visible portion of upper end bell with marking
   pen.

f) Remove 5/16-24 nut which retains the positioner
   motor rotor with appropriate socket and ratchet
   wrench. Remove lock washer and positioner
   motor washer.

   With large pliers grasp positioner motor rotor,
   and remove both positioner rotor and stator
   together from positioner shaft. NOTE: DO NOT
   REMOVE POSITIONER MOTOR ROTOR FROM STATOR!

g) Clean positioner shaft using Kimwipe tissues
   which have been saturated with 100% isopropyl
   alcohol.

   NOTE: DO NOT ROTATE POSITIONER SHAFT AT ANY TIME

h) From lower end bell remove bearing and discard.
   NOTE: DO NOT USE BRG WHICH WAS REMOVED WITH END
   BELL. Make sure that belleville springs do not
   fall out of lwr end bell when removing bearing.
   Belleville springs are to be stacked as shown
   in Fig. 5-30.

i) Install new positioner shaft bearing in end bell.
   Clean bearing I.D. using cotton swab saturated
   with alcohol.

   NOTE: DO NOT ALLOW ALCOHOL TO ENTER SHIELD IN
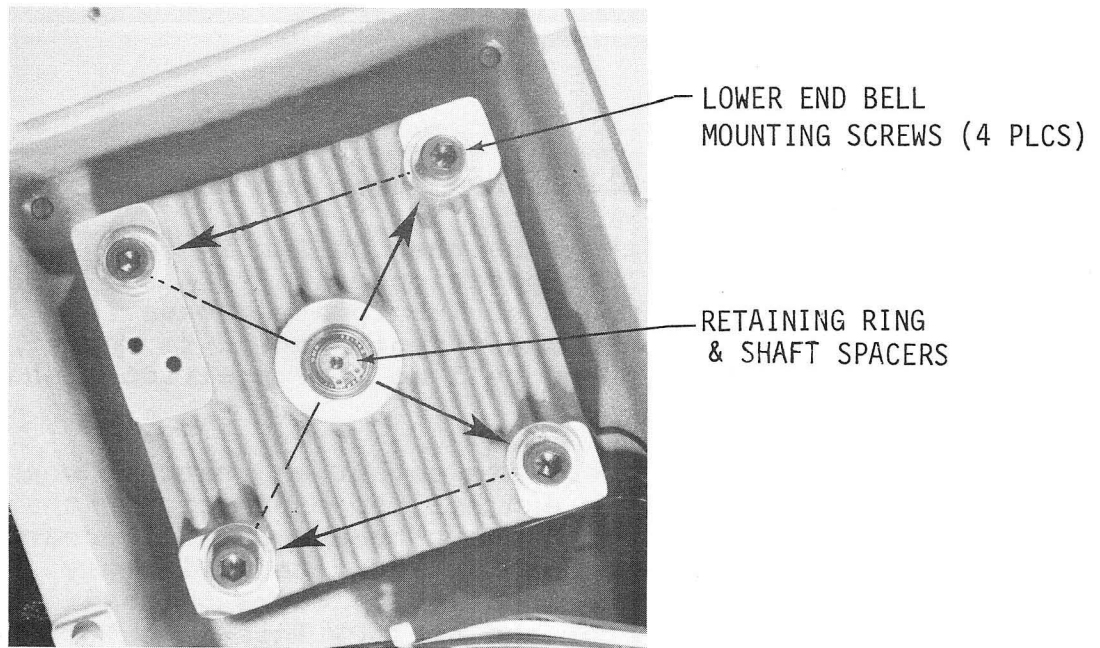   THE BEARING.

LOWER END BELL
MOUNTING SCREWS (4 PLCS)

RETAINING RING
& SHAFT SPACERS

Figure 5-28
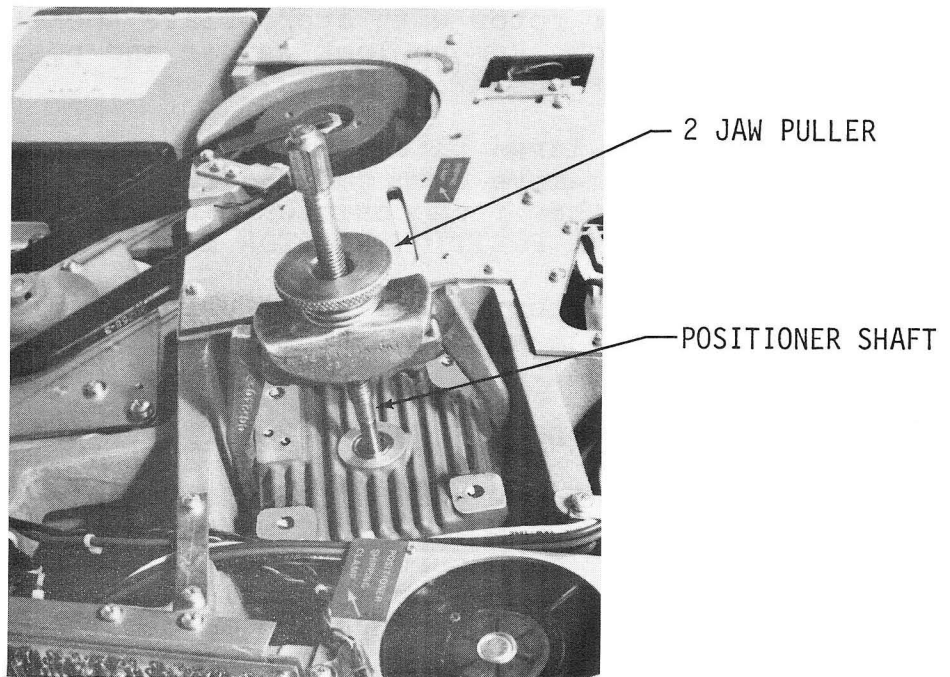Positioner Motor (Retaining Ring)

2 JAW PULLER
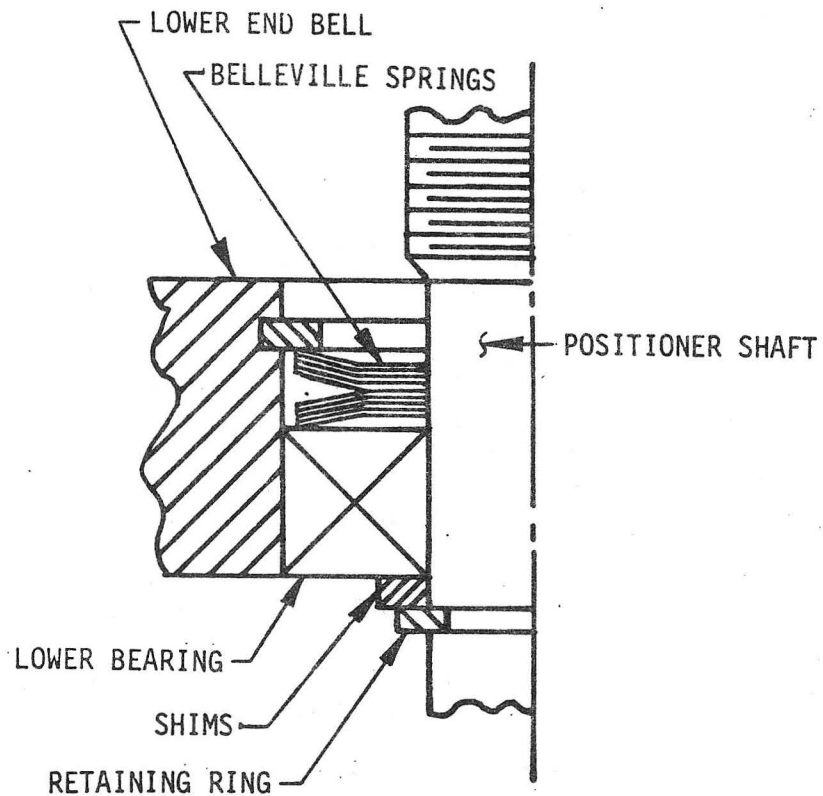
POSITIONER SHAFT

Figure 5-29
Pulling the Lower End Bell

Figure 5-30
Bellville Washer Location

j) Remove remaining locktite compound from positioner shaft by using .062 thich plastic mtrl. Move plastic mtrl in movements parallel to shaft.

Clean positioner shaft with Kimwipe tissues saturated with alcohol.

NOTE
Do not attempt to scrape locktite material from shaft with any metal object or damage will be done to the shaft.

k) Install new positioner motor to positioner shaft making sure that marks on motor rotor and stator line up with the marks made previously during motor removal. NOTE: DO NOT ALLOW MOTOR ROTOR TO EVER BE SEPARATED FROM STATOR! SEPARATION WILL CAUSE DE-MAGNETIZATION OF MOTOR. Orient marks on rotor and stator as noted in 5.4.1(e).

Re-install positioner motor washer, lock washer and nut. Re-orient drive so that it is upside down. When nut is torqued to   ft-lb the shaft will rotate cw until the positioner arm inside the enclosure moves to the magnetic detent position. The shaft should be left in this position for the remainder of this operation. (This is the only time the shaft will rotate.)

l) Install lower end bell to positioner shaft making sure bearing does not come out of end bell during installation.

NOTE: Make sure lower end bell is oriented in proper direction as shown in Fig.5-27.

Install 1/4-20 bolts and progressively tighten in sequence shown in Fig. 5-28.

Torque bolts to 60 lb-in.

m) Add thick (.030) shim washers until retaining ring fails to engage shaft groove while compressing springs under bearing. Remove that shim which prevented retaining ring from engaging shaft groove and replace with thin shim (.010). If retaining ring still fails to engage groove then remove thin shim and snap retaining ring into groove.

n) Remove retaining ring and shims and the four 1/4-20 bolts and remove lower end bell.

o) Clean bearing I.D. and shaft where bearing is located with cotton swab immersed in alcohol. Do not allow alcohol to enter bearing.

p) Apply thin coat of no. 271 Locktite retaining compound to positioner shaft, where bearing mounts, and to I.D. of bearing in lower end bell. Use wooden end of swab to apply compound.

NOTE: DO NOT ALLOW ANY LOCKTITE COMPOUND TO ENTER BEARING!

q) Install lower end bell to positioner shaft making sure bearing does not come out of end bell during installation.

NOTE: Make sure lower end bell is oriented in proper direction as shown in Fig. 5-27.

Install 1/4-20 bolts and progressively tighten in sequence shown in Fig. 5-28.

Torque bolts to 60 lb-in.

r) Re-install bearing shims selected per step (m) and install new retaining ring into shaft groove.

s) Re-install positioner shipping arm, shipping bracket and ground strap previously removed. Set positioner shipping arm .040 from shipping bracket using .040 plastic shim material as shown in Fig. 5-32.
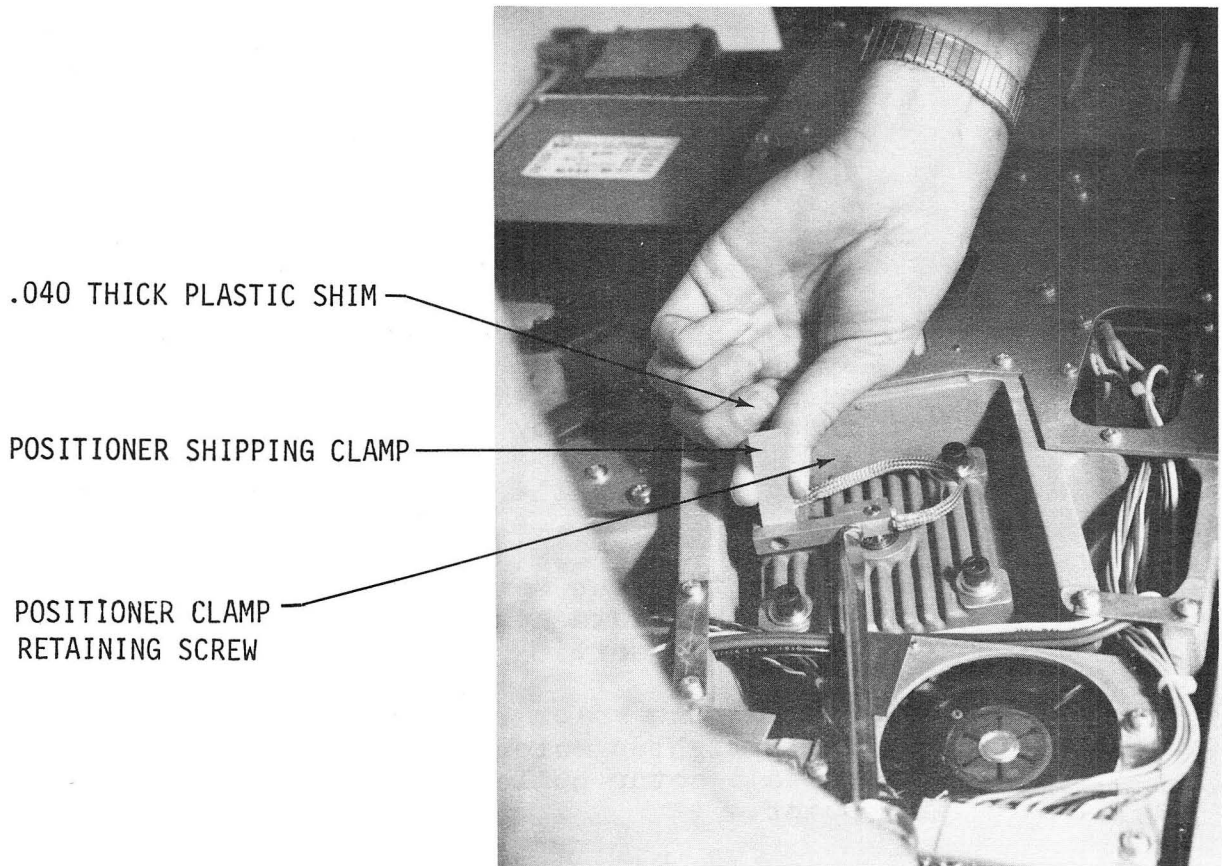

.040 THICK PLASTIC SHIM

POSITIONER SHIPPING CLAMP

POSITIONER CLAMP
RETAINING SCREW

Figure 5-31
Shimming Shipping Clamp Arm

t) With positioner motor connector (P16)
   removed, turn on power and rotate shipping arm
   while checking for freedom of motion. If any
   binding occurs, remove power and re-assemble
   motor.

u) Reconnect positioner motor connector (P-16)
   to the power amplifier assembly.

v) Re-install drive in cabinet.

5.15   SPINDLE DRIVE MOTOR REPLACEMENT

a) Tools required: #2 phillips screwdriver
                   Bondhus hex driver set
                   3/8 drive hex socket wrench set
                      with ratchet (Bonney no.
                      B-80308 or equal)
                   Okidata 30244 pulley spanner wrench
                   Okidata 30282 pulley puller tool
                   Torque wrench (Williams BWT-1RC
                      or equal)

b) Remove drive from cabinet and position
   vertically on left hand side of drive as shown
   in Fig.

c) Remove motor connector (P24) from the connector
   mounting plate as shown in Fig. 5-37.

d) Remove spindle drive belt per 5.16. With
   spanner wrench and appropriate socket remove
   pulley motor nut. NOTE: This is a left-hand
   thread - remove by turning cw.

   Using pulley puller remove pulley from motor
   shaft.

e) Remove the four motor retaining screws using
   the appropriate hex driver from the Bondhus
   hex driver set.

f) Install new motor to drive deck casting. Do not
   fully tighten motor mounting screws at this time.
   Install motor pulley but not the nut at this
   point.

g) Re-install drive belt and adjust motor position per sec. 5.16. CAUTION: Observe rotation direction as noted by label on drive when installing drive belt.

h) Tighten pulley nut to   in.lbs.

i) Re-connect motor connector (P24) to connector mounting plate.

j) Install drive in cabinet.

5.16   DRIVE BELT TENSION ADJUSTMENTS

The spindle drive belt tension should be maintained between 22 and 29 lbs. High belt tension will result in early motor bearing failures and also reduce spindle operating life. Low belt tension will cause excessive belt slippage during drive start and stopping.

The blower drive belt is a semi-elastic type and does not require tension adjustments. NOTE: Never stretch blower drive belt more than necessary for installation or permanent deformation will occur.

Belt tension adjustments are to be made per the following procedure:

a) Tools required: Bondhus hex driver set
                   #2 phillips screwdriver
                   18" steel scale (10ths & 100ths
                      grade)
                   Spring scale (Chatillon DPP-5
                      or equal)
                   6" steel scale (10ths & 100ths
                      grade)

b) Remove drive from cabinet and position vertically on left hand side of drive as shown in Fig. 5-1.

c) Check belt tension by deflecting belt to .50 inches halfway between motor and spindle pulleys as shown in Fig. 5-32. With spring scale measure force at belt deflection noted above. This force should be 4 ±1/2 lbs.
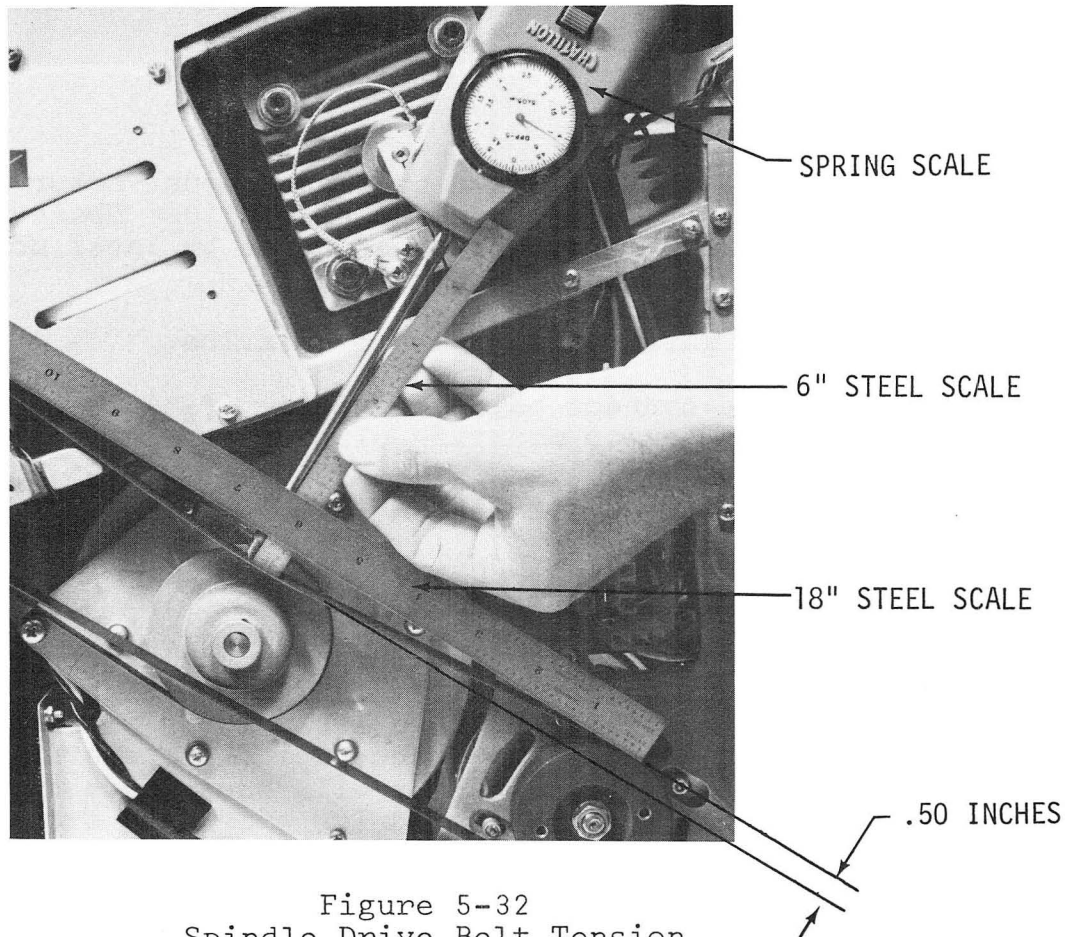
Figure 5-32
Spindle Drive Belt Tension

NOTE

On 50Hz units the motor mounting screws may
not be accessible with the pulley installed.
On these units perform adjustment steps by
loosening pulley and pulling pulley 1/8"
forward. This will make the mounting screws
accessible. Pulley nut is left thread.

If measured force is not correct, loosen
drive motor mounting screws and shift motor
to increase or decrease belt tension. Repeat
this procedure until the correct tension
is obtained. NOTE: It may be useful to remove
the spindle drive belt to adjust motor
location. This is accomplished in (d) below.

d) Remove spindle drive belt by pushing solenoid
plunger shaft (through opening in power supply
mounting plate - see Fig. 5-24) and with upward
force on belt rotate spindle in direction until
belt is released. NOTE: DO NOT ROTATE CCW OR
SERIOUS DAMAGE TO HEADS WILL RESULT.

e) Re-install belt and check tension as defined in (c) above.

f) When proper belt tension is achieved, re-install drive in cabinet.

5.17   INDEX TRANSDUCER & SPINDLE GROUND SPRING

   I.   INDEX TRANSDUCER ADJUSTMENT

   a) Tools required: #2 phillips screwdriver
                        .020 thick plastic shim

   b) Loosen index transducer mounting screws and insert plastic shim between blower pulley and transducer. Move mounting bracket in against shim and tighten mounting screws. Pull shim out. Index transducer is now set at proper spacing.

   II.   SPINDLE GROUND SPRING

The spindle ground spring contacts a silver/graphite button which is located in the end of the spindle shaft.

Replacement of the spindle ground spring is accomplished by removing the mounting screw. The spindle ground button in the spindle shaft is now accessible for replacement if necessary.

Add new button and/or ground spring and re-install mounting screw. Make sure ground spring is centered on button before tightening screw.

5.18   COOLING FAN ASSEMBLY

The cooling fan is located where shown in Fig. 5-33. Under normal conditions, the cooling fan need not be replaced over the life span of the drive.

If replacement is necessary, then the following procedure is to be followed:

a) Tools required: #2 phillips screwdriver

b) Remove drive from cabinet and position
vertically on left hand side of drive as
shown in Fig.

c) Remove connectors from power amplifier
assembly and two lower screws holding power
amplifier PCB assembly to fan mounting bracket.

Disconnect fan connector (P25) from A/C
distribution connector plate.

Remove cable clamps and fan mounting bracket
screws.

NOTE: Three screws mount the fan assembly to
the base casting, two of which also mount cable
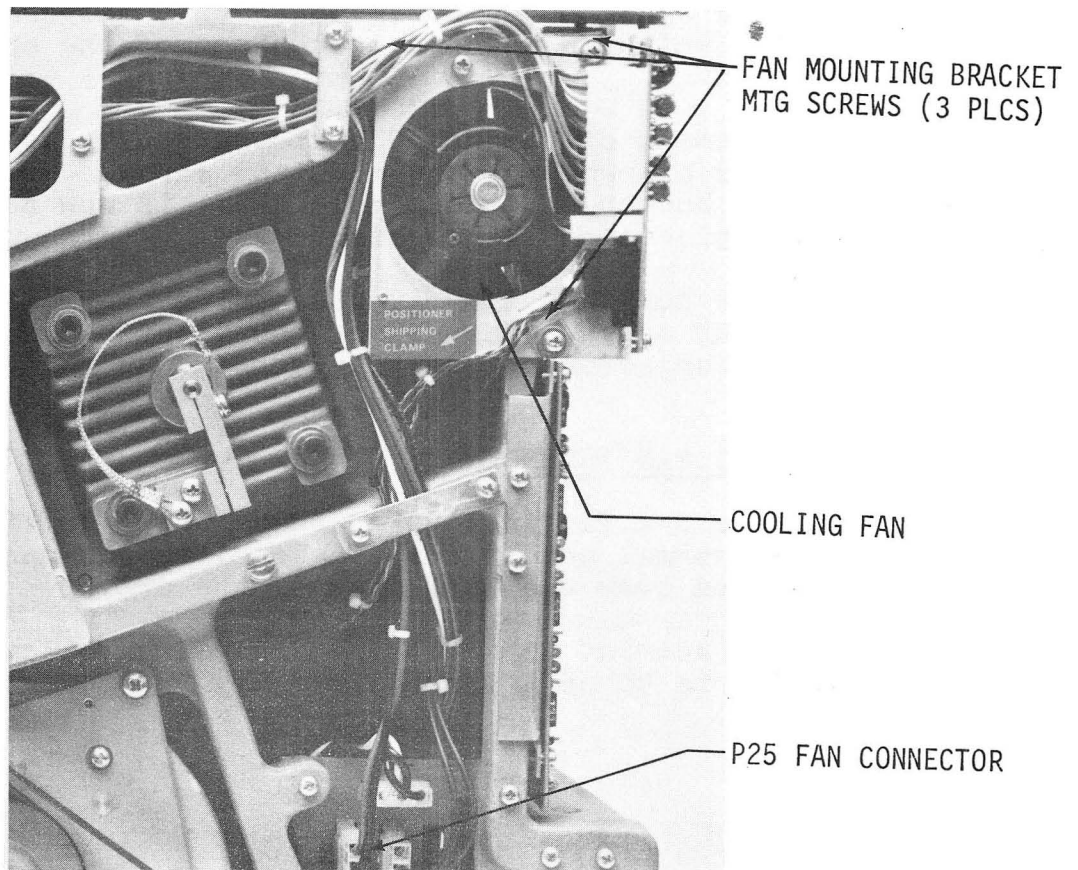clamps as shown in Fig. 5-33.

FAN MOUNTING BRACKET
MTG SCREWS (3 PLCS)

COOLING FAN

P25 FAN CONNECTOR

Figure 5-33
Cooling Fan Assembly

d) Remove defective fan assembly and replace
   with new assembly. Follow reverse procedure
   for installation of fan assembly.

e) Install drive in cabinet.

5.19   A/C DISTRIBUTION ASSY

The A/C distribution assembly is located where
shown in Fig. 5-34. The internal harness assembly
has a service loop which allows the A/C assembly
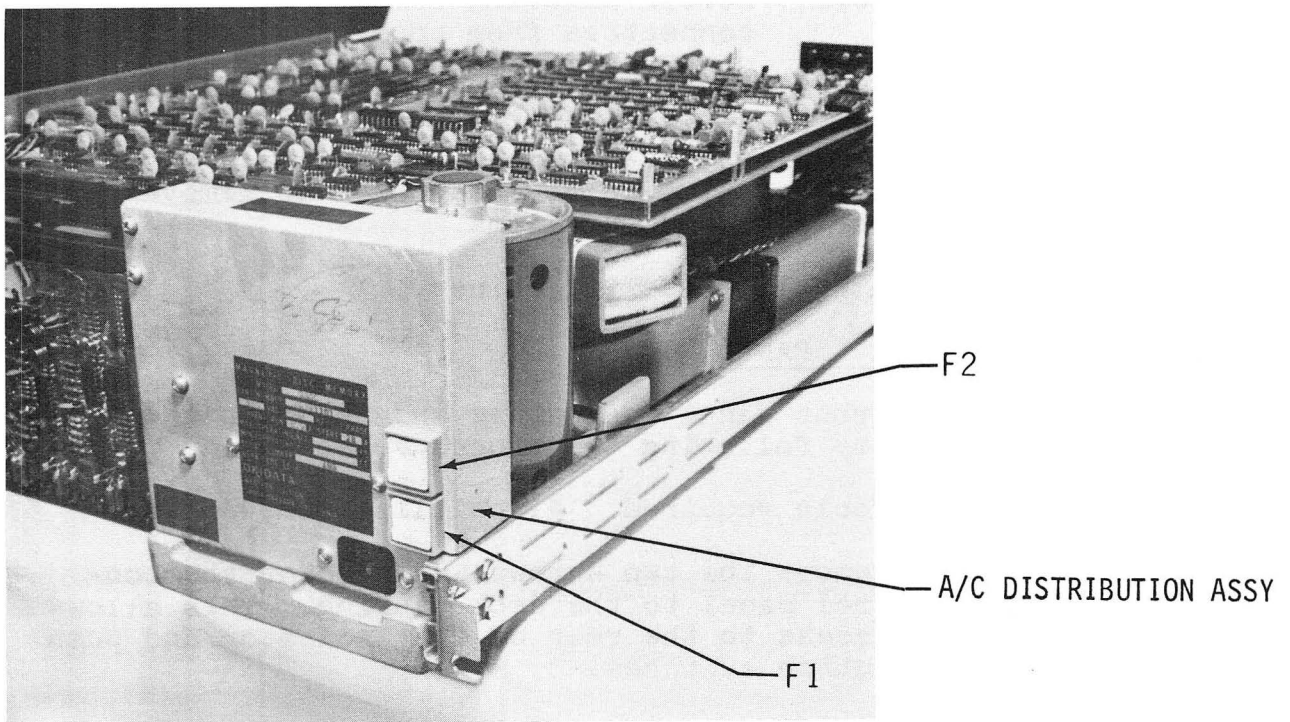to fold down and away from the drive for servicing.

Figure 5-34
AC Distribution Assembly

5.19.1   Removal of A/C Distribution Assembly

a) Tools required: #2 phillips screwdriver

b) Remove drive from cabinet and place drive
    on bench or table with rear of drive over-
    hanging bench as shown in Fig. 5-35. This
    allows access to the mounting screws on
    the lower surface of the drive.

c) Remove the four screws which mount the A/C
    distribution assembly to the drive deck
    casting. The A/C distribution assembly can
    now be folded down and away from the drive
    for servicing as shown in Fig. 5-36.

d) Removal of the three screws which mount the
    A/C connector plate (see Fig. 5-37) will
    allow the entire A/C distribution assembly
   to be removed from the drive.

    NOTE: Before removing screws, disconnect
           connectors from connector mounting
           plate, and P27 (Fig. 5-3).

e) After servicing, re-install connector mount-
    ing plate (if removed) and A/C assembly to
    deck casting in reverse order as removed as
    per preceding sections.

f) Install drive in cabinet.

5.20   CONTROL PANEL

The front panel indicators and switches are replace-
able by following the procedure below:

a) Tools required: #1 phillips screwdriver

b) Remove the two screws which mount the con-
    trol panel to the deck casting. This allows
    access to the rear of the indicator and push
    button switches.

c) Push on rear of defective unit until it snaps
    out of mounting bracket as shown in Fig. 5-38.

d) Disconnect terminals from assembly and replace
    with new unit. Snap new assembly into bracket
    hole and replace switch panel mounting bracket
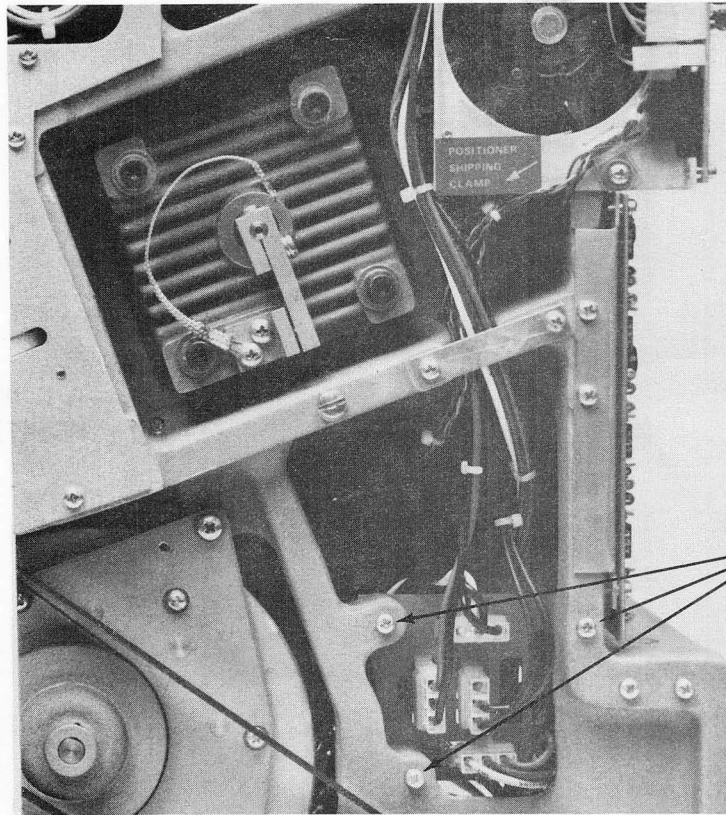   to deck casting.
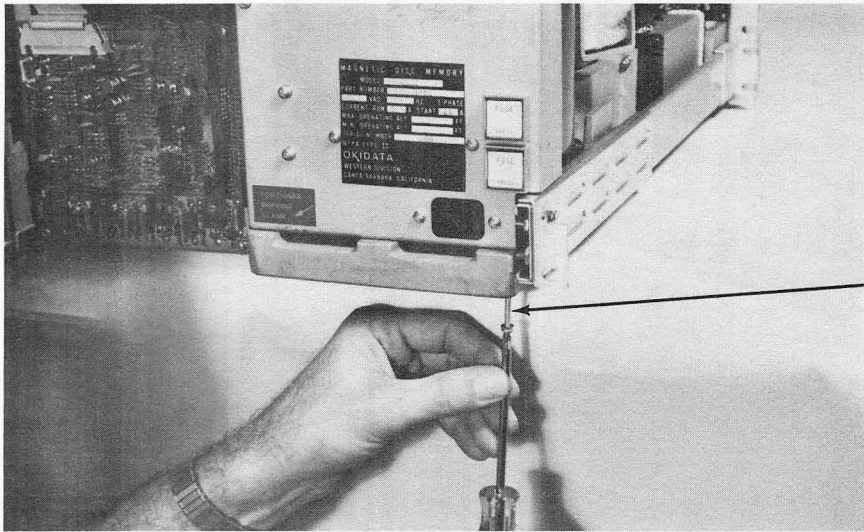
A/C ASSY
MOUNTING SCREW (4 PLCS)

Figure 5-35
Removing the AC Distribution Assembly

A/C CONNECTOR MOUNTING PLATE
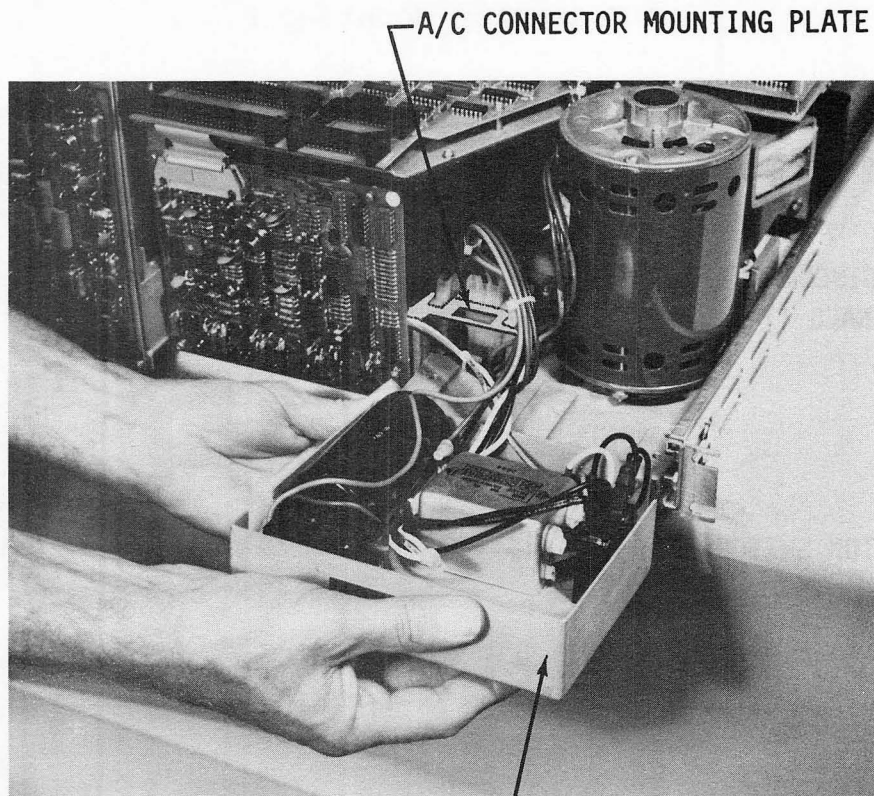
A/C DISTRIBUTION ASSY

Figure 5-36
AC Distribution Assembly in Repair Position

A/C CONNECTOR MOUNTING PLATE SCREWS (3 PLCS)

Figure 5-37
AC Connector Mounting Plate

SWITCH PANEL ASSY

QUICK DISCONNECT TERMINALS (TYP)
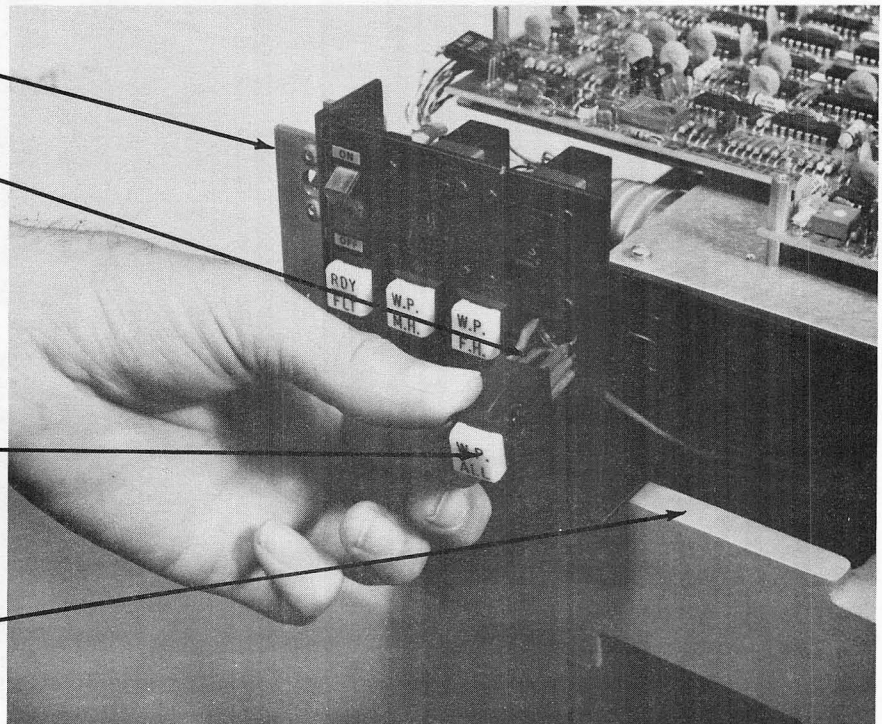
PUSH BUTTON SWITCH

DECK CASTING

Figure 5-38
Replacing Defective Switch

5.20.1   Replacing Switch/Indicator Lamp

    a)   Remove lens cap by grasping both sides of
        cap and pulling forward.

    b)   Push a piece of 3/16 shrink tubing (PVC-105
        preferred) over the lamp and pull.

    c)   Replace lamp by pushing into place, then
        replace lens cap.

5.21   TROUBLESHOOTING

Troubleshooting of the Okidata 3300 Disc Drive Units
requires a thorough knowledge of the contents of
Section 4. Before performing any detailed trouble-
shooting, the preliminary checks contained in the
following paragraph should be performed. If the
problem is not corrected by performing the prelim-
inary checks, refer to the paragraphs on system
level troubleshooting and to the troubleshooting
charts. Note that the troubleshooting procedures
do not include checking individual components such
as I. C.'s, capacitors, resistors, etc. Checking
of such components is to be done by conventional
voltage and resistance tests, with the aid of the
schematic and assembly diagrams in Section 6.

5.22   PRELIMINARY CHECKS

Preliminary checks are performed to ascertain that
the equipment is connected properly and that the
proper operating voltages are present.

    a)   Verify that all cables and connectors are
        in good condition and that connections
        are made correctly.

    b)   Verify that the two A/C fuses on the A/C
        distribution assembly (P/N 30337) and four
        DC fuses on the power amp assembly (P/N
        30105) are not burned out, and that they
        are of the specified rating.

    c)   Inspect for evidence of broken wires, and
        overheated components.

An initial check should always include the power
supply circuits. Specifically, $+32V$, $+5V$ & $-2V$
should be checked at P21 on the power amp assembly
to ensure correct output voltage. Also, eliminate

the possibility of external equipment causing the malfunction. If the malfunction is a control function or if all heads are affected, ensure that all inputs to the disc drive are correct.

5.23   <u>TROUBLESHOOTING CHARTS</u>

The system troubleshooting charts are provided to aid the maintenance technician in isolating malfunctions in the disc drive. The troubleshooting charts provide typical symptoms of malfunctions along with probable causes, possible remedies and references to procedures within the manual which may aid the maintenance technician in isolating a fault. These tables should be used in conjunction with the assembly and schematic diagrams in Chapter 6.

TROUBLESHOOTING GUIDE

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE
Spindle motor does not start or does not come up to speed (cont.)	AC fuse F2 blown	See section "AC Fuse , F2, Blows" (below)	
	+32V Power supply failure	Check J15 pin 3 for $+32V \pm 5V$; repair or replace power supply assembly	5.3.1
	Connectors loose	Push in plugs P17, P22, P24, P25, P26, & P27 until seated	Fig.5-38 & Fig. 5-3
	Brake band maladjusted	Adjust or replace brake band	5.13.1
	Defective spindle motor	Replace spindle motor	5.15
AC fuse, F1, blows	Wrong fuse installed	Install correct fuse as labelled	Fig. 5-35
	Stuck spindle motor or shorted spindle motor	Remove drive belt if motor does not turn freely, replace spindle motor	5.16d, 5.15
	Short in AC distribution assembly	Repair or replace AC distribution assembly	5.19
	Unit plugged into wrong (AC) voltage	Check for proper line voltage	
AC fuse, F2, blows	Wrong fuse installed	Install correct fuse as labelled	Fig. 5-35
	Power supply voltage taps incorrect -OR-	Match tap configuration to line voltage	5.3
	Unit plugged into wrong (AC) voltage	Check for proper line voltage	

TROUBLESHOOTING GUIDE

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE
AC fuse, F2, blows (cont.)	Shorted power supply	Repair or replace power supply assembly	5.3.1
	Shorted fan	Replace fan	5.18
Ready light does not turn on 30 seconds after power on	Position motor shipping clamp screw not removed	Remove shipping clamp screw	Fig. 5-1
	Burnt out ready light	Check for continuity, if open replace light	5.20
	Power amplifier thermal switch S1	Connect cables to switch. Check for continuity;if open, replace switch.	5.4.1
	Proper voltages on all boards	Check and seat power connectors P1, P3, P5, P8, P10, P18, P20, P21.	Section 6
		Check DC fuses F1, F2, F3, F4 and replace if necessary	Fig. 5-5
		Check DC voltages on J21 on Power Amp Pin 1 −2V ±.1V Pin 3 −5.2V ±.05V spc Pin 9 +5V ±.05V adjust Pin 11 −32V ±5V Pin 13 +32V ±5V	5.4 5.3.1
	Signals not applied to servo bd	Check orientation and seat connectors P4, P9, P13; P19 enclosure; P14 power amp	Section 6

TROUBLESHOOTING GUIDE

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE
Ready light does not turn on 30 seconds after power on (cont.)	Ready line stays low	Check P12 pin 29 on I/O bd.; if TTL low adjust or replace servo bd. (P/N 30103), otherwise adjust or replace I/O bd. (P/N 30115)	5.6
	Relay, K1, defective on P/N 30105	Check pins 1 & 4 for continuity, if open, replace relay	
	Defective servo bd.	Adjust or replace servo bd. (P/N 30103)	5.6
	Defective power amp assy.	Replace power amp assy.(P/N 30332)	5.4.3
	Defective I/O bd.	Replace I/O bd. (P/N 30115)	
Ready Light flashes	Uncleared fault condition	Momentarily switch off AC power, ready light should turn on within 30 seconds. If ready light again begins to flash, see below	
	Continuous write fault	Check 1U5 pin 9 on matrix bd.; if TTL low, replace matrix bd. (P/N 30 440)	4.4.2
		Check 1U8 pin 1 on optional fixed head amplifier bd.; if TTL low, replace fixed head amplifier bd. (P/N 30104)	4.4.3
		If no FHA on drive, check if FLT2 jumper on I/O bd. is in-stalled; install if necessary	4.5
		If 1U5 pin 9 on matrix bd., 1U8 pin 1 on FHA are TTL hi and correct "FLT" jumper are installed, replace I/O bd. (P/N 30115)	

TROUBLESHOOTING GUIDE

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE
Ready Light flashes (cont.)	Optional thumbwheel switches set at same number (unit address)	Set thumbwheel switches to different numbers, as required	5.9.1
	Write protect fault	Check that optional write protect switches have not been accidentally engaged	4.5
	Invalid interface commands from disc controller	Check connectors P31, P32, P33, P34 or terminator card for proper installation, check interface cables for damage	
	DC power fault	See "proper voltages on all boards", pg. V-58. Check U32 pin 3 on servo bd.; if TTL low, replace servo bd. (P/N 30103)	5.4
	Defective P. C. bd(s)	Various seek, write and/or read problems can result in a fault condition. See "Write Fault", pg. V-60; "Does not Seek on Command", pg. V-61; "Does not Read", pg. V-66; "Does not Write", pg. V-65.	

TROUBLESHOOTING GUIDE

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE
Does not seek on command (ready light on)	Illegal or invalid address requested	Check P31, P34 or terminator card for proper installation, check interface cables for damage Check 2U69 pin 6 (illegal address: ILLADR) on servo bd, if ever TTL high, illegal address was requested, check disc controller and I/O address lines	
	No seek strobe asserted	Check J12 pin 31 on I/O bd for high going 1µs pulse If pulse exists: Is seek complete, 3U42 pin 8 on servo bd, TTL low during pulse? If so, check disc controller timing;replace servo bd (P/N 30103) If no pulse exists at J12 p 31: Check tag 1/2U25 pin 9 on I/O bd if none, check connectors P31,P34 or terminator card and interface cables If tag 1, is moving head unit selected? Is ready line hi (J12 pin 29 on I/O bd) If ready is low, see "Proper Voltages on all Boards", Pg. and "Ready Line Stays Low", Pg. V-59.	
	Uncleared seek late	Issue "Restore" or momentarily switch power off (controller should issue restore when "Seek Error" is high).	

TROUBLESHOOTING GUIDE

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE
Sporadic missed seeks or relay K1 on power amp bd drops occasionally	Defective servo bd	Adjust or replace servo bd (P/N 30103)	5.6
Continuous data errors (errors common to both write and read)	Some faulty address lines	Check P31, P34 or terminator card for proper installation. Check interface cables for damage	
		Replace I/O bd	
	Invalid head selected	Check P31, P32, P33, P34 and/or terminator card for proper installation, check interface cables for damage	4.4.2
		Check for valid head address on matrix bd, check 1U11 pin 1,2,3, 4, 5, 6,7, 9, 10, 11, 1U14 pin 3, 5. One pin should be TTL low, all others @ +24V. On optional fixed head amplifiers: Check 1U2 pin 1, 2, 3, 4, 5, 6, 7, 9, 1U5 pin 1, 2, 3, 4, 5, 6, 7, 9, 1U7 pin 1, 2, 3, 4, 5, one pin should be TTL low, all others @ +24V AND check 1U10 pin 7, 12, 1U11 pin 7, 12, and 1U12 pin 7, 12, one pin should be -5V, all others @ +24V	4.4.3
		Check (moving) head address lines and optional fixed head address lines on I/O bd	

TROUBLESHOOTING GUIDE

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE
Continuous data errors (errors common to both write and read) (cont.)	Neither moving head nor fixed head unit selected	Check P31, P32, P33, P34 and/or terminator card for proper installation, check interface cables for damage	
		Check 2U51 on I/O board or optional thumbwheel switches for unit addresses	5.9.1
	Voltage regulators on data bd defective	Check 3U39 pin 4 on data board for -12V, U39 pin 7 for +8V; replace data bd (P/N 30102)	
	Data bd phase-locked-loop out of lock	Check 3U39 pin 6, should be -5VDC to -9VDC w/200mVp-p noise, repair or replace data bd (P/N 30102)	4.4.5
Continuous data errors (moving or fixed head only)	Voltage regulators	Moving head: Check matrix bd 1U2, U4, U6, U10 (right-hand most pin on each) for +24V, -24V, -5V, +8V respectively, repair or replace matrix bd (P/N 30440) Optional fixed heads: Check fixed head amplifier bd (FHA bd) 1U3, 1J4, output pin, for +24V, -24V respectively, repair or replace board (P/N 30104)	

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE

Does not write (cont.)	Write enable not asserted	Check J11 pin 5 on I/O bd, should be TTL low during write, if so and
		1. moving heads only, repair or replace matrix board (P/N 30440)
		2. optional fixed heads only, replace FHA board (P/N 30104)
		3. all heads, replace data board (P/N 30102)
		Fault Condition, see "Ready Light Flashes", pg. V-60.
		
		Controller fault, simultaneous assertion of
		  1. write and read
		  2. 2 or more tags
		  3. write and servo offset (+ or -)
		or write when not on cylinder
			4.5

	No write clock	Check P31, P33, P34 and/or terminator card for proper installation, check interface cables for damage Check 3U46 pin 7 on data board, should have 7.97 MHz TTL square wave, if not, check "WTCLK" on I/O bd (3U62 pin 4), repair or replace defective P.C. board (P/N 30115)	

V-65

V-66

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE
Does not write (cont.)	No write data (NRZ)	Check P31, P32, P33, P34 and/or terminator card for proper installation, check interface cables for damage Check J11 pin 7 on I/O bd for NRZ data during write. If data exists Repair or replace data board (P/N 30102). If all heads bad, Repair or replace matrix board (P/N 30440). If moving heads bad, Repair or replace FHA board (P/N 30104). If no data at J11 pin 7, repair or replace I/O bd (P/N 30115)	
	Maladjusted write current	Adjust matrix or optional FHA board as necessary	5.7
Does not read	Read enable not asserted	Check P31, P32, P33, P34 and/or terminator card for proper installation, check interface cables for damage Check J11 pin 15 on I/O bd, should be low during read, if not, check power to I/O board, repair or replace (P/N 30115)	

TROUBLESHOOTING GUIDE

SYMPTOM	PROBABLE CAUSE	REMEDY	REFERENCE
Does not read (cont.)	No read clock and/or no read NRZ data	Check 3U49 pin 13 on data bd, should be 7.97 MHz TTL square wave. If not, check all data board taps are not missing or open. If taps OK repair or replace data board (P/N 30102)	5.8
	Continuous read errors	Does unit write correctly? See "Does not Write", pg. V-64.	5.8
		Moving and optional fixed heads: Adjust or replace data board (P/N 30102), replace I/O board (P/N 30115)	
		Moving heads only: replace matrix board (P/N 30440) Fixed heads only: replace FHA board (P/N 30104)	
		Controller error: tries to read, (1) and write simultaneously; (2) when not on cylinder	
	Sporadic read errors	All heads: adjust or replace data board (P/N 30102)	5.8
		Moving heads only: Check if write current set properly, replace matrix board (P/N 30440)	4.4.2 3 5.7.1
		Optional fixed heads only: Check if write current set properly, replace FHA board (P/N 30104)	4.4.3 3 5.7.2

OSM 3300 DISC DRIVE SPARE PARTS LIST

This list contains: (a) Those parts necessary to
maintain the drive assembly, and (b) Those parts
necessary to repair printed circuit boards.

It is recommended that the customer who services
his own drives maintain an inventory of spare parts
as indicated in the columns, based on the number of
drives in his field population.

Only active and precision components are listed,
since remaining items on the printed circuit board
parts list are readily available resistors and
capacitors.

OSMP   3300 DISC DRIVE
RECOMMENDED SPARE PARTS LIST

PART NO.	DESCRIPTION	MACHINE POPULATION							
		1-9	10-24	25-49	50-99	100-199	200-499	500-999	1000-UP
30258-1	Belt, Spindle Drive 60 Hz	1	2	3	5	10	20	40	80
30258-2	Belt, Spindle Drive 50 Hz	1	2	3	5	10	20	40	80
30258-3	Belt, Blower	1	2	3	5	10	20	40	80
30243-1	Motor, Spindle Drive - 115V, 50/60 Hz	1	1	2	2	4	8	10	15
30243-2	Motor, Spindle Drive - 240V, 50/60 Hz	1	1	2	2	4	8	10	15
SU2A1	Fan, Heat Sink	1	2	3	4	4	8	8	15
30205	Filter, Air Breather Assy.	2	4	6	10	20	40	80	100
	Bearing Replacement Kit, Blower Spindle (Contains two bearings & retaining ring.)	1	1	2	2	4	8	10	15
30330	Index Sensor Assy.	1	2	3	4	8	10	15	20
30247	Solenoid Assy., Spindle Brake	1	1	2	3	6	12	18	25
30322	Spring, Spindle Brake	2	4	6	10	20	40	80	100
30290	Switch Assy., Spindle Brake	1	2	3	5	10	15	20	30
30226	Brake Band Assy.	1	2	3	5	10	15	20	30
LTA 211-TAMB	Switch, ON/OFF 120V	1	1	2	2	4	8	10	15
LTA 211-TAMB w/240Vlamp	Switch, ON/OFF·240V	1	1	2	2	4	8	10	15
05-125	Switch, Pushbutton (Write Protect)	1	1	2	2	4	8	10	15
05-105	Indicator	1	1	2	2	4	8	10	15
GE-85	Lamp, (Ready or Write Protect)	4	6	8	10	20	40	80	150
R10-ET-W4-V700	Relay, Positioner	1	2	3	4	8	10	12	15
2N6284	Power Transistor	2	3	4	5	10	20	40	80
2N6287	Power Transistor	2	3	4	5	10	20	40	80
NO #	Positioner Motor Kit (Contains Stator, Rotor, Lower Bearing, Ret. Ring)		1	2	2	4	8	1	15

OSMP   3300 DISC DRIVE
RECOMMENDED SPARE PARTS LIST

PART NO.	DESCRIPTION	MACHINE POPULATION							
		1-9	10-24	25-49	50-99	100-199	200-499	500-999	1000-UP
MDA-990-2	Power Supply Rectifier	1	1	2	2	4	8	15	30
KB-8	Relay, Spindle Motor Start 115V	1	4	6	8	16	25	50	100
KB-2	Relay, Spindle Motor Start 240V	1	1	2	2	4	8	15	25
KB-6	Relay, Spindle Motor Start 100V	1	2	3	4	8	15	25	50
30102	Date PCB Assy.	2	3	5	6	10	15	20	25
30103	Servo Logic PCB Assy.	4	6	8	10	15	20	25	30
30440	Matrix PCB Assy.	1	2	3	4	8	12	16	20
30332	Power Amplifier Assy.	1	2	3	4	8	12	16	20
30104	*Fixed Head Amplifier PCB Assy.								
	(.72m Byte)	1	2	3	4	8	12	16	20
	Fuse, 4 amp. 32V (All Units)	5	10	15	20	50	100	150	200
	Fuse, 5 amp. 32V (All Units)	5	10	15	20	50	100	150	200
	Fuse, 10 amp. 32V (All Units) (115V	10	20	30	40	50	100	150	200
	Fuse, 15 amp. (Slow Blow) 250V Units)	5	10	15	20	50	100	150	200
	Fuse, 4 amp. 250V (115V Units) (240V	5	10	15	20	50	100	150	200
	Fuse, 8 amp. (Slow Blow) 250V Units)	5	10	15	20	50	100	150	200
	Fuse, 2 amp. 250V (240V Units)	5	10	15	20	50	100	150	200
30115-1	*Interface PCB Assy.	1	2	3	4	6	8	10	12
30115-2	*Interface PCB Assy.	1	2	3	4	6	8	10	12
30115-3	*Interface PCB Assy.	1	2	3	4	6	8	10	12
30115-4	*Interface PCB Assy.	1	2	3	4	6	8	10	12
30115-5	*Interface PCB Assy.	1	2	3	4	6	8	10	12
30115-6	*Interface PCB Assy.	1	2	3	4	6	8	10	12
	*A number of optional PCB's are available. Consult Okidata for pricing.								

OSMP   3300 DISC DRIVE
RECOMMENDED SPARE PARTS LIST

PART NO.	DESCRIPTION	MACHINE POPULATION							
		1-9	10-24	25-49	50-99	100-199	200-499	500-999	1000-UP
1N4150	Diode	5	10	15	20	40	60	80	100
1N4002	Diode	5	10	15	20	40	60	80	100
1N4934	Diode	2	3	5	10	20	40	70	100
1N5232B	Diode	2	3	5	10	20	40	70	100
1N5243B	Diode	2	3	5	10	20	40	70	100
1N5230C	Diode	2	3	5	10	20	40	70	100
1N5229C	Diode	2	3	5	10	20	40	70	100
1N5235B	Diode	2	3	5	10	20	40	70	100
1N3062	Diode	2	3	5	10	20	40	70	100
2N2369A	Transistors	2	3	5	10	20	40	60	80
2N2222A	Transistors	2	3	5	10	20	40	60	80
2N2905A	Transistors	3	6	8	12	25	50	75	100
2N2907A	Transistors	2	3	5	10	20	40	60	80
2N3440	Transistors	2	3	5	10	20	40	60	80
2N5415	Transistors	2	3	5	10	20	40	60	80
MPSA06	Transistors	2	3	5	10	20	40	60	80
4308-101-820	Resistor N/W	2	3	5	10	20	40	60	80
898-3-470	Resistor N/W	2	3	5	10	20	40	60	80
AH5012CN	I. C.	2	3	5	10	20	40	60	80
10136	I. C.	2	3	4	5	10	20	40	80
LM3046	I. C.	3	6	8	12	25	50	75	100
LM3146	I. C.	2	3	4	6	12	15	30	60
LM339	I. C.	2	3	4	6	12	15	30	60
LM355N	I. C.	2	3	4	5	10	20	40	80
LM319	I. C.	2	3	5	7	15	30	60	100

OSMP   3300 DISC DRIVE
RECOMMENDED SPARE PARTS LIST

PART NO.	DESCRIPTION	MACHINE POPULATION							
		1-9	10-24	25-49	50-99	100-199	200-499	500-999	1000-UP
LM304	I. C.	2	3	4	5	10	20	40	80
MC10104	I. C.	2	3	5	7	15	30	60	100
MC10102	I. C.	2	3	4	6	12	25	50	100
MC10105	I. C.	2	3	4	5	10	20	40	80
MC10106	I. C.	2	3	4	5	10	20	40	80
MC10109	I. C.	2	3	4	5	10	20	40	80
MC10113	I. C.	2	3	4	5	10	20	40	80
MC10116	I. C.	2	4	6	8	15	30	60	100
MC1458CPI	I. C.	3	5	8	10	20	40	80	100
MC1456CPI	I. C.	4	7	10	13	25	50	100	200
MC10125	I. C.	2	3	4	5	10	20	40	80
MC10124	I. C.	2	3	4	5	12	25	50	100
MC7808CP	I. C.	2	3	4	5	10	20	40	80
MC7812CK	I. C.	2	3	4	5	10	20	40	80
MC10131P	I. C.	3	5	8	10	20	40	80	100
MC7824CP	I. C.	2	3	4	5	10	20	40	80
MC7908CP	I. C.	2	3	4	5	10	20	40	80
MC7924CP	I. C.	2	3	4	5	10	20	40	80
MC7905CP	I. C.	2	3	4	5	10	20	40	80
MC7912CK	I. C.	2	3	4	5	10	20	40	80
MC7912CP	I. C.	2	3	4	5	10	20	40	80
UA7230DC	I. C.	2	3	4	5	10	20	40	80
MC3408	I. C.	2	3	4	5	10	20	40	80
MC7902CK	I. C.	2	3	4	5	10	20	40	80
MC10141	I. C.	2	3	4	5	10	20	40	80

OSMP 3300 DISC DRIVE
RECOMMENDED SPARE PARTS LIST

PART NO.	DESCRIPTION	MACHINE POPULATION							
		1-9	10-24	25-49	50-99	100-199	200-499	500-999	1000-UP
MPSA56	Transistors	4	6	8	10	20	40	80	100
MJ2500	Transistors	4	6	8	10	20	40	80	100
MM8006	Transistors	2	3	4	5	10	20	40	80
E177	Transistors	2	3	5	6	12	25	50	100
E106	Transistors	2	3	4	5	10	20	40	80
100K	Potentiometers	2	3	4	5	10	20	40	80
100ohm	Potentiometers	2	3	4	5	10	20	40	80
10K	Potentiometers	2	3	4	5	10	20	40	80
1K	Potentiometers	2	3	4	5	10	20	40	80
20K	Potentiometers	2	3	4	5	10	20	40	80
2K	Potentiometers	2	3	4	5	10	20	40	80
200ohm	Potentiometers	2	3	4	5	10	20	40	80
.1r 3W 3%	PWR Resistors	2	3	4	5	10	20	40	80
2.4K 1/2W 5%	PWR Resistors	2	3	4	5	10	20	40	80
2.7K 1/2W 5%	PWR Resistors	2	3	4	5	10	20	40	80
250r 3W 5%	PWR Resistors	2	3	4	5	10	20	40	80
2.2r 2W	PWR Resistors .	2	3	4	5	10	20	40	80
2.4K 1W 5%	PWR Resistors	2	3	4	5	10	20	40	80
1K 5W 5%	PWR Resistors	2	3	4	5	10	20	40	80
200r 1W 1%	PWR Resistors	2	3	4	5	10	20	40	80
50r 5W 1%	PWR Resistors	2	3	4	5	10	20	40	80
.05r 7W 1%	PWR Resistors	2	3	4	5	10	20	40	80
.05r 7W 3%	PWR Resistors	2	3	4	5	10	20	40	80
100r 3W 1%	PWR Resistors	2	3	4	5	10	20	40	80
100r 3W 5%	PWR Resistors	2	3	4	5	10	20	40	80

OSMP 3300 DISC DRIVE
RECOMMENDED SPARE PARTS LIST

PART NO.	DESCRIPTION	MACHINE POPULATION							
		1-9	10-24	25-49	50-99	100-199	200-499	500-999	1000-UP
100r 15W	PWR Resistors	2	3	4	6	10	20	40	80
500r 3W 5%	PWR Resistors	2	3	4	5	10	20	40	80
100r (Bournes)	Resistor N/W	8	12	15	19	40	80	150	300
10K (SIP)	Resistor N/W	4	6	8	10	20	40	80	100
10K (RPI)	Resistor N/W	4	6	8	10	20	40	80	100
22K (SIP)	Resistor N/W	4	6	8	10	20	40	80	100
4N4-002-103	Resistor N/W	4	6	8	10	20	40	80	100
4116R-002-560	Resistor N/W	4	6	8	10	20	40	80	100
4308-102-471	REsistor N/W	4	6	8	10	20	40	80	100
MCM7641	I. C.	2	3	4	5	10	20	40	80
NE555V	I. C.	2	3	4	5	10	20	40	80
NE592A	I. C.	4	6	8	10	20	40	80	100
MC10164	I. C.	2	4	6	8	16	30	60	100
74LS00	I. C.	10	15	20	25	50	100	200	400
74LS04	I. C.	2	4	5	6	12	25	50	100
74LS30	I. C.	2	4	6	8	16	30	60	100
74LS08	I. C.	5	8	12	15	30	60	100	150
74LS11	I. C.	2	4	6	8	16	30	60	100
74LS21	I. C.	2	4	6	8	16	30	60	100
74LS54	I. C.	2	4	5	6	12	25	50	100
7416	I. C.	2	4	5	6	12	25	50	100
7406	I. C.	2	3	4	5	10	20	40	80
74LS10	I. C.	2	4	5	6	12	25	50	100
74LS51	I. C.	2	4	6	8	16	30	60	100
74LS02	I. C.	2	4	5	6	12	25	50	100

OSMP 3300 DISC DRIVE
RECOMMENDED SPARE PARTS LIST

PART NO.	DESCRIPTION	MACHINE POPULATION							
		1-9	10-24	25-49	50-99	100-199	200-499	500-999	1000-UP
74LS74	I. C.	8	12	16	20	40	80	150	300
74LS86	I. C.	2	4	6	8	16	30	60	100
74LS32	I. C.	2	4	5	6	12	25	50	100
74LS37	I. C.	2	3	4	5	16	20	40	80
74LS74	I. C.	2	3	4	5	16	20	40	80
74LS266	I. C.	4	6	8	10	20	40	80	100
75451	I. C.	2	3	4	5	10	20	40	80
7445	I. C.	4	6	8	10	20	40	80	100
74LS279	I. C.	2	3	4	5	10	20	40	80
74LS138	I. C.	2	4	6	8	16	30	60	100
74LS175	I. C.	8	12	16	20	40	80	150	300
74LS14	I. C.	5	8	12	15	30	60	100	200
74LS283	I. C.	2	4	6	8	16	30	60	100
75471	I. C.	4	6	8	10	20	40	80	100
74LS157	I. C.	2	3	5	6	12	25	50	100
74LS191	I. C.	5	8	12	15	30	60	100	200
75107B	I. C.	8	12	16	20	40	80	150	300
74LS221	I. C.	2	3	4	5	10	20	40	80
74S124	I. C.	2	3	4	5	10	20	40	80
74221	I. C.	2	3	4	5	10	30	40	80
75110	I. C.	10	15	20	25	50	100	200	400
733	I. C.	2	3	4	5	10	20	40	80
74S288	I. C.	2	3	4	5	10	20	40	80
9601	I. C.	2	3	4	5	10	20	40	80
9602	I. C.	2	4	6	8	16	30	60	100

BLOCK DIAGRAM
3300 DISK DRIVE

OSMP, INC.

SIZE D   DWG NO. 70801600   TYPE SC   SHEET 1 of 1   REV D

ASSEMBLY DRAWING
MATRIX P.C. Bd.

OSMP. INC.

SIZE C	FSCM NO.	DWG. NO. 71501500			REV. E
SCALE 2X				SHEET 1 OF 5	

DO NOT SCALE DRAWING

SEE PARTS LIST SHEETS 3 THRU 5

MATRIX CARD (SCHEMATIC)

OSMP INC.

DRAWING NO. 71701500

SEE DETAIL 'A' ③⑥

CHECK ALL MINI BUSSES (ITEMS 30, 31, & 32) FOR SHORTS AND INSTALL PRIOR TO I.C. INSTALLATION.

③⑧ ③⑥

U14 · U15

RP7 · TP10 · R15 / R16

DL3 · U21

DETAIL A SCALE 2X

③⑦ ③⑧

③ ③

②④ ②⑥ ②⑧

③ ③

②⑤ ②⑦ ②⑨

③②

③⑥ ③⑨

U43

R68 / R69 / R70

DL2

DETAIL B SCALE 2X

③⑥ SEE DETAIL 'B'

⑪②

②⑤ ②⑦ ②⑨

③① ④⓪ 32 PLCS

③⓪ ③⑨

②② ②③ 4 PLCS

3. R12 & R14 TO BE INSTALLED SO THAT WITH COMPONENT BODY .12" ABOVE BOARD SURFACE.

2. INSTALL USECO TERMINAL, ITEM 40, 32 PLACES FROM NEAR SIDE OF BOARD.

NOTES: 1. UNUSED REFERENCE DESIGNATIONS: R20

DATA ELECTRONICS
(READ AMP)

OSMP, INC.

DWG. NO. 71700700

REV. D

SHEET 1 of 3

NOTES: UNLESS OTHERWISE SPECIFIED.
1. RESISTORS IN OHMS, ¼W, 5%.
2. CAPACITORS IN μF.
3. [RP] = 100Ω RESISTORS TO -2V.
4. TRANSISTORS ARE LM3046.
5. USED IN AUTO ZERO OPTION ONLY.

DATA ELECTRONICS
(WRITE ENCODER)

OSMP, INC.

DATA BOARD

OSMP, INC.

DWG. NO. 71700700

SHEET 3 of 3

NOTES:
1. ALL RESISTORS 5% ¼W
2. SELECT IN TEST FROM FOLLOWING VALUES:
   1.0 pf
   3.0 pf
   5.0 pf
   7.0 pf
   10.0 pf
3. 5636 BPI ONLY
4. 6060 BPI ONLY
5. * U9 IS A FAIRCHILD 95105 DC.

ADD RESISTOR

REVISIONS

REV	DESCRIPTION	DATE	APPR
A	ECN 6063 PRODUCTION RELEASE	8-9-77	
B	ECN 6144, 6187, 6196	6 DEC 79	

NOTE HDWARE ORIENTATION

R5 AND R6:
COMPONENT BODY TO BE
.125" MIN. FROM BOARD

GND

OSMP, INC.

ASSEMBLY

SERVO LOGIC BOARD

SCALE 1/1		REVISED REV E
DATE 6-5-77		SH. 1 OF 10
		DRAWING NUMBER
		7150
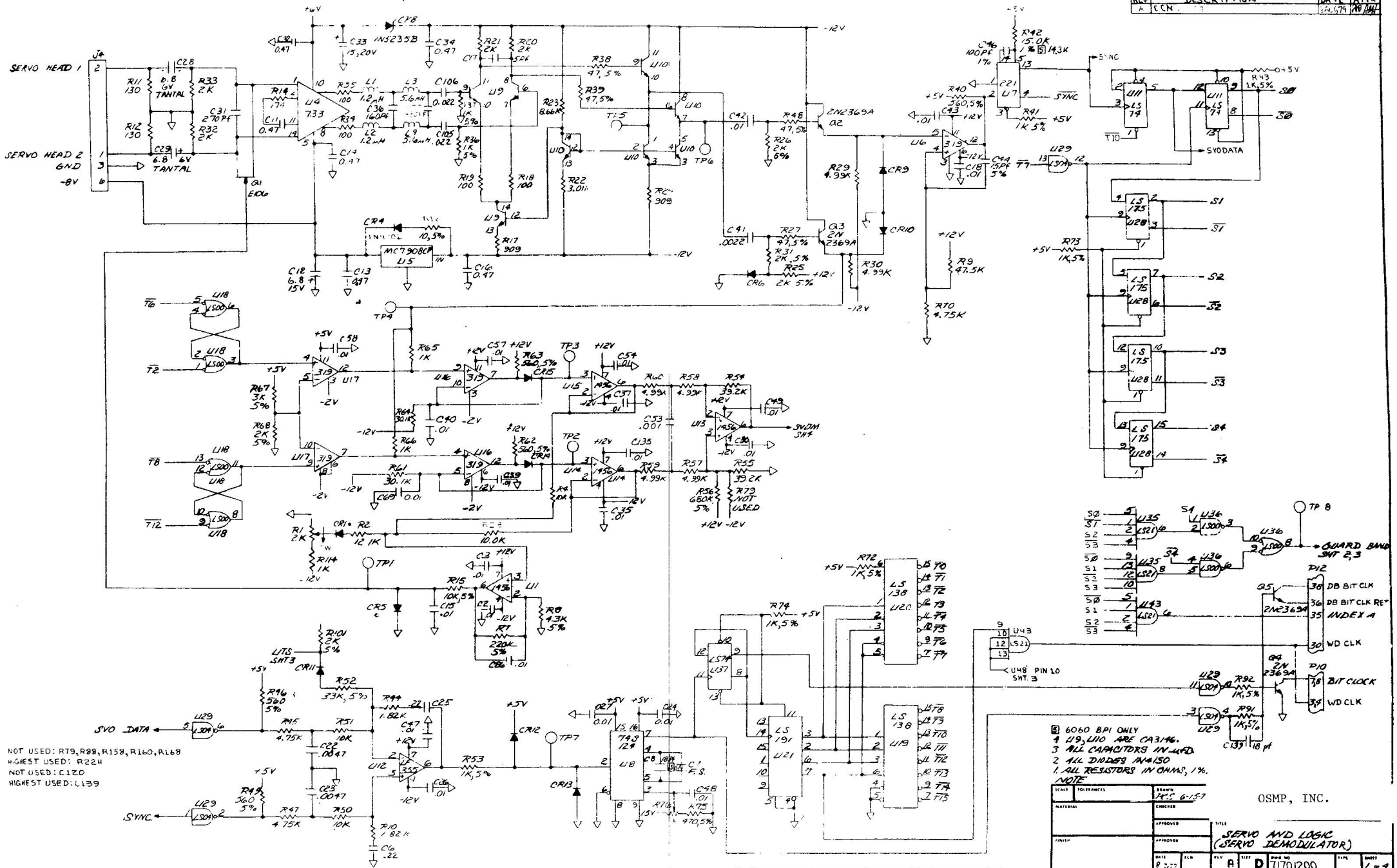
SERVO AND LOGIC
(SERVO DEMODULATOR)

OSMP, INC.

DWG NO. 71701200   REV A   SIZE D   SHEET 1 of 1
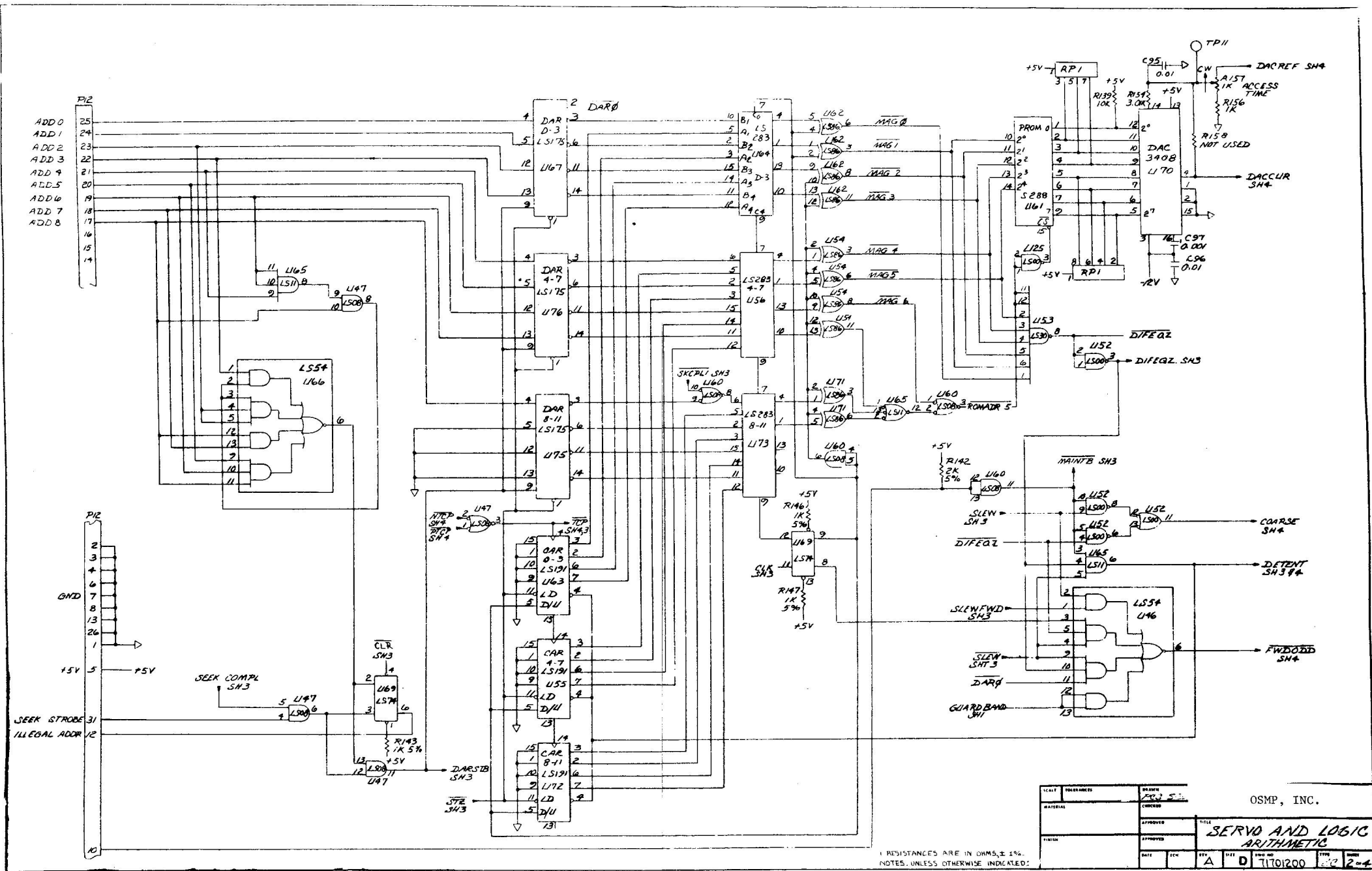
SERVO AND LOGIC
ARITHMETIC
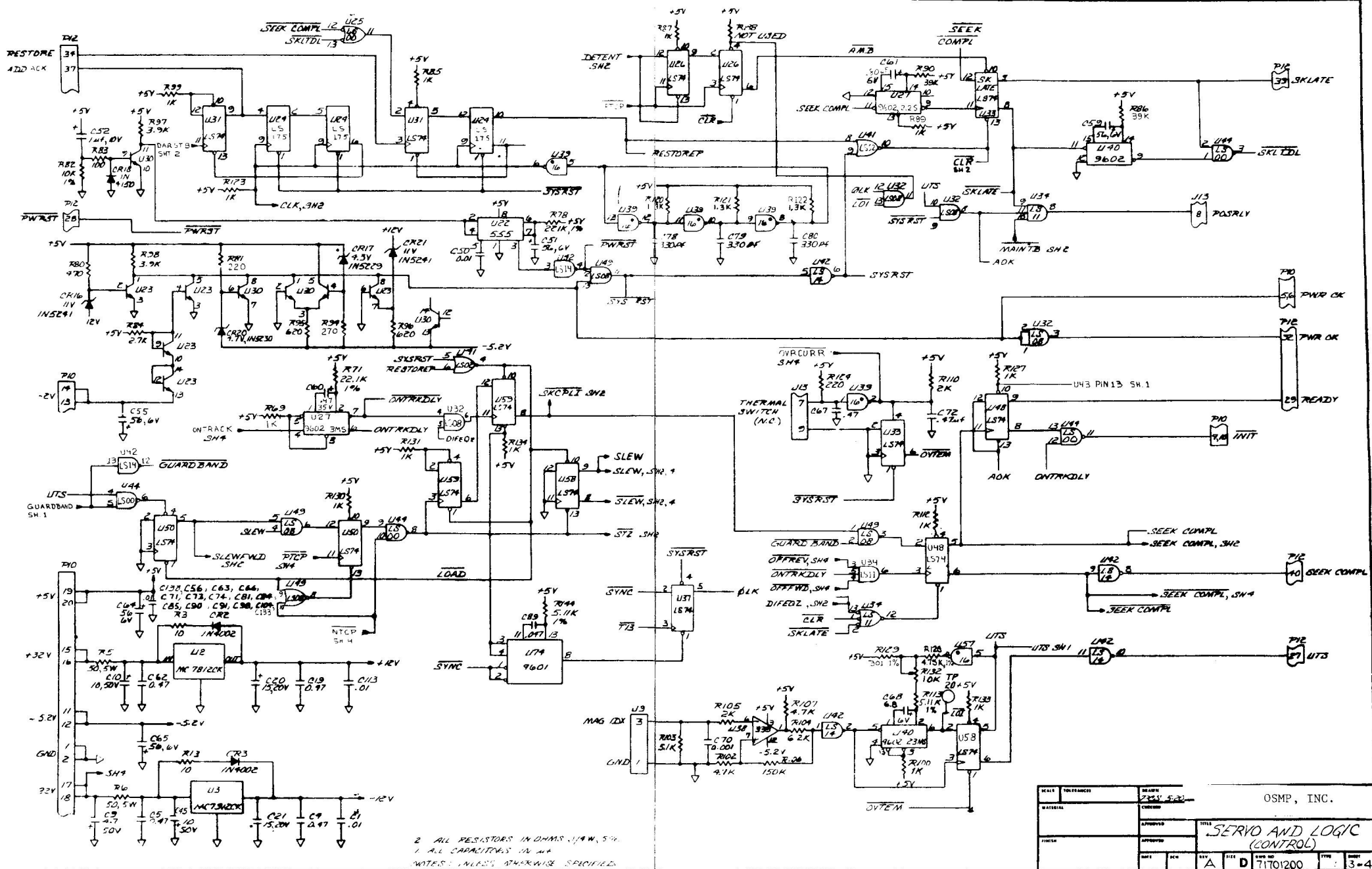
OSMP, INC.

SCALE	TOLERANCES		DRAWN		
MATERIAL			CHECKED		
			APPROVED		
			APPROVED		
FINISH			DATE	ECN	

DWG NO. 71701200   SHT 2-4

SERVO AND LOGIC (CONTROL)

OSMP, INC.

71701200

3-4

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITIES IN μf.
2. ALL RESISTORS IN OHMS, 1/4 W, 5%.

SERVO AND LOGIC (SERVO SYSTEM)

OSMP, INC.
WESTERN DIVISION · SANTA BARBARA, CALIFORNIA
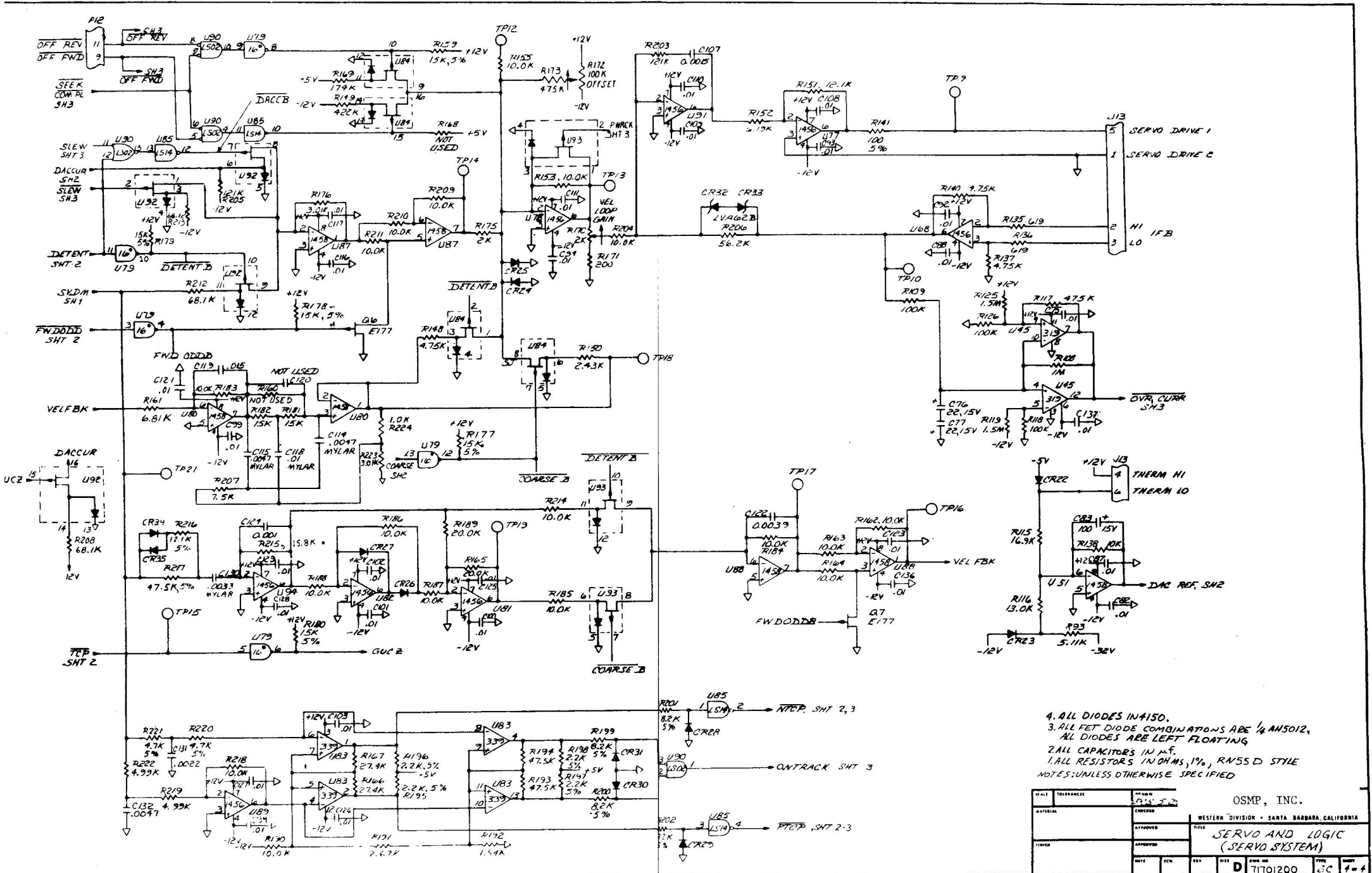
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS IN OHMS, 1%, RN55 D STYLE
2. ALL CAPACITORS IN μf.
3. ALL FET DIODE COMBINATIONS ARE ¼ AH5012, ALL DIODES ARE LEFT FLOATING
4. ALL DIODES IN4150.

SIZE D 71T01200 1-4

		OSMP, INC.		
SCALE	TOLERANCES	DRAWN ZAT 5JAN79	WESTERN DIVISION • SANTA BARBARA, CALIFORNIA	
MATERIAL		CHECKED 5-18-79	TITLE FIXED HEAD AMPLIFIER	
		APPROVED	ASSEMBLY DWG	
FINISH		APPROVED		
		DATE ECN REV B SIZE D DWG NO 71501800 TYPE	SHEET 1 of 5	
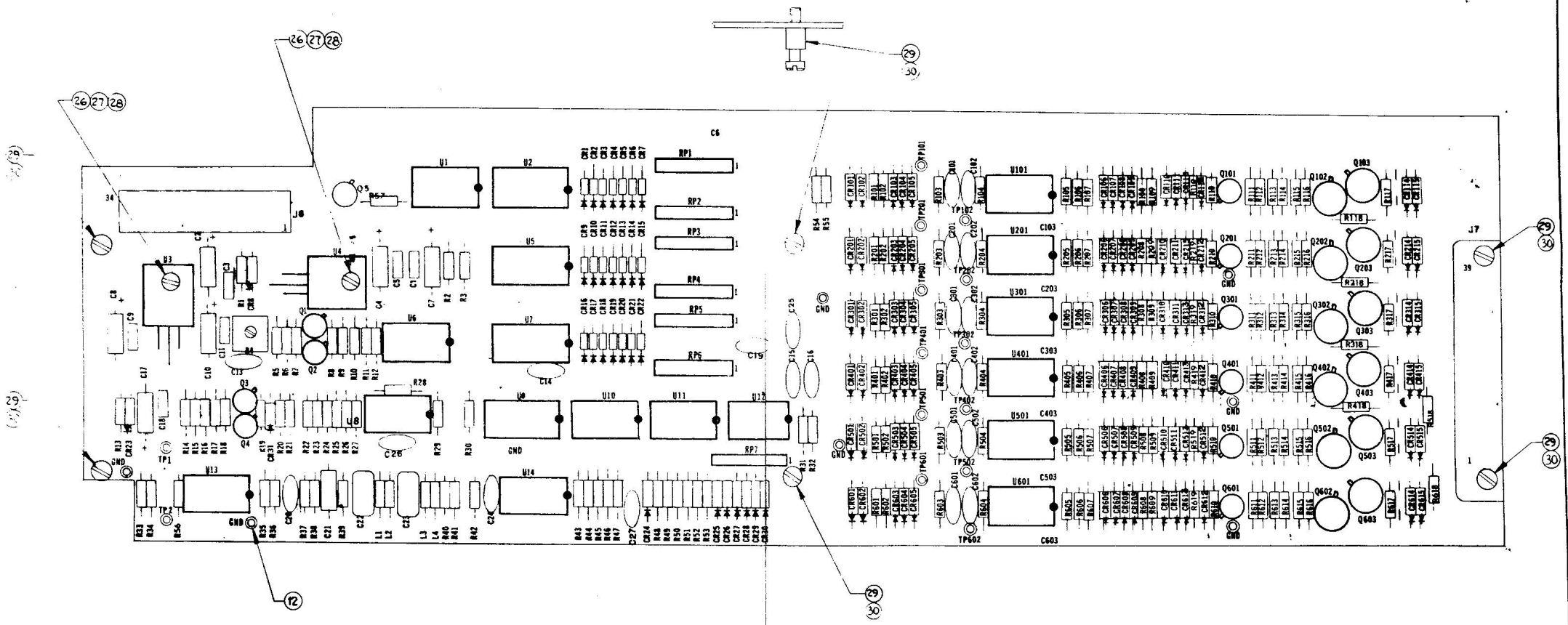
NOTES:
1. REF: SCHEMATIC 71701800 REV A   FAB 71601800 REV A

FIXED HEAD AMPLIFIER

OSMP, INC.
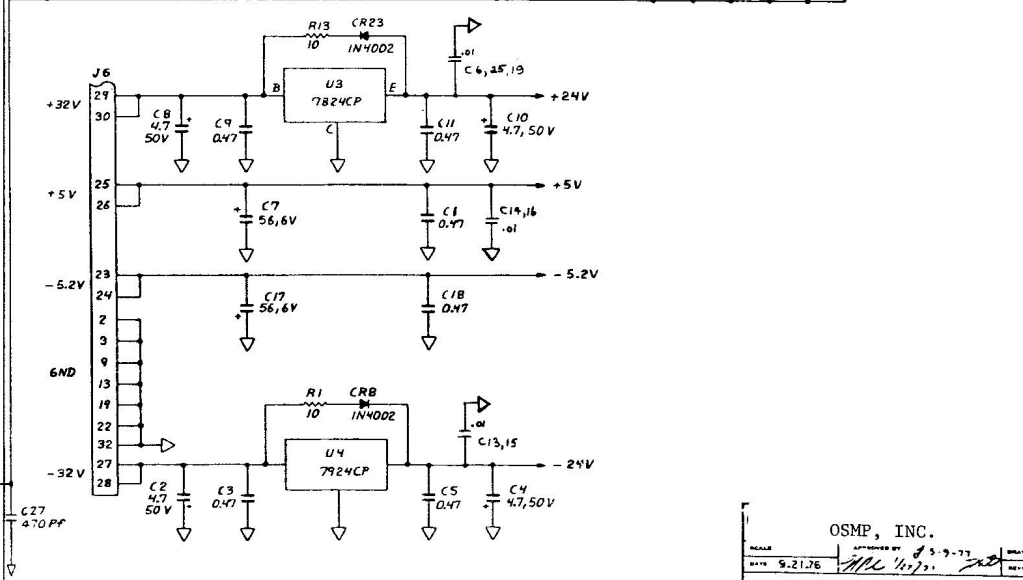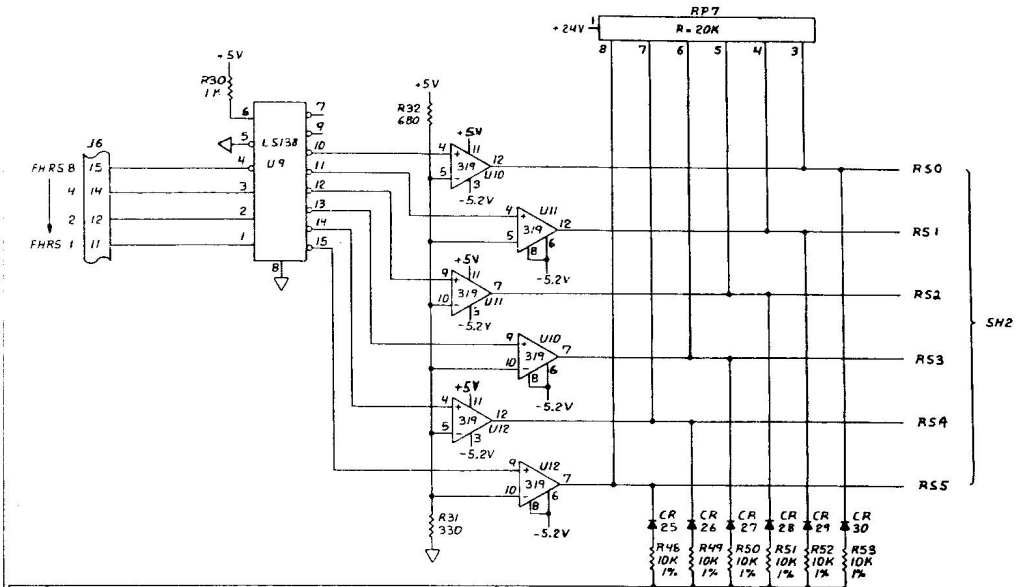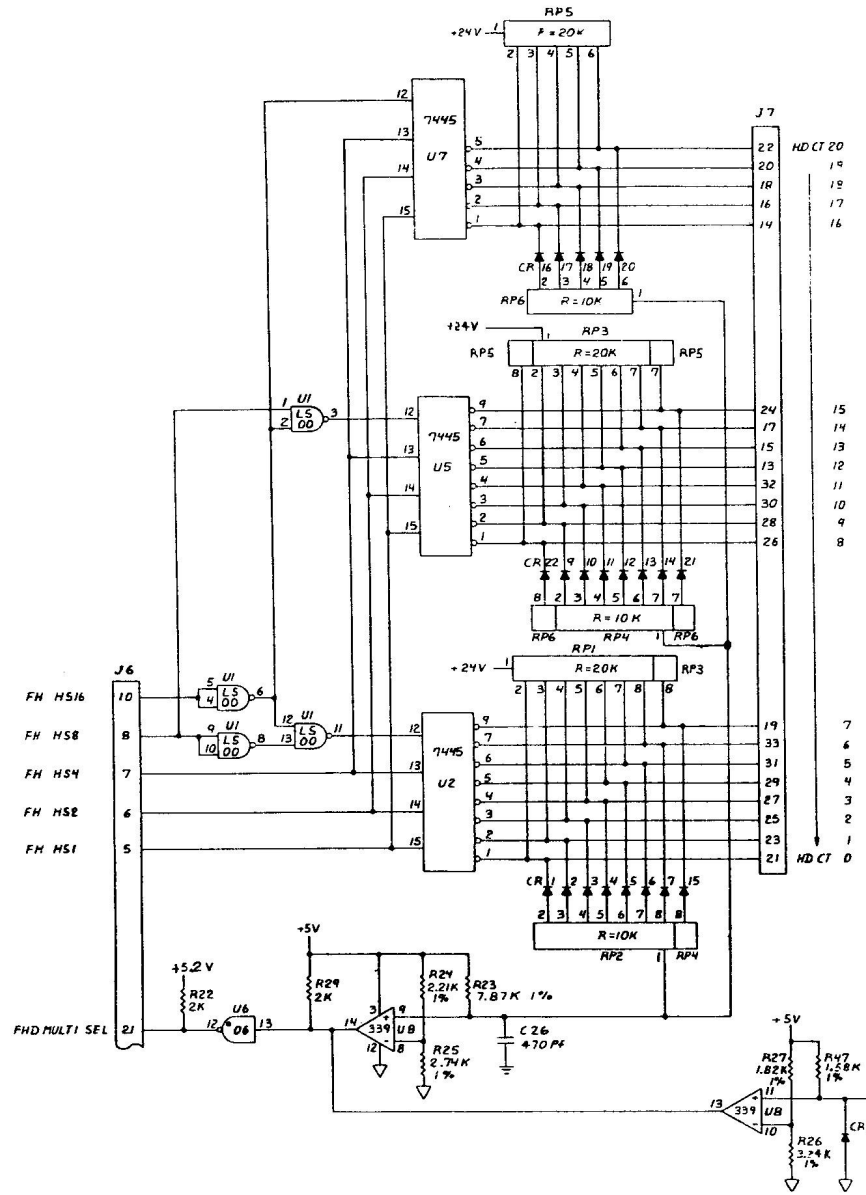
NOTE. 1. ALL DIODES ARE 1N4150
2. ALL RESISTORS IN OHMS, 1/4 W, 5%.

REV A — SHEET 1 OF 3 — 71701800

FIXED HEAD AMPLIFIER
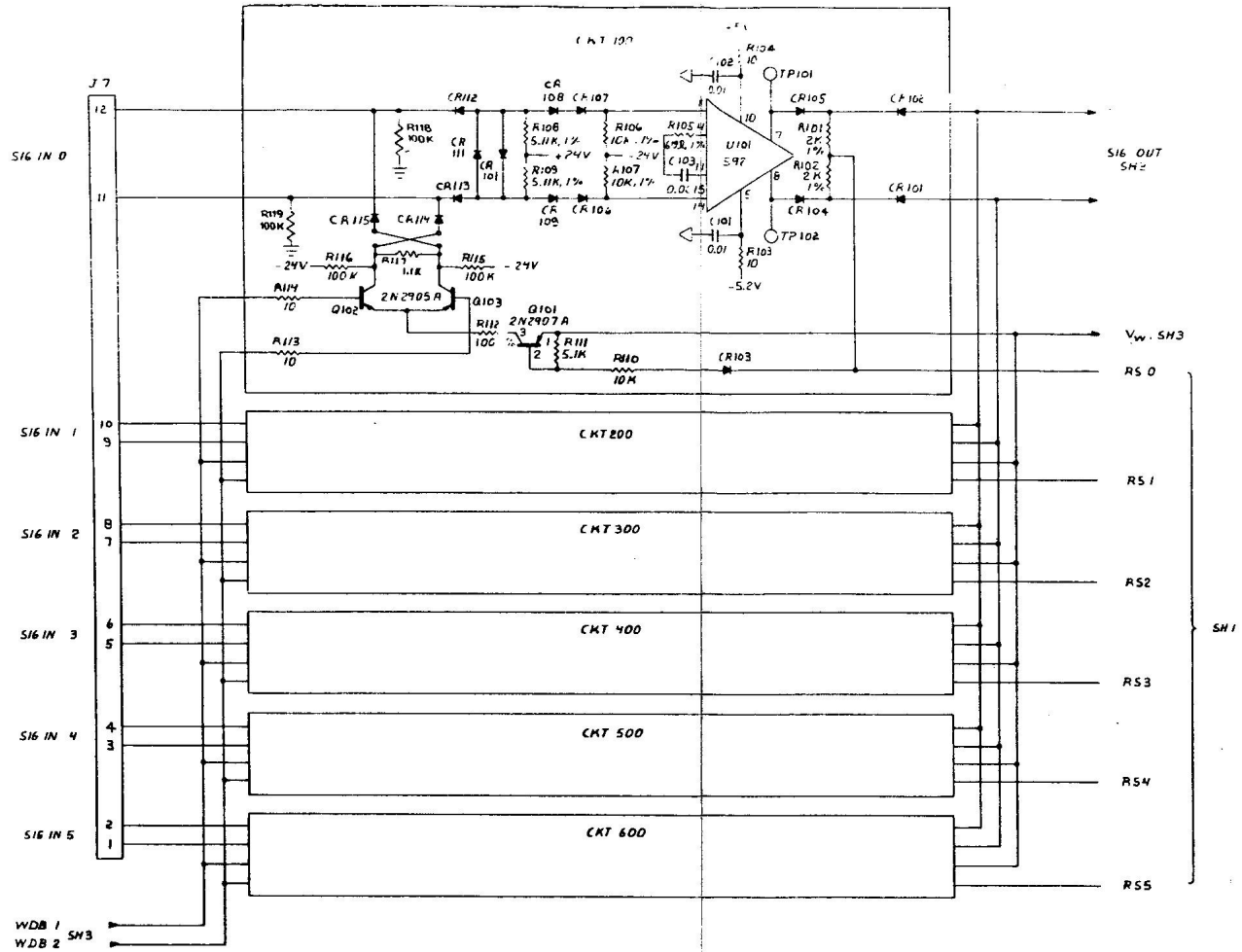
NOTES 1. ALL DIODES 1N4150
2. COMPONENTS IN EACH CIRCUIT HAVE 100, 200, ETC. ADDED TO THEIR PART NUMBERS.

NOTE : 1. INDUCTOR VALUES IN µH
2. ALL RESISTORS IN OHMS, 1/4 W, 5%.

NOTES: 1. R20, R21, & R26 TO BE RAISED .125 ABOVE BOARD SURFACE.

2. INSTALL ITEM 79 (TERMINAL-USECO #1299-B, 6 REQ'D) USING SWAGE TOOL USECO #1299.

3. FASTEN R23 & R24 TO TOP SECTION OF TERMINAL SO AS TO HAVE AT LEAST .150" CLEARANCE BETWEEN BOARD AND RESISTOR.

4. FASTEN C14 TO TOP SECTION OF TERMINALS. TOP SURFACE OF C14 SHOULD BE SAME HEIGHT AS R23 & R24.

NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTORS 5% 1/4W
2. CAPACITORS IN μF
3. ALL 1% RESISTORS ARE RN55D
4. ✳ TO BE INSULATED FROM GROUND

REV	DESCRIPTION	DATE	APPR
A	— ENGINEERING RELEASE — ECN 5918	15 FEB 79	
B	ECN 6159	19 NOV 79	
C	ECN 6175	30 JAN 80	

REVISIONS

TYP 8 PLCS

71502000
715010XX

71502000
'10 PLCS

71502000

71502000
715010XX

71502000
715010XX

71502000
715010XX

CUT PIN 10
(TOP PIN)

8 REQ

(71502000)

ONIDATA CORP
715010 REV
ASSEMBLY P.C. BOARD

① INSTALL USECO TERMINAL # 2060 B (8 PLCS)(ITEM 43. 71502000)
ON NEAR SIDE OF BD.

NOTES:

Schematic diagram: 3300 CDC 9760 - I/O

OSMP, INC.
WESTERN DIVISION • SANTA BARBARA, CALIFORNIA

TITLE: 3300 CDC 9760 - I/O

REV: B   SIZE: D   DWG. NO.: 71701000   TYPE: SC   SHEET: 1 of 3

NOTES:
1. DESIGNATIONS NOT USED: C14, C35, R57

RU2, RU4 = 82 Ω
RU1, RU3, RU5, RU6, RU7, RU8, RU9 = 470 Ω

3300 CDC 9760 - I/O

OSMP, INC.

SIZE D · DWG. NO. 7170 1000 · TYPE SC · SHEET 3 of 3 · REV B

ZONE	REV	DESCRIPTION	DATE	APPR
	A	ECN 5983 (PRODUCTION RELEASED)	30 MAR 79	2.J.L
	B	ECN 6190	30 JAN 80	CAC
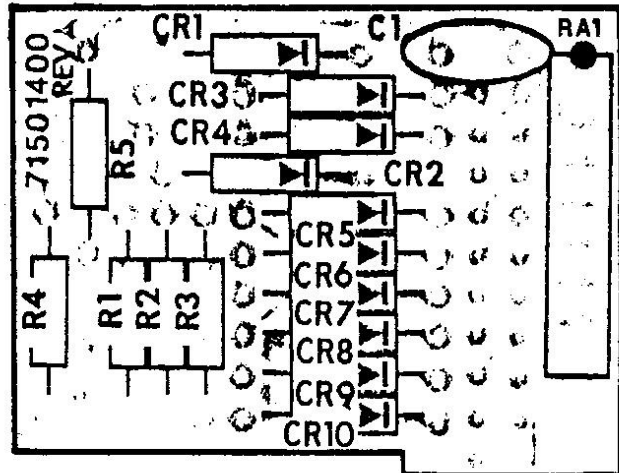
OKIDATA

ASSEMBLY

MATRIX CABLE SELECT

NOTES:

1. SCHEMATIC - DWG. No. 71701400.

MATRIX CABLE SELECT BOARD

REVISIONS

REV.	DESCRIPTION	DATE	APPROVED
A	ECN 5983 (PRODUCTION RELEASE)	30 MAR 79	𝓡.𝓢.𝓭.

+24V

R4
10K
5%
1/4W

NOTE 1

P2   RA-1

R5
10K
5%
1/4W

C1
.47μf

100K TYP.

CR3
CR4
CR1
CR2   NOTE 2
CURRENT LOOP
CR5
CR6
CR8
CR9

FROM MATRIX CARD   (Q6)   (Q5)

CR10   CR7

R2, 1.0K
1%, 1/10W

R1   R3
7.15K   7.15K
1%, 1/10W   1%, 1/10W
+24V
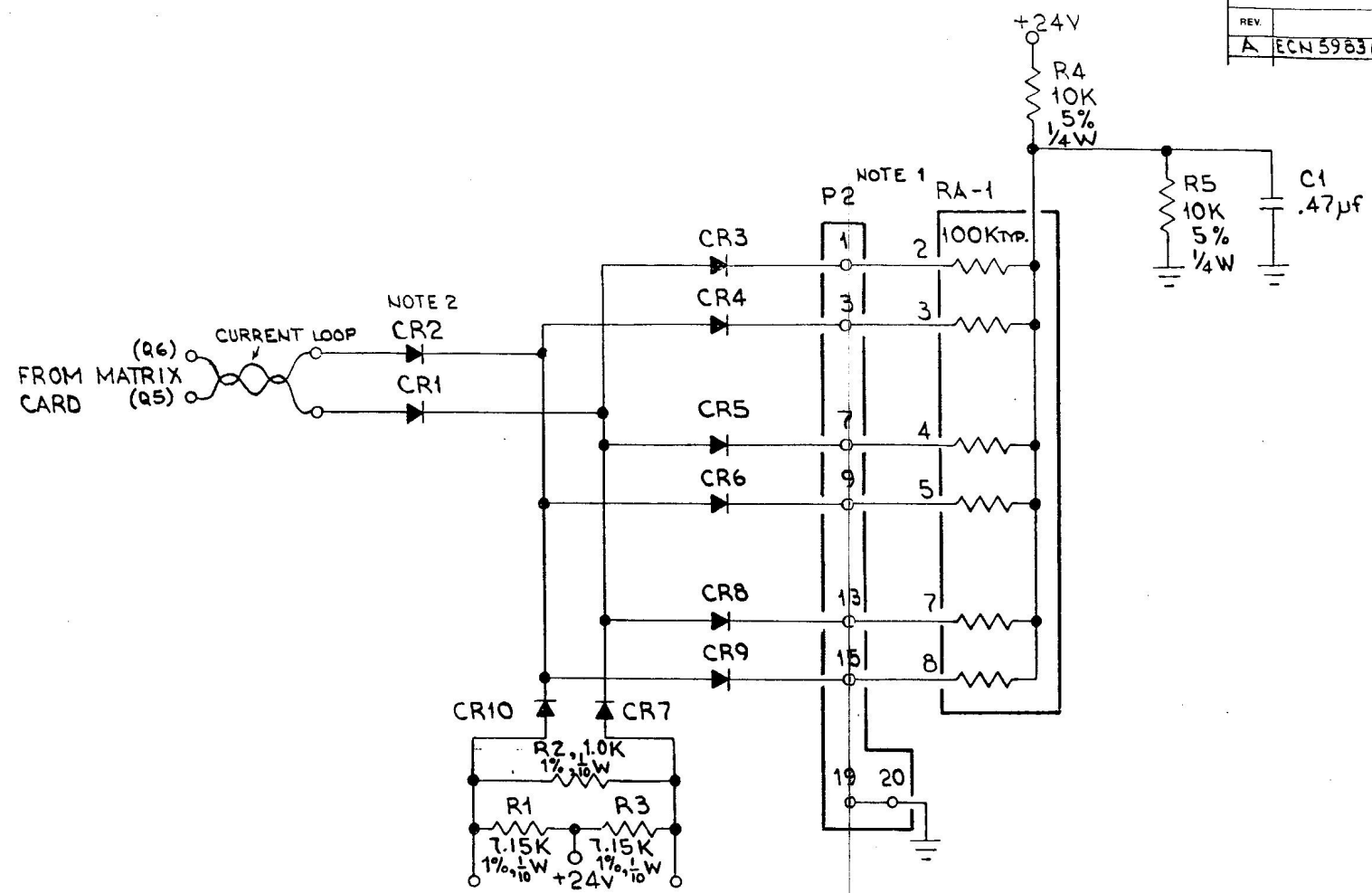
PIN CONNECT
→ Q7 ON MATRIX CARD

PIN CONNECT
→ Q8 ON MATRIX CARD

NOTES:

1. SEE MATRIX P.C.B. ASSY DWG. 71501500.
2. ALL DIODES 1N4150.
3. REF: MATRIX P.C.Bd. SCHEMATIC 71701500

71501400	3300
NEXT ASSY	USED ON

APPLICATION

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS   DECIMALS   ANGLES
±   .XX ±   ±
             .XXX ±

MATERIAL

FINISH

CONTRACT NO.

APPROVALS	DATE
DRAWN KONA	2/22/79
CHECKED	
ISSUED N.S.Porron	24 APR 79

OSMP, INC.

MATRIX CABLE SELECT BOARD

SIZE	FSCM NO.	DWG. NO.	REV.
B		71701400	A

SCALE

DO NOT SCALE DRAWING

SHEET 1 of 1

ASS'Y. 71502300 REV

R1
R2
R3
R4
R5
R6
U1
CR3 CR4
C2
R7
C3
+ C4
U2
C5
C7
CR2
R11
R12
Q1
R13
CR3
C6
CR4
CR5
R8
R9
R10
U3
J41

J40

㉑

⑧

J41 (ITEM 21)
CUT PINS 1 & 6

PIN 3

J40 (ITEM 8)
CUT PIN 3

㉙
㉚
⑪ (FARSIDE OF BOARD)

ELECTRONIC MOTOR START
P.C.B. CIRCUIT (SCHEMATIC)

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECN 6018 WAS 30465	5-29-79	
B	ECN 6051	20 JUNE 79	

NOTES: (UNLESS OTHERWISE SPECIFIED)
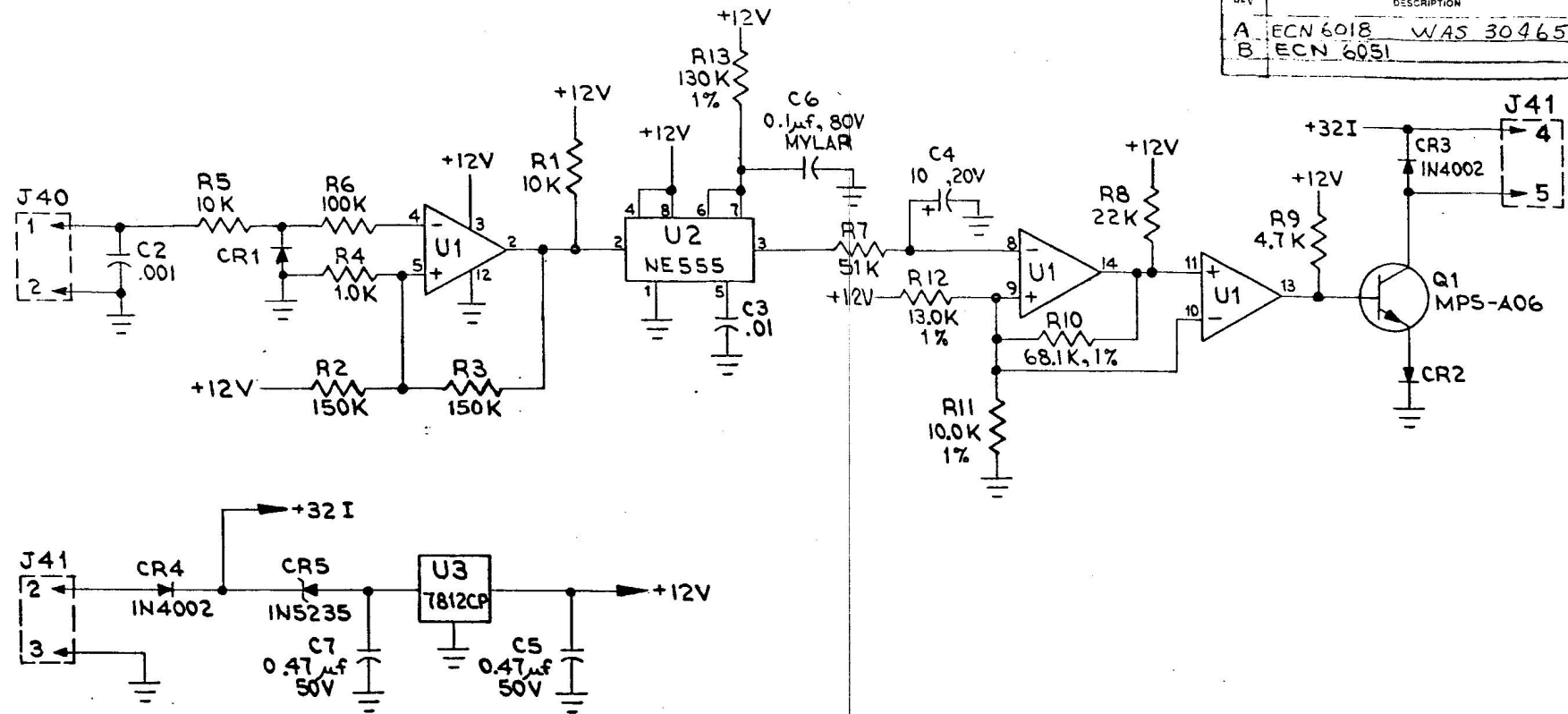
5. CAPACITOR VALUES IN μf.
4. U1 IS A LM339.
3. ALL DIODES ARE 1N4150.
2. ALL RESISTORS ARE $\frac{1}{4}$ W, ±5%, VALUES IN OHMS.
1. GND. UNUSED PINS ON U1.

-01 AC DISTRIBUTION BOX (100V - 130V)

JO

F1 15A 250V SLO-BLOW

FL RFI FILTER

GND

F2 4A 250V

BLK
WHT
BRN
BLU
GRN/YEL

P27

PWR ON/OFF

P22 J22
BLK
BLK
WHT

BRAKE ON NC NO

P26 J26
BLK
KEY
BLK

BRAKE INTERLOCK

FAN

P25 J25
KEY

SPINDLE MOTOR START RELAY 120V

K1

CABLE ASSY P41

J41 PCB

SPINDLE MTR.

P24 J24
BLK
BLUE
RED

RED

C1 400-480 µF 110 VAC

TABLE A

MODULE LINE	P27 PIN CONNECTIONS	
100	5-7 & 9	11-10 & 12
110	5-4 & 6	11-10 & 12
120	5-7 & 9	11-13 & 15
130	5-4 & 6	11-13 & 15
100	5, 4, 6	11, 10, 12
110	5, 7, 9	11, 10, 12
120	5, 4, 6	11, 13, 15
130	5, 7, 9	11, 13, 15
105	5, 4, 6	11, 10, 12
110	5, 7, 9	11, 10, 12
115	5, 4, 6	11, 13, 15
120	5, 7, 9	11, 13, 15

POWER SUPPLY ASSY

30334 , REV 'A' & 'B'

70008102 , REV 'C' TO CURRENT

70008101 , REV 'C' TO CURRENT
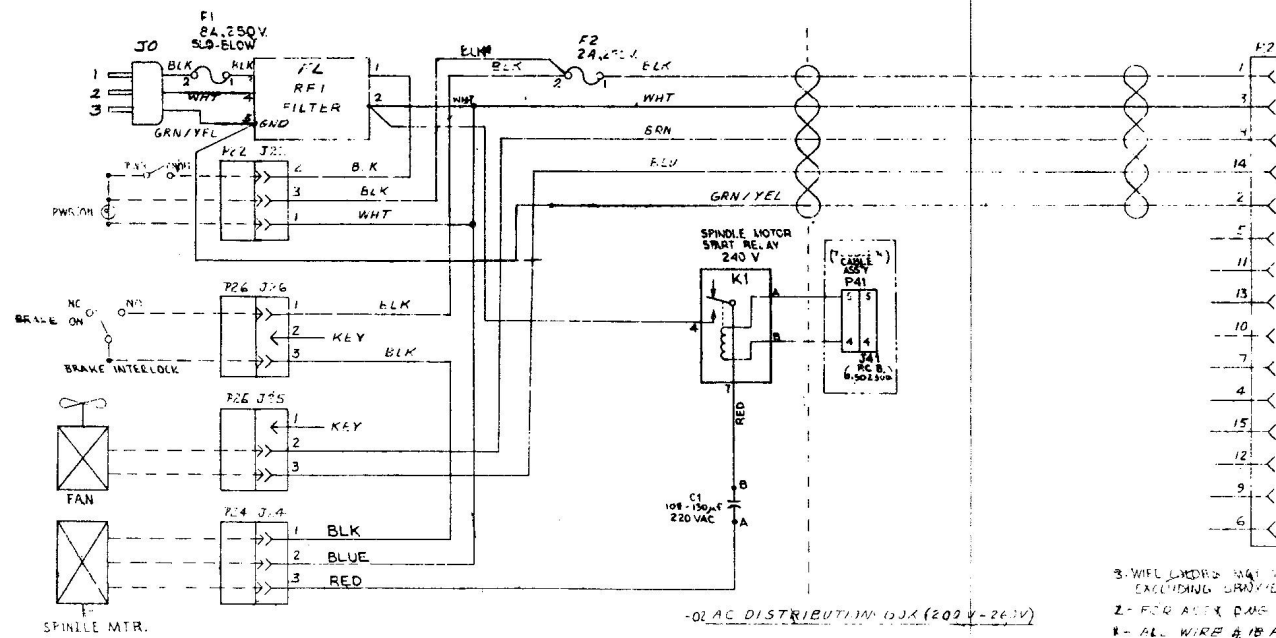
-02 AC DISTRIBUTION BOX (200V - 260V)

JO

F1 8A 250V SLO-BLOW

FL RFI FILTER

GND

F2 2A 250V

BLK
WHT
BRN
BLU
GRN/YEL

P27

PWR ON/OFF

P22 J22
BLK
BLK
WHT

BRAKE ON NC NO

P26 J26
BLK
KEY
BLK

BRAKE INTERLOCK

FAN

P25 J25
KEY

SPINDLE MOTOR START RELAY 240V

K1

CABLE ASSY P41

J41 PCB

SPINDLE MTR.

P24 J24
BLK
BLUE
RED

RED

C1 108-130µF 220 VAC

TABLE B

PRIMARY VAC LINE	P27 PIN CONNECTIONS		
200	5-9	12-7	11-10
220	5-6	12-4	11-10
240	5-9	15-7	11-13
260	5-6	15-4	11-13
200	5, 6	12, 4	11, 10
220	5, 9	12, 7	11, 10
240	5, 6	15, 4	11, 13
260	5, 9	15, 7	11, 13
210	5, 6	12, 4	11, 10
220	5, 9	12, 7	11, 10
230	5, 6	15, 4	11, 13
240	5, 9	15, 7	11, 13

POWER SUPPLY ASSY

30334 , REV 'A' & 'B'

70008102 , REV 'C' TO CURRENT

70008101 , REV 'C' TO CURRENT

3. WIRE CROSS MAY OR MAY NOT BE AS INDICATED EXCLUDING GRN/YEL GND WIRES
2. FOR ASSY DWG SEE 70008400.
1. ALL WIRE #18 AWG TYPE 101

NOTES: UNLESS OTHERWISE SPECIFIED

OSMP, INC.

SCHEMATIC
A.C. DISTRIBUTION
(ELECTRONICS)

708009006

D

J27

WH 8
WH 7
BLU 6
BLU 5
WH 4
WH 3
BLU 2
BLU 1
T2

P15

2-#18W AC +   2-#18 ORN
C5 1µf 100V   CR1 MDA 990-2   C4 20000µf 40V   R4 1K 5W   ORN #18   5 +32V
                                                                          6
                              C3 20000µf 40V   R3 1K 5W   GRY #18   1 MOTOR RET
                                                                          2
2-#18W AC -   2-#18 PUR   PUR #18   4 -32V
                                          3
2-#18 GRY

WH 8
WH 7
BLU 6
BLU 5
WH 4
WH 3
BLU 2
BLU 1
T1

2-#18W AC +   2-#18 YEL
C6 1µf 100V   CR2 MDA 990-2   C2 15000µf 15V   R2 500Ω 3W   YEL #18   9 +10V
                                                                          10
                              C1 15000µf 15V   R1 500Ω 3W   BLK #18   7 DC GND
                                                                          8
2-#18W AC -   2-#18 BLU   BLU #18   12 -10V
                                          11
2-#18 BLK

BLU #18
WH #18
Y/GRN #18

70008101		
PIN	VOLT	PIN
1 —	0V	— 5
2 —	5V	— 6
3 —	110V	— 7
4 —	120V	— 8

70008102		
PIN	VOLT	PIN
1 —	0V	— 5
2 —	10V	— 6
3 —	110V	— 7
4 —	130	— 8
T1	AND	T2

NOTES- UNLESS OTHERWISE SPECIFIED.
1) USE SLEEVING ON ALL PRIMARY & SECONDARY TRANSFORMER SOLDER LUGS.
2) USE TYPE 1015 WIRE FOR ALL PRIMARY WIRING.
3) USE TYPE 1061 WIRE FOR ALL SECONDARY WIRING.
4) SEE 70008lxx FOR ASSY.
5) WIRE COLOR MAY BE OTHER THAN INDICATED, EXCEPT YEL/GRN GND WIRE.

OSMP, INC.

SCHEMATIC, POWR SUPPLY

DRAWN A.H. 12-7-79
CHECKED

SIZE D   DWG. NO. 70800800   REV H

DO NOT SCALE DRAWING
SHEET 1 OF 1

70800800   H