Model 500

Description:

The state-of-the-art Model 500 Single Board Computer is fully compatible with the Ohio Scientific 48-pin bus and all Ohio Scientific Accessory Boards. The Model 500 is based on the 6502 microprocessor by MOS Technology. This chip is second sourced by Synertek and third sourced by Rockwell International. The Model 500 accepts 8 2K X 8 2616 Mask programmed ROMs (normally containing our 8K BASIC by Microsoft). 2704s, 2708s, 2716s, or similar parts can be used instead of the ROMs if the user has a custom application using his own software. Space is also provided for 4K of 2102-type RAM, an ACIA based serial interface which can be populated for RS-232 or 20ma current loop. Options include a PIA based parallel I/O port, 256K Memory Management (allows the system to address up to 256K memory), and up to three 1702-type PROMs.

Applications:

The 500 CPU Board can be used as a powerful small system. It is especially powerful because if has "instant 8K BASIC" and because of its 4K of on-board RAM memory. It can also be used as the basis of a larger Challenger type system. It is capable of supporting additional memory, our 430B Audio Cassette Interface, our 440B Video Graphics Board, our Floppy Disk Drive, and all other peripheral devices offered by Ohio Scientific. If a person already has an Ohio Scientific system, the 500 Board can be used to store 8K BASIC in ROM and as a 4K RAM board.

Specifications:

Mechanical: 8" X 10" G-10 Double-Sided Plated Through Hole Board

Electrical: +5 Volts at 2 Amps
-9 Volts at 500ma

Processors: Supports the 6502 or 6502A. Can be used as the controller for the 560Z which offers Z-80 and 6100.

PROM: Supports three 1702-type PROMs. Ohio Scientific offers 65A Serial PROM Monitor, 65V Video PROM Monitor, and Floppy Disk Bootstrap PROMs.

RAM: Can support up to 4K X 8 2102 type RAM

Firmware: 8K BASIC in ROM (User can supply own software in ROM)

Serial I/O: Serial Interface can be configured for RS-232 or 20ma. loop. 5 possible baud rates are jumper selectable.

Other Features: Buffering to drive up to 250 Ohio Scientific System Boards.
Memory Management for up to 256K Bytes of Memory.
PIA based parallel port also available.

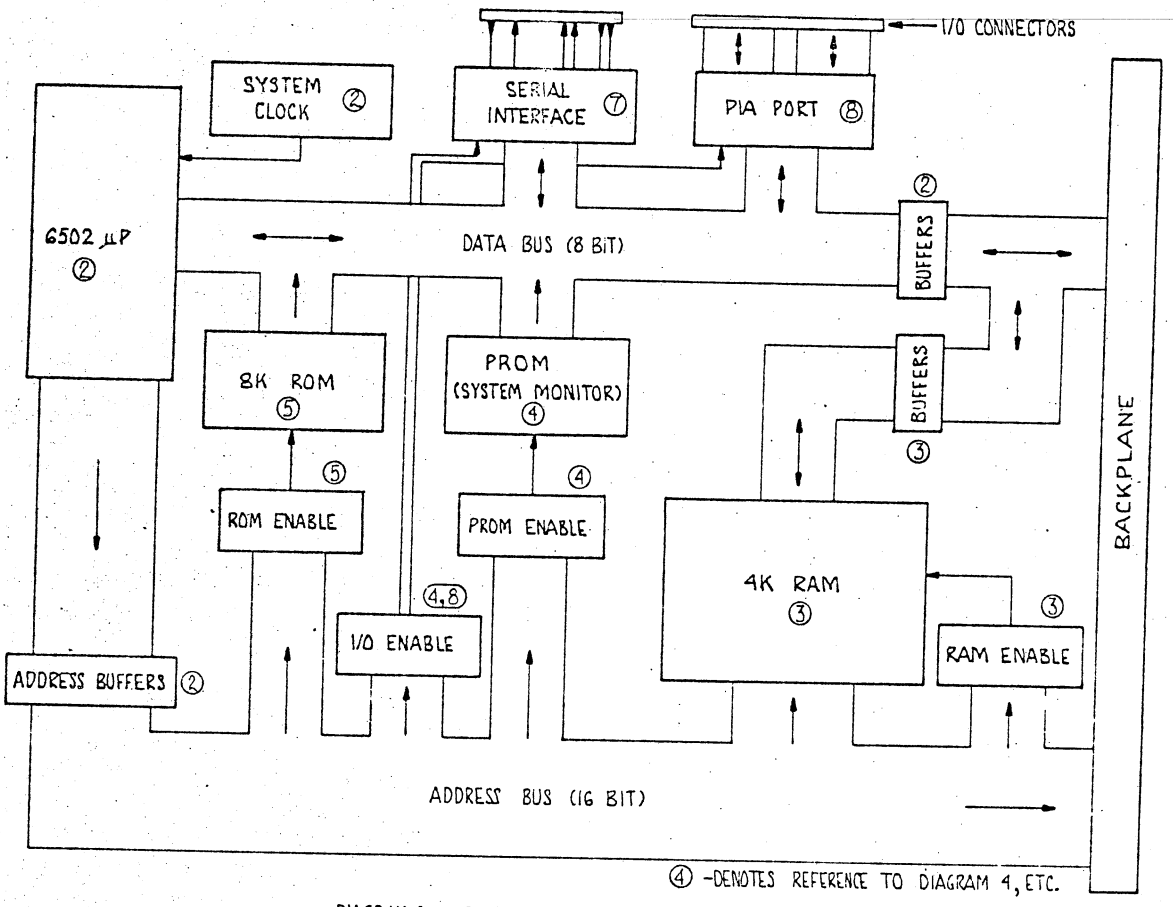


DIAGRAM 1 - SYSTEM OVERVIEW

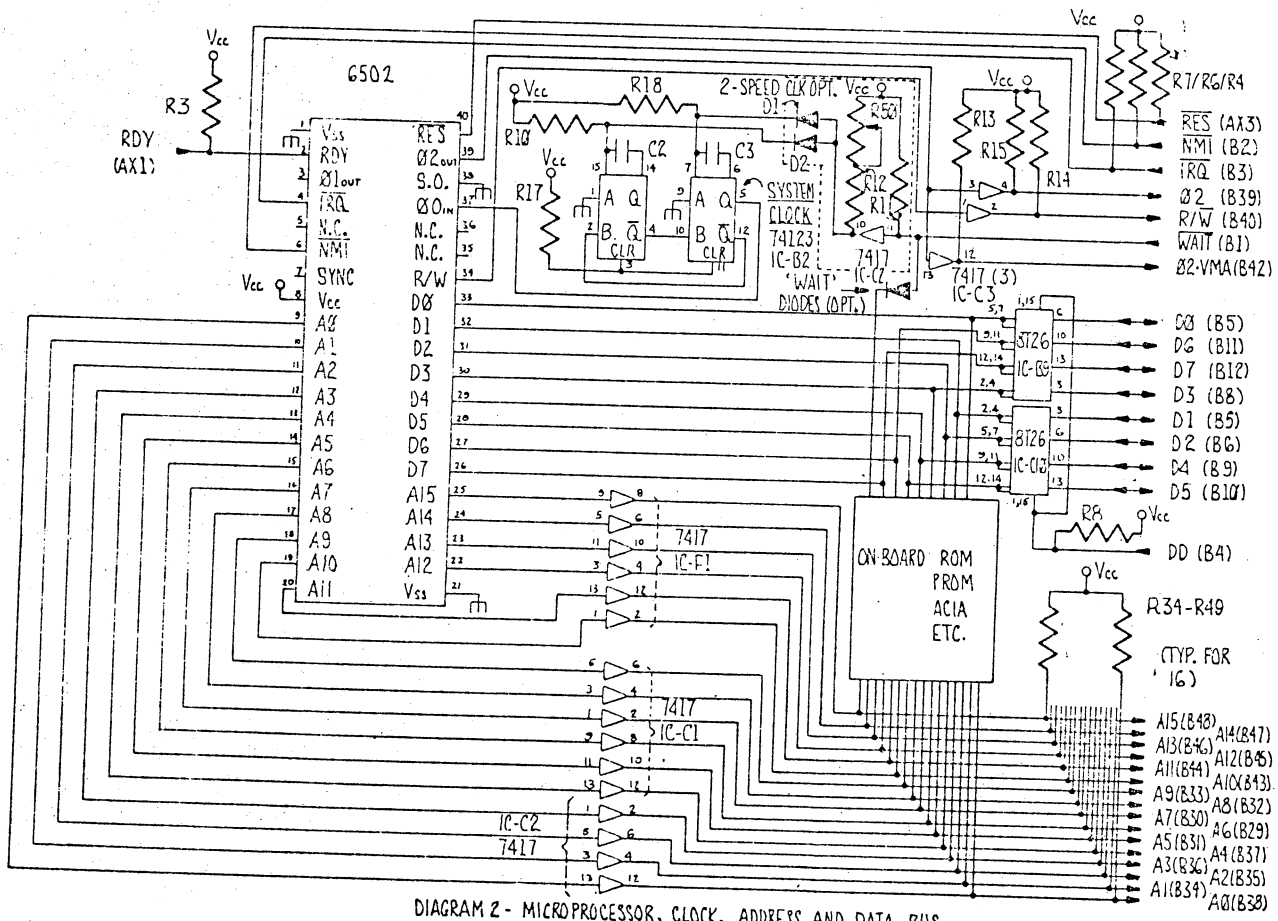


DIAGRAM 2 - MICROPROCESSOR, CLOCK, ADDRESS AND DATA BUS

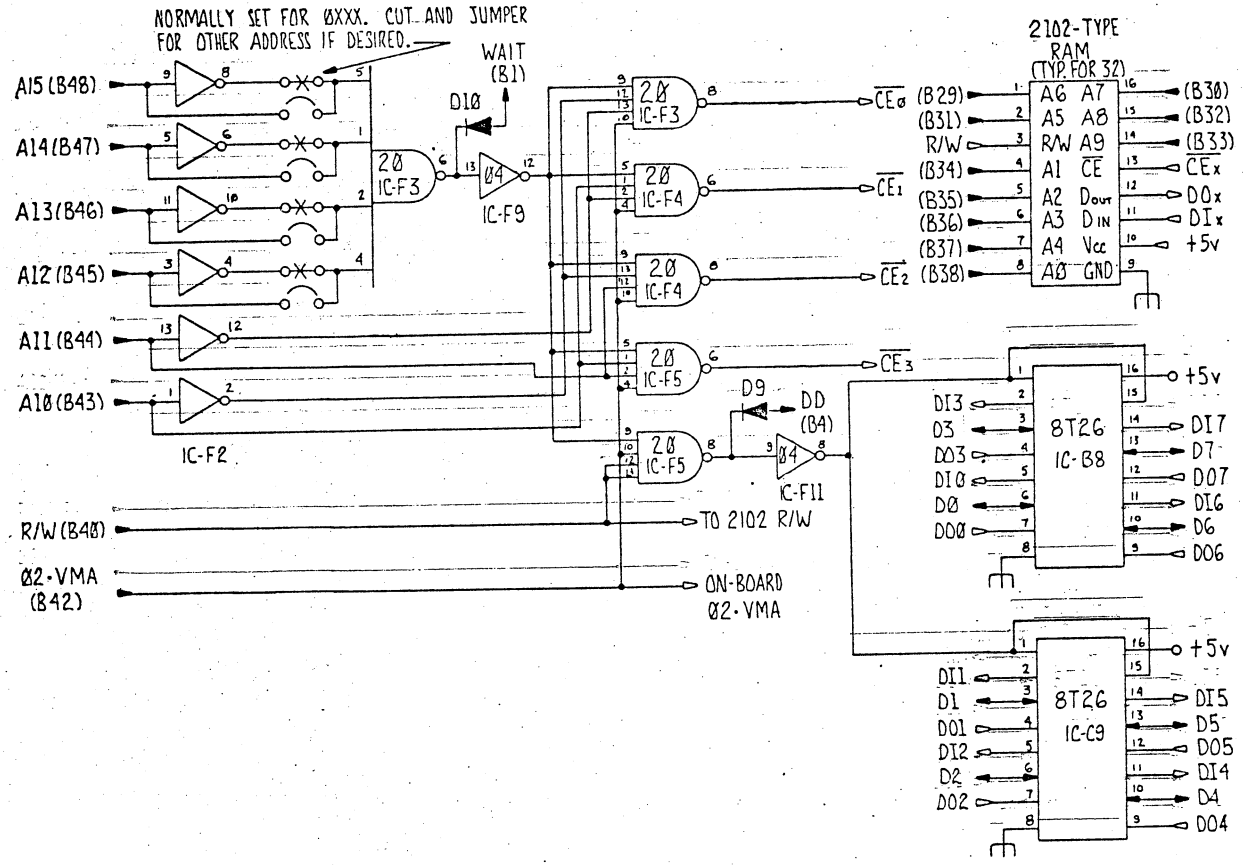


DIAGRAM 3- RAM IMPLEMENTATION

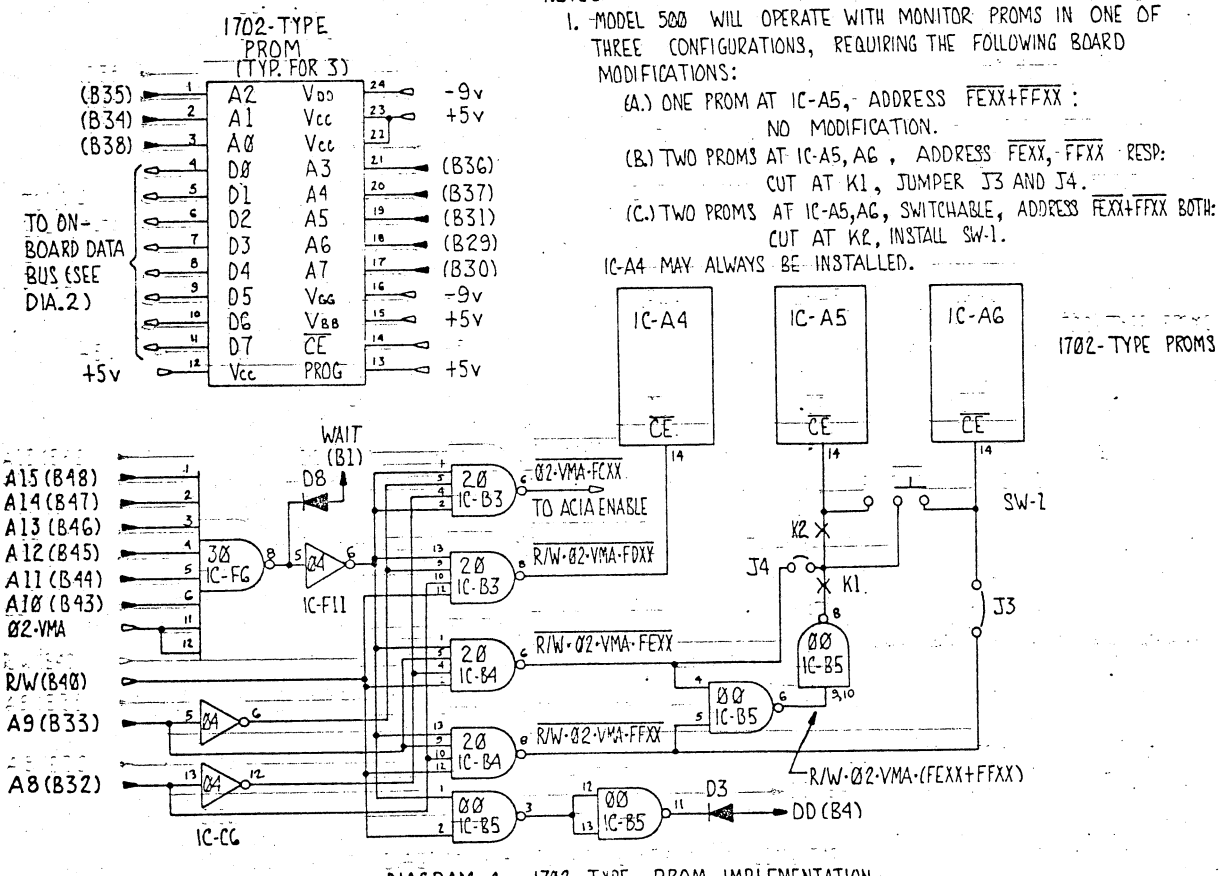
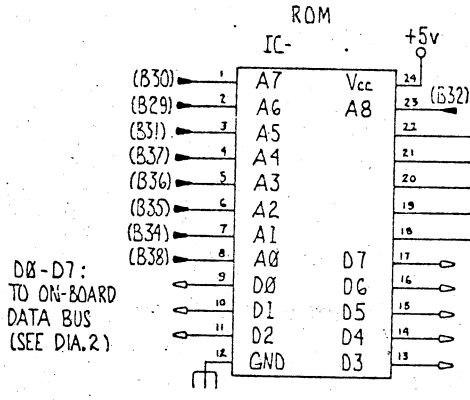


DIAGRAM 4- 1702-TYPE PROM IMPLEMENTATION



SYNERTEK SY2316B	INTEL 2704	INTEL 2708	INTEL 2716	TI 2716	INTEL 2316E
A9	GND	A9	A9	A9	A9
P	-5v	-5v	+5v	-5v	P
CEX	$\overline{CEX}$	$\overline{CEX}$	$\overline{CEX}$	A10	$\overline{CEX}$
A10	+12v	+12v	A10	+12v	A10
P	GND	GND	GND	$\overline{CEX}$	P

NOTES:

1. P = CONNECTION TO +5v. (PULLUP)
2. BOARD NORMALLY SET FOR SY2316B. SEE DIA. 6 FOR MODIFICATIONS FOR OTHER CHIPS.

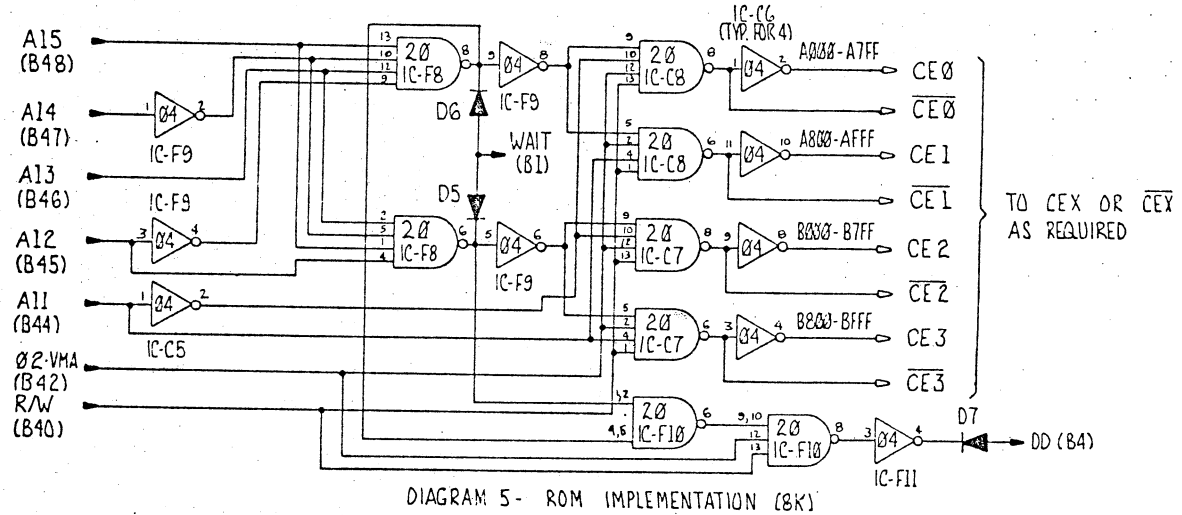
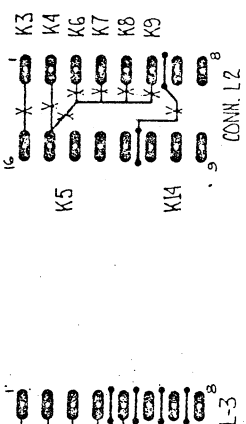


DIAGRAM 5- ROM IMPLEMENTATION (8K)

SYNERTEK SY2316B	INTEL 2704	INTEL 2708	INTEL 2716	TI 2716	INTEL 2316E
CUT	CUT	CUT	CUT	CUT	CUT
NONE REQ'D.	K-3 K-4 K-5 K-10 K-11 K-12 K-13 K-14	K-3 K-4 K-5 K-10 K-11 K-12 K-13	K-5 K-10 K-11 K-12 K-13	K-3 K-4 K-6 K-7 K-8 K-9 K-10 K-11 K-12 K-13	K-10 K-11 K-12 K-13
JUMPER	JUMPER	JUMPER	JUMPER	JUMPER	JUMPER
NONE REQ'D.	L2 p.7-p.6 p.8-p.1 p.9-p.2 L3 p.8-p.7 p.9-p.4 p.10-p.3 p.11-p.2 p.12-p.1	L2 p.7-p.6 p.8-p.1 p.9-p.2 L3 p.9-p.4 p.10-p.3 p.11-p.2 p.12-p.1	L2 p.7-p.6 L3 p.5-p.1 p.5-p.2 p.5-p.4	L2 p.8-p.1 p.9-p.2 p.11-p.6 p.12-p.5 p.13-p.4 p.14-p.3 L3 p.5-p.1 p.5-p.2 p.5-p.3 p.5-p.4	L3 p.9-p.4 p.10-p.3 p.11-p.2 p.12-p.1

NOTE: L3 p.9-p.4 means jumper pin 9 to pin 4 of connector L3, etc.



(ABOVE) CONNECTORS L2 AND L3 SHOWING CUT POINTS. VIEW FROM REAR OF BOARD.

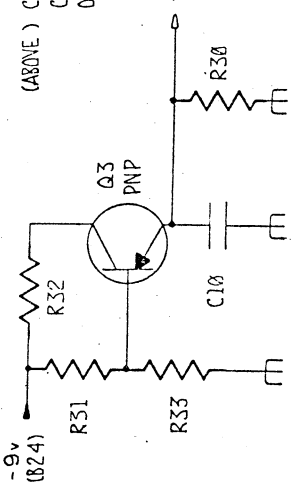


DIAGRAM 6- ROM JUMPER CONFIGURATION AND -5v POWER

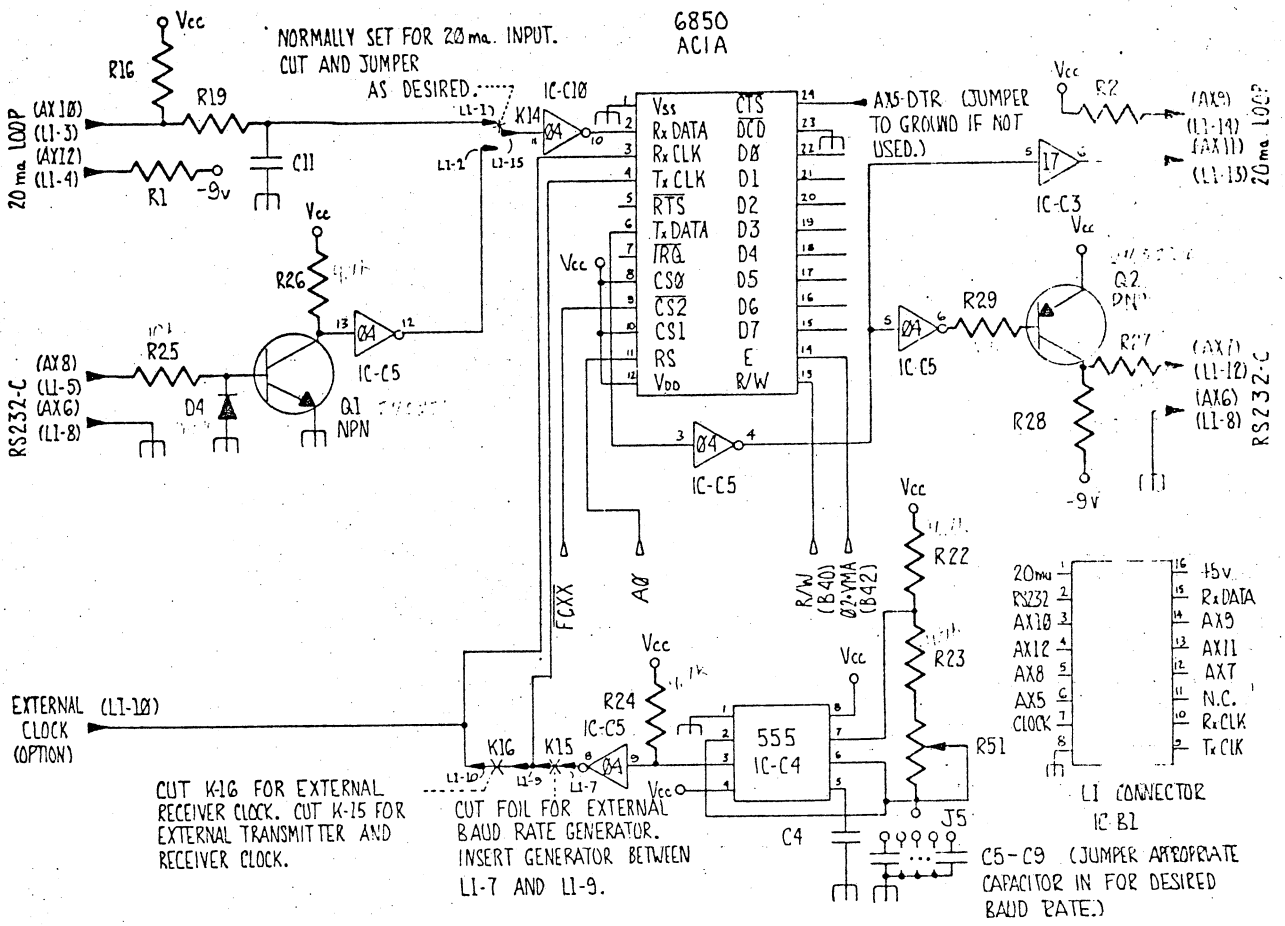
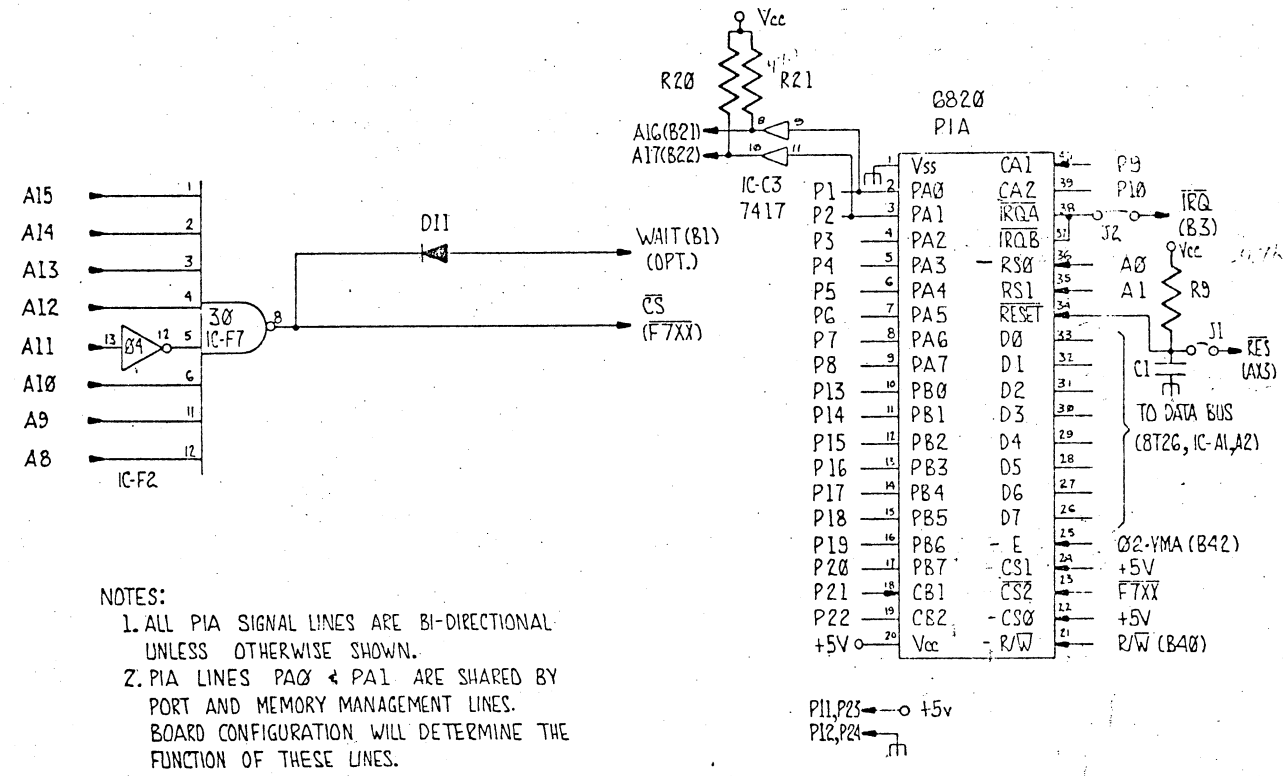


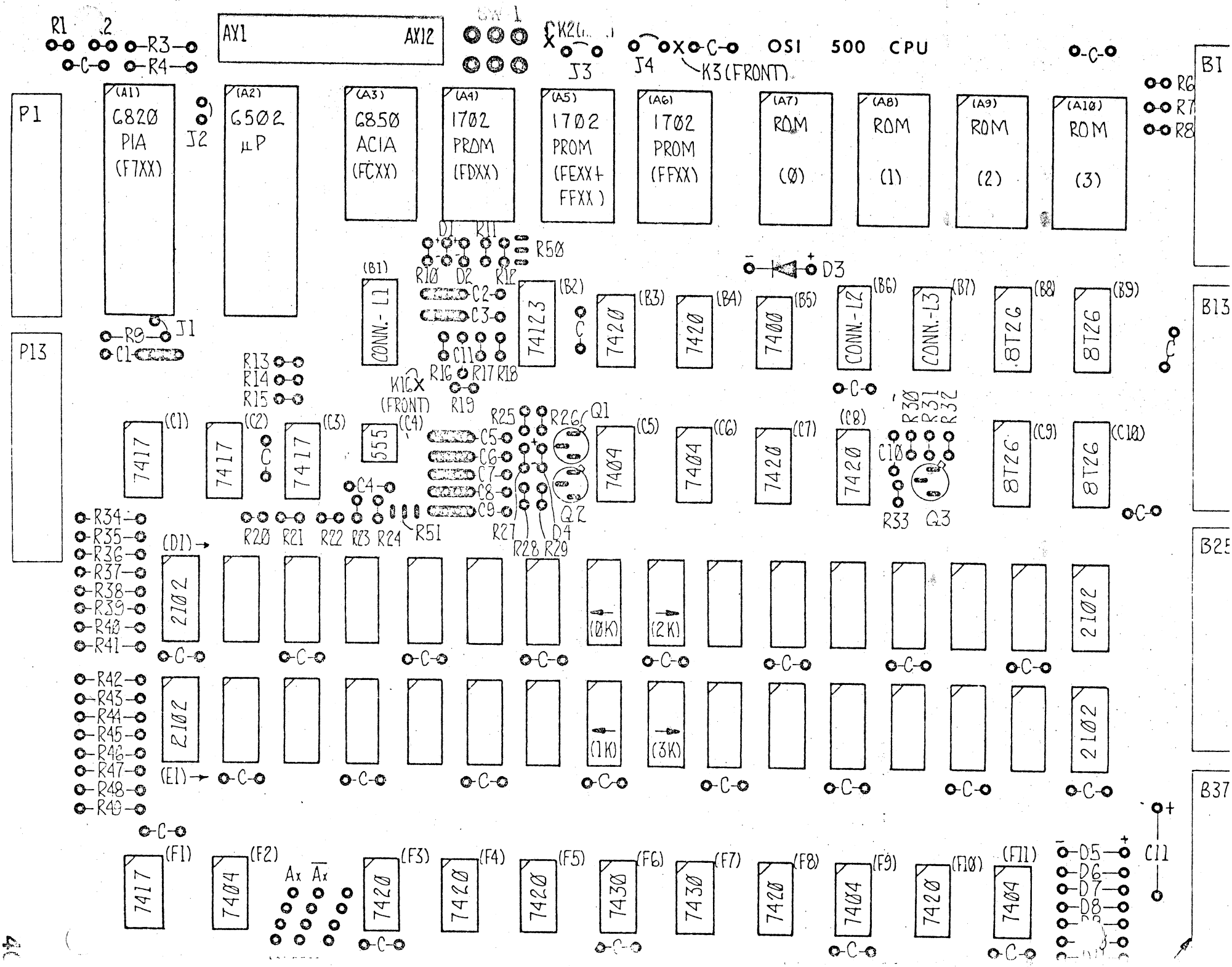
DIAGRAM 7- SERIAL INTERFACE

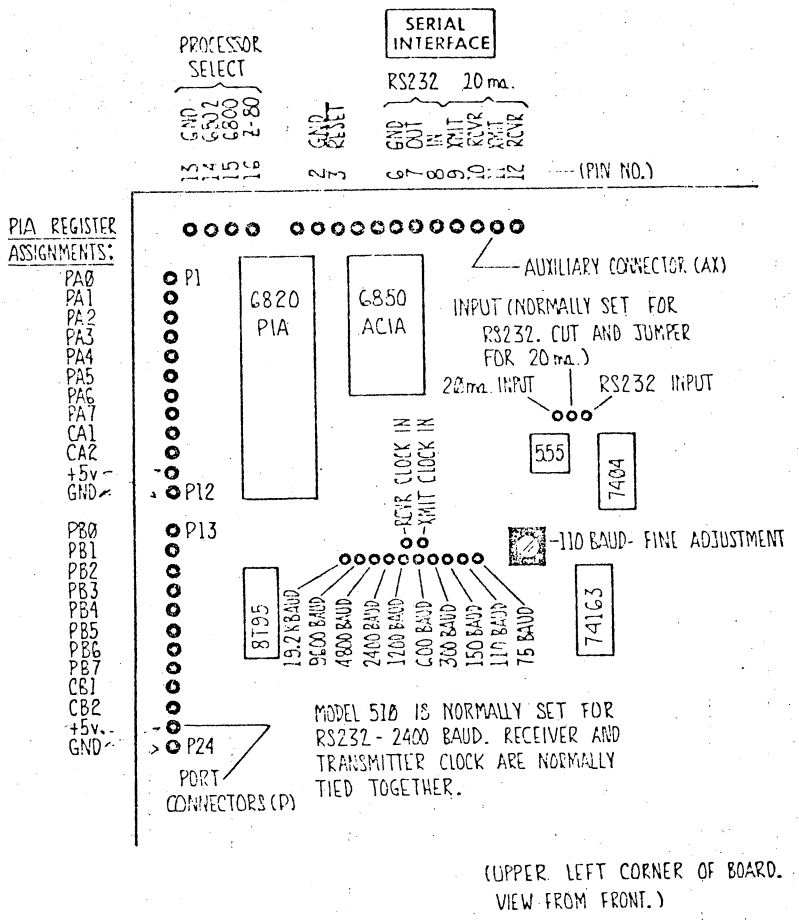


NOTES:

1. ALL PIA SIGNAL LINES ARE BI-DIRECTIONAL UNLESS OTHERWISE SHOWN.
2. PIA LINES PA0 & PA1 ARE SHARED BY PORT AND MEMORY MANAGEMENT LINES. BOARD CONFIGURATION WILL DETERMINE THE FUNCTION OF THESE LINES.

DIAGRAM 8- PIA PORT


OSI 500 CPU
AX1
AX12
P1
P13
J1
J2
J3
J4
K3 (FRONT)
K1 (FRONT)
(A1) 6820 PIA (F7XX)
(A2) 6502 µP
(A3) 6850 ACIA (FCXX)
(A4) 1702 PROM (FDXX)
(A5) 1702 PROM (FEXX + FFXX)
(A6) 1702 PROM (FFXX)
(A7) ROM (0)
(A8) ROM (1)
(A9) ROM (2)
(A10) ROM (3)
(B1) CONN.-L1
(B2) 74123
(B3) 7420
(B4) 7420
(B5) 7400
(B6) CONN.-L2
(B7) CONN.-L3
(B8) 8T26
(B9) 8T26
(C1) 7417
(C2) 7417
(C3) 7417
(C4) 555
(C5) 7404
(C6) 7404
(C7) 7420
(C8) 7420
(C9) 8T26
(C10) 8T26
(D1) 2102
(E1) 2102
(F1) 7417
(F2) 7404
(F3) 7420
(F4) 7420
(F5) 7420
(F6) 7430
(F7) 7430
(F8) 7420
(F9) 7404
(F10) 7420
(F11) 7404
(0K)
(1K)
(2K)
(3K)
Ax Āx
D1 D2 D3 D4 D5 D6 D7 D8
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11
R0 R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51
Q1 Q2 Q3
B1 B13 B25 B37



(UPPER LEFT CORNER OF BOARD. VIEW FROM FRONT.)

MODEL 510 I/O CONNECTIONS

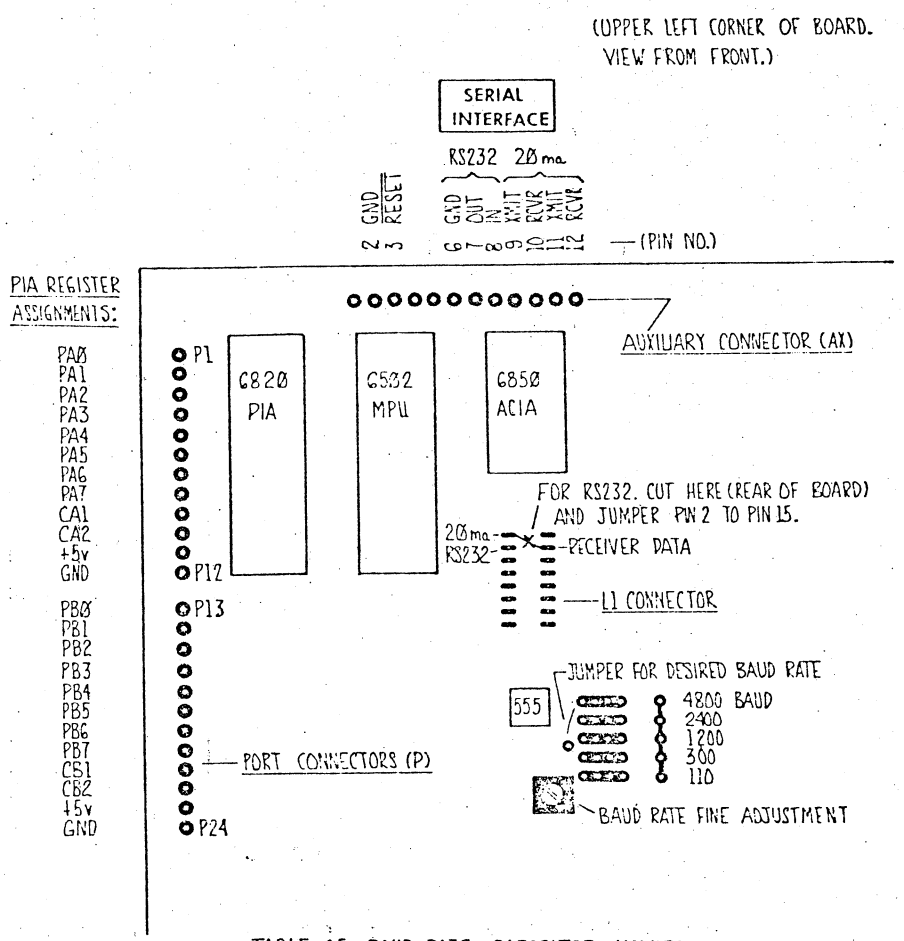


TABLE OF BAUD RATE CAPACITOR VALUES

	MIN	MID-RANGE	MAX
4800 BAUD	.001 µf	.002 µf	.0027 µf
2400	.0022	.0033	.0056
1200	.0045	.0068	.0110
300	.0179	.027	.0446
110	.0489	.082	.1216

MID-RANGE CAPACITANCE VALUES ARE RECOMMENDED, HOWEVER ANY VALUE BETWEEN MIN AND MAX MAY BE SUBSTITUTED. ALL VALUES ARE IN µf.

MODEL 500 I/O CONNECTIONS

510 CPU Board

Description:

The Model 510 CPU Board is the most technically advanced CPU Board available today for small computers. It is always supplied with three processors; 6502A, 6800, and Z-80. One processor is run at a time; an optional software switch is available to permit the user to change processors under software control. When the user switches processors, memory contents are preserved. The board can also be provided with "megabyte memory pager" allowing up to 1 megabyte of memory to be addressed. The CPU board can be configured to handle up to 16 users on a single system. Other features of the board include a serial interface with crystal controlled baud rate generator capable of operating from 110 to 19,200 baud. Up to three PROM Monitors can be provided for the 6502 and one for the 6800. The 510 Board is automatically configured for disk use.

Applications:

The Model 510 allows the user to have three processors for about $200 more than one processor. This is ideal for industrial development applications where an engineer wishes to compare three different processors. It is also ideal for small business systems as it allows up to 16 users. The three processors insure the businessman that his machine won't become obsolete when a new software package comes along--simply because he chose the wrong processor. These same reasons make the 510 ideal for educational as well as home use. Since the 510 is fully compatible with all of Ohio Scientific's peripherals (it is also used as the heart of the Challenger III systems), and since it is fully expandable, it is the ideal CPU for almost all applications. It allows the user to have the flexibility of owning three powerful computer systems at slightly over the cost of owning one!

Specifications:

Mechanical: 8" X 10" G-10 Epoxy Double-Sided Plated Through Hole Boards

Electrical: +5V at 2amps
-9V at 500ma

Processors: Comes standard with 6502A, 6800, and Z-80

PROM: Supports up to three 1702 type PROMs for the 6502, and one PROM for the 6800

Serial I/O: One Serial Interface can be configured for RS-232 or 20ma loop. Crystal controlled baud rate can be set from 110 baud to 19,200 baud

Parallel I/O: Offers one PIA based parallel port (optional)

Other Features: Allows one-megabyte memory management
Allows up to 16 users on a system
Comes configured for disk operation
Software Switch Option enables user to change from processor to processor under software control. When processors are changed (even if change is manual) memory is preserved.

OHIO SCIENTIFIC			product name/number 510/C3-8/C3-0	
date 8/77	revision A	page 48	status Production	sheet 1 of 1

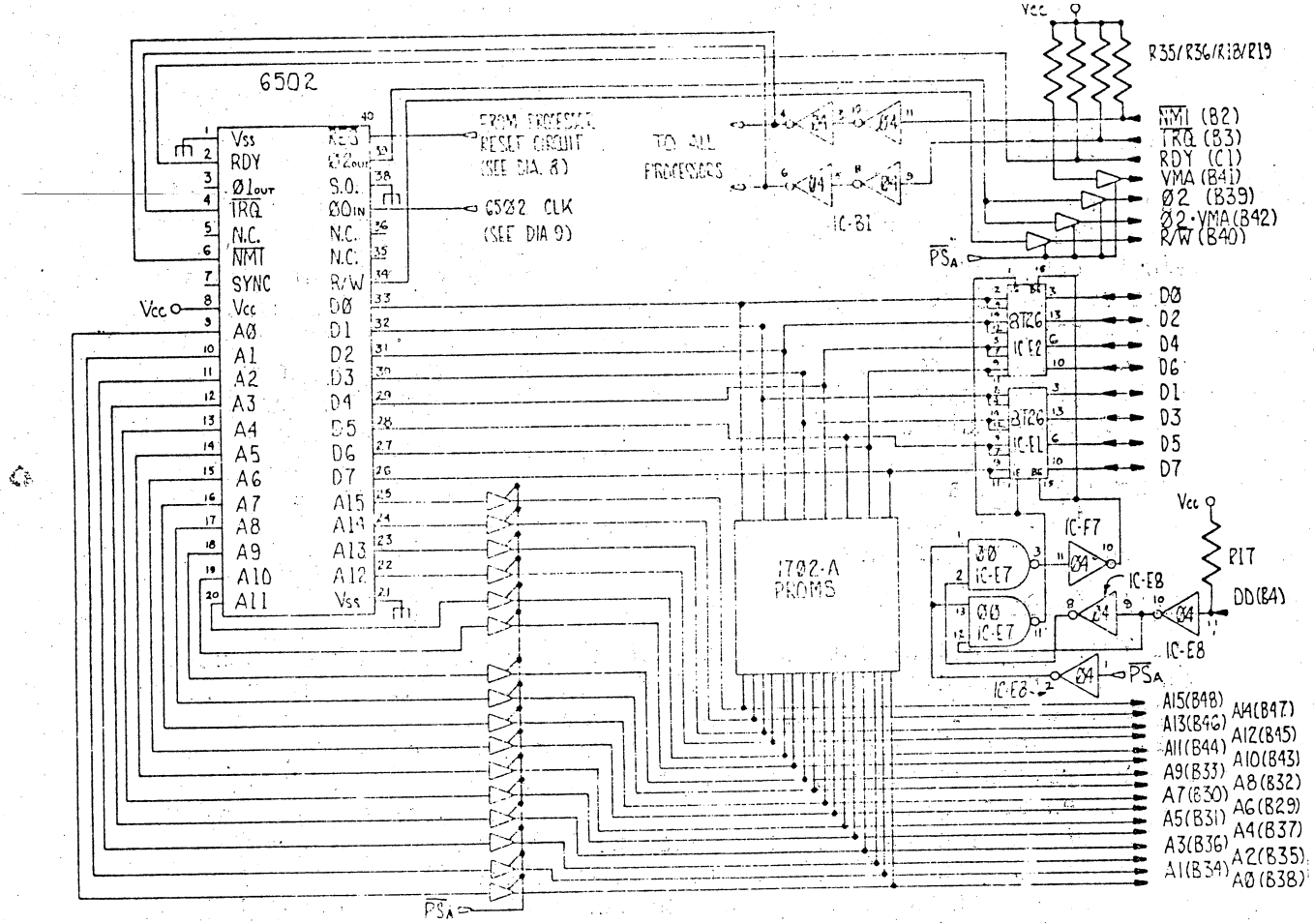


DIAGRAM 2 - 6502 CIRCUITRY

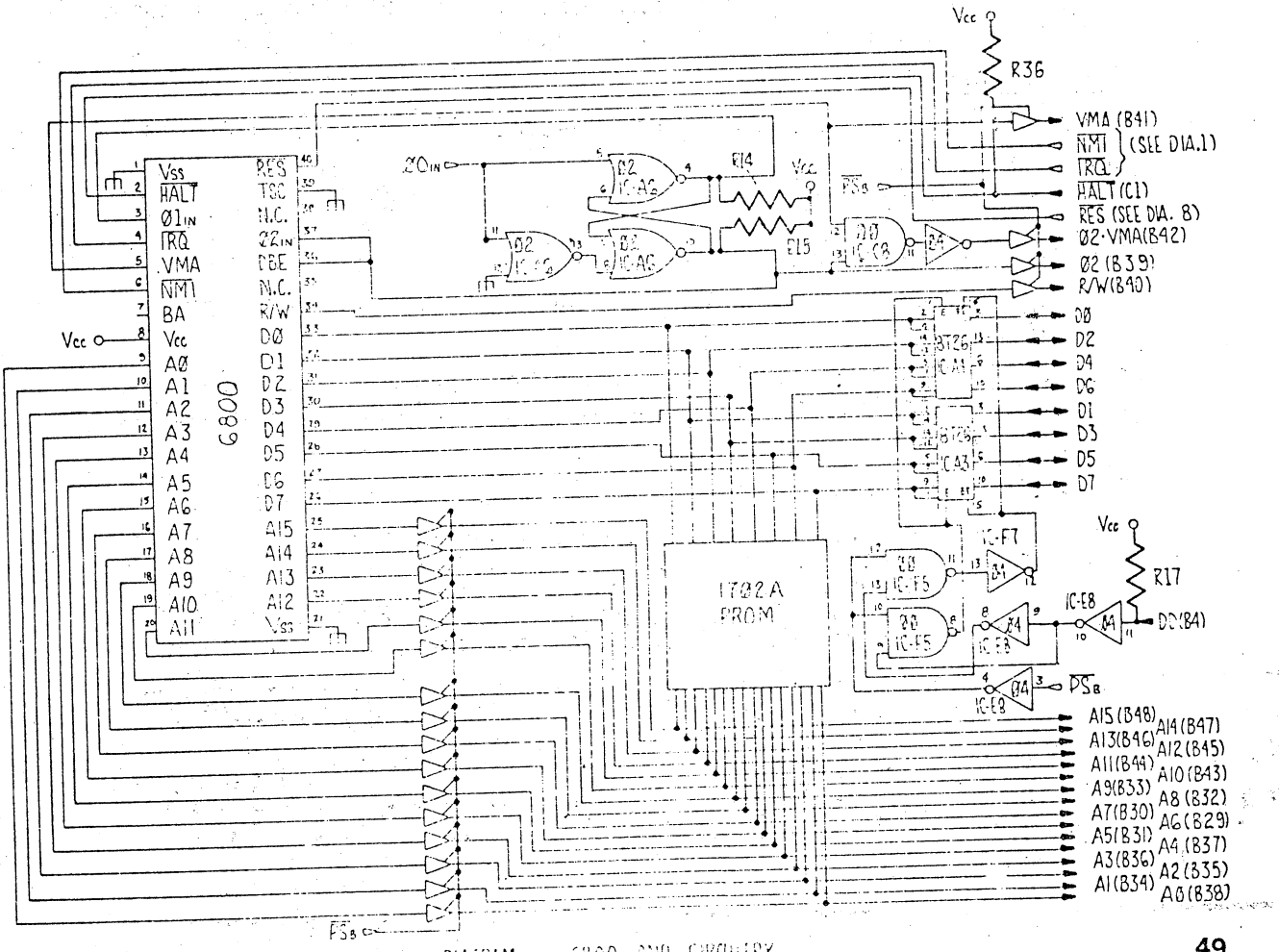


DIAGRAM 3 - 6800 AND CIRCUITRY

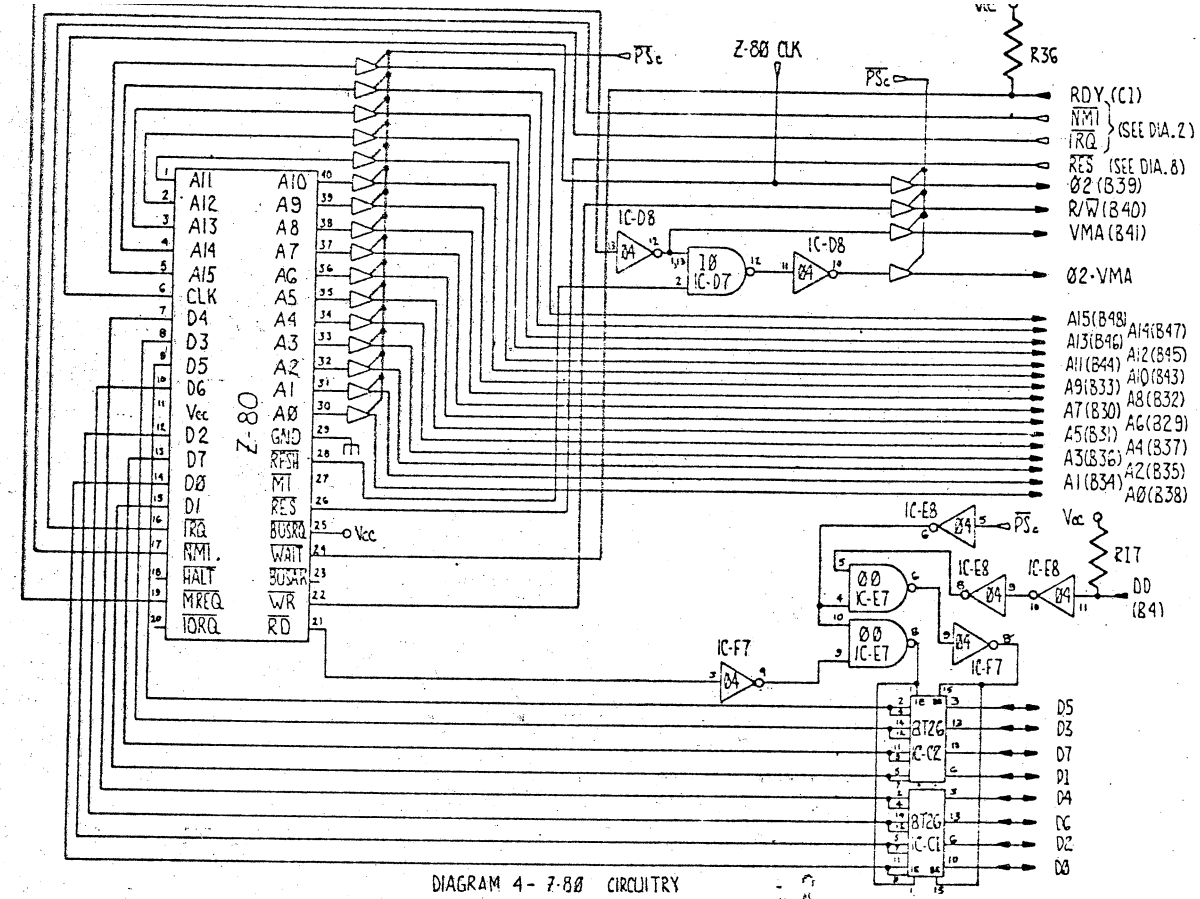
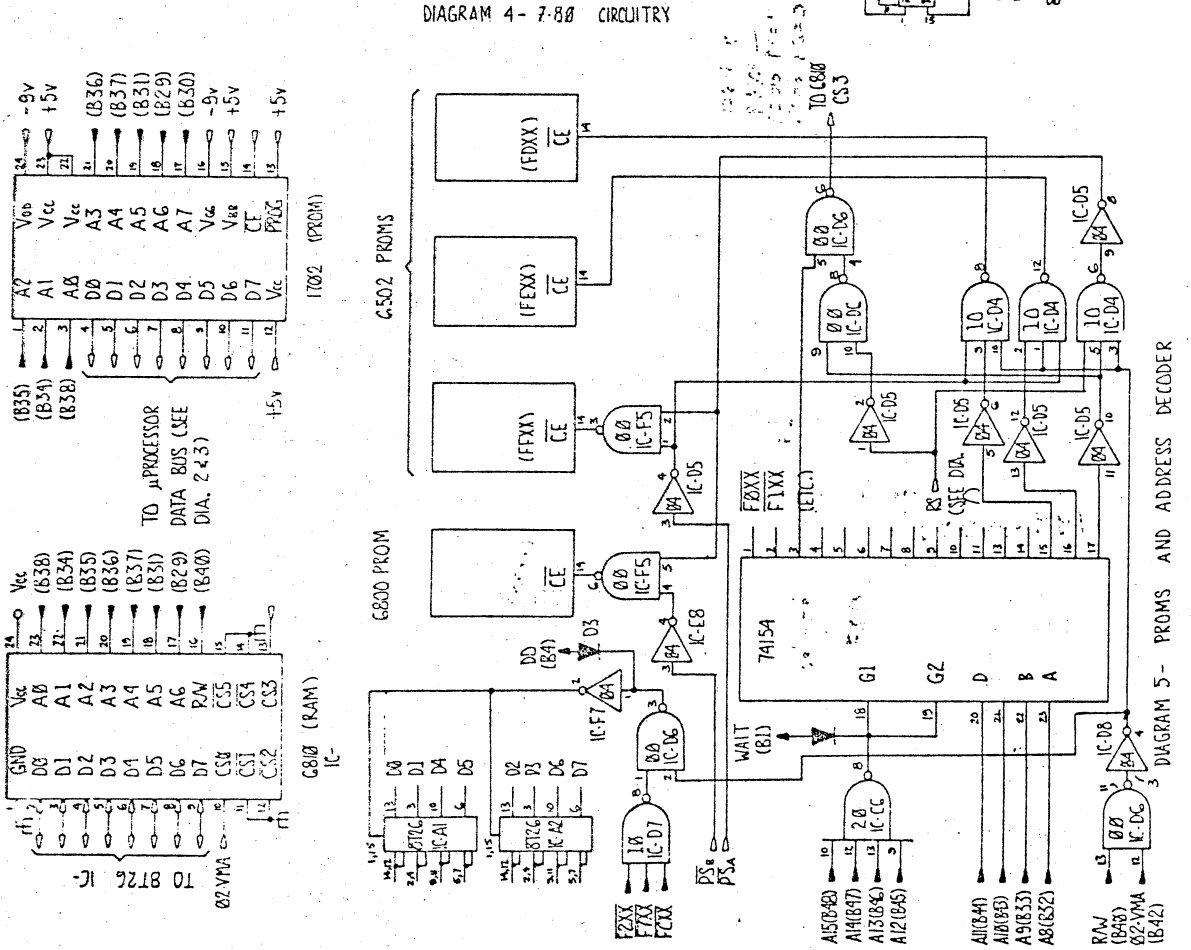


DIAGRAM 4- Z-80 CIRCUITRY



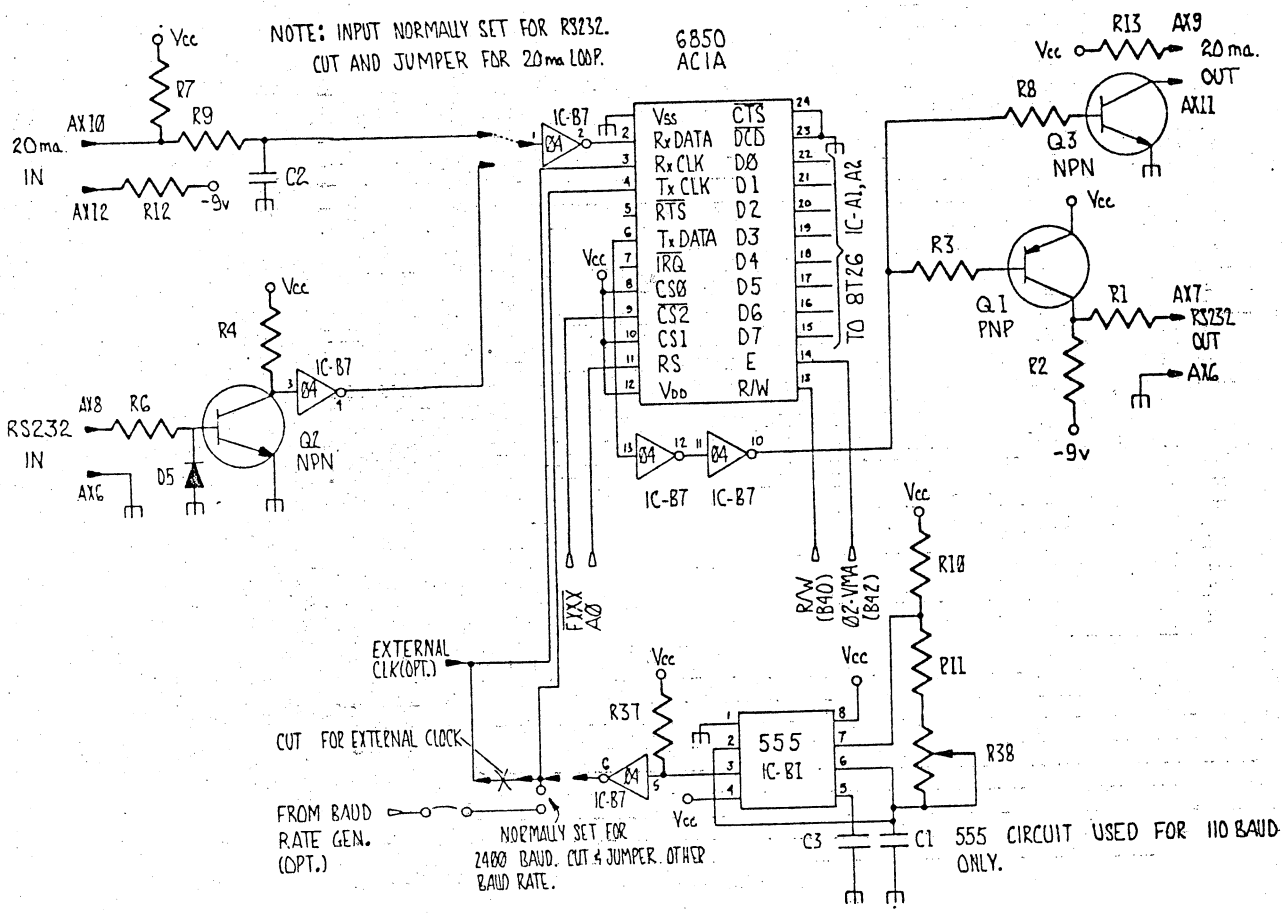
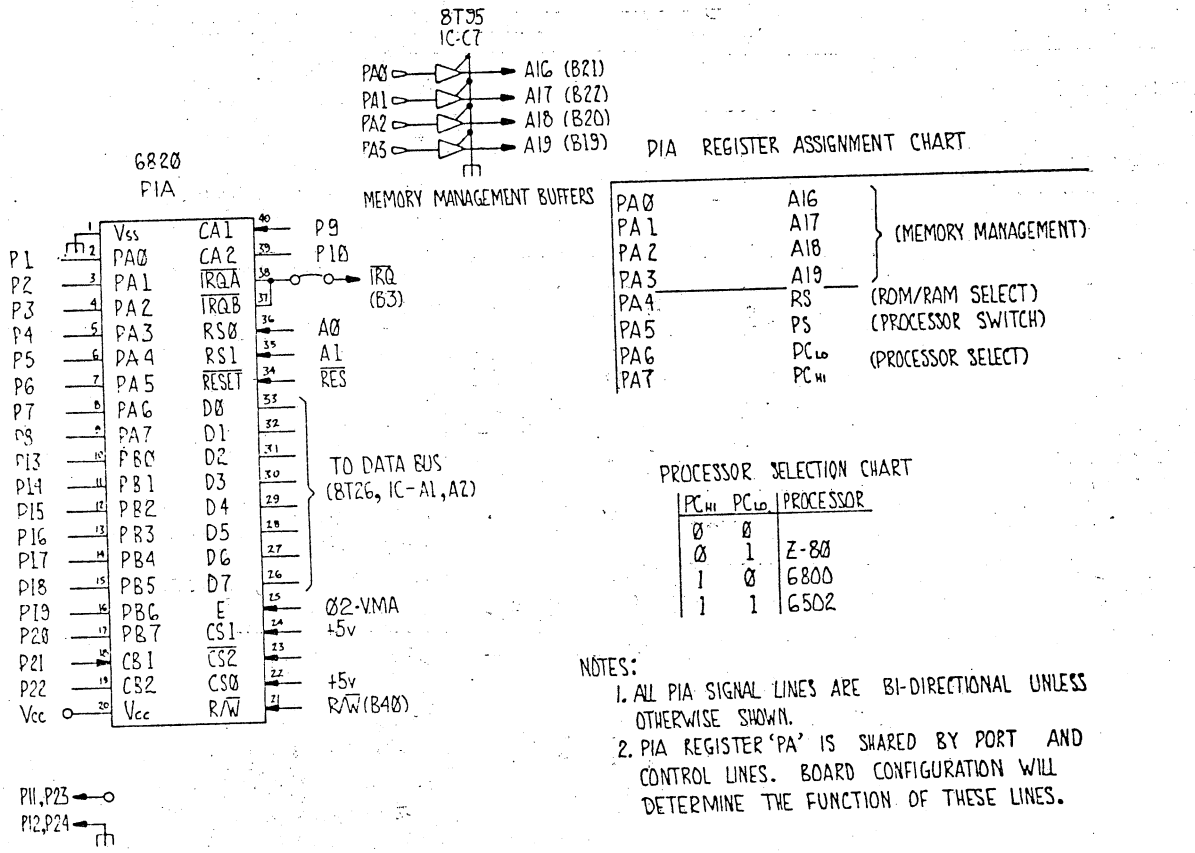


DIAGRAM 6- SERIAL INTERFACE



PIA REGISTER ASSIGNMENT CHART

PA0	A16	(MEMORY MANAGEMENT)
PA1	A17	
PA2	A18	
PA3	A19	
PA4	RS	(ROM/RAM SELECT)
PA5	PS	(PROCESSOR SWITCH)
PA6	PC_{LO}	(PROCESSOR SELECT)
PA7	PC_{HI}	

PROCESSOR SELECTION CHART

PC_{HI}	PC_{LO}	PROCESSOR
0	0	
0	1	Z-80
1	0	6800
1	1	6502

NOTES:

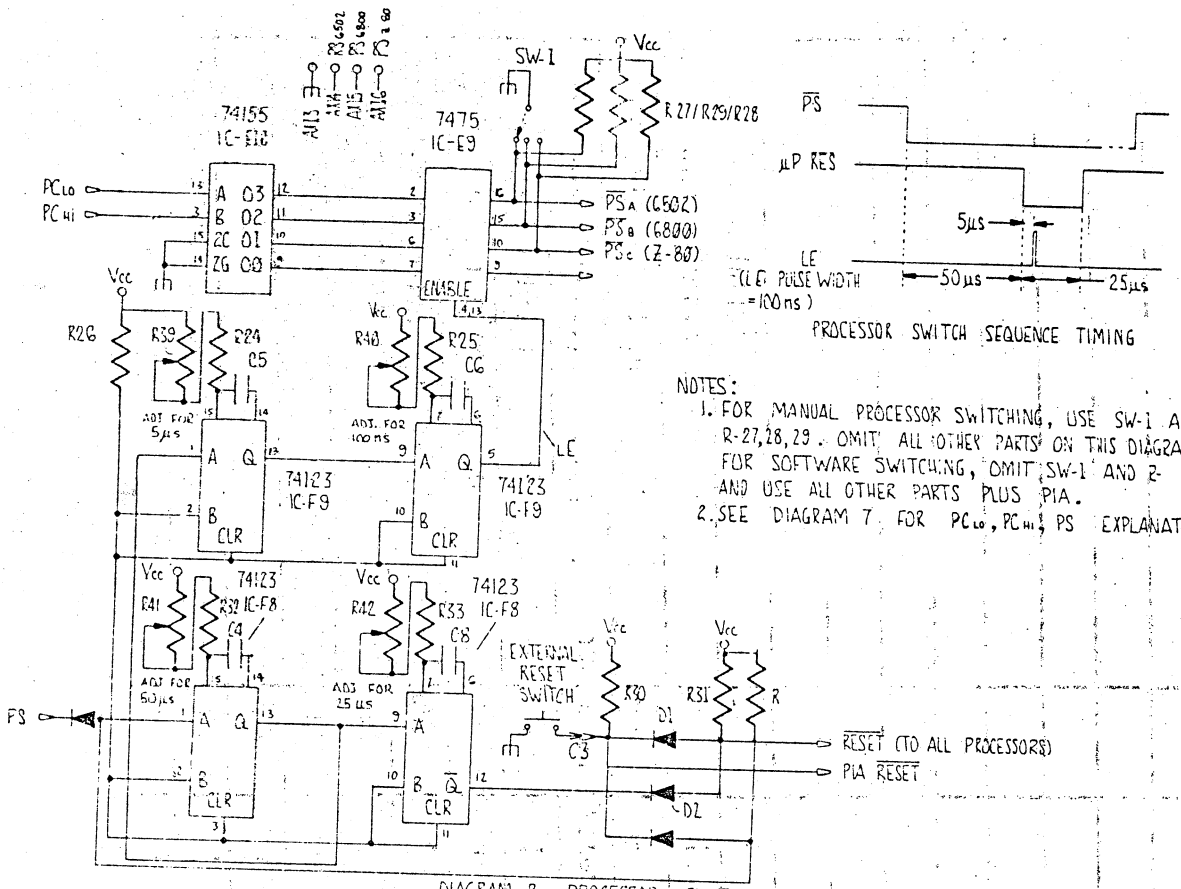
1. ALL PIA SIGNAL LINES ARE BI-DIRECTIONAL UNLESS OTHERWISE SHOWN.
2. PIA REGISTER 'PA' IS SHARED BY PORT AND CONTROL LINES. BOARD CONFIGURATION WILL DETERMINE THE FUNCTION OF THESE LINES.

DIAGRAM 7- PIA IMPLEMENTATION

DISK Challenger III Utilities
DIRECTORY

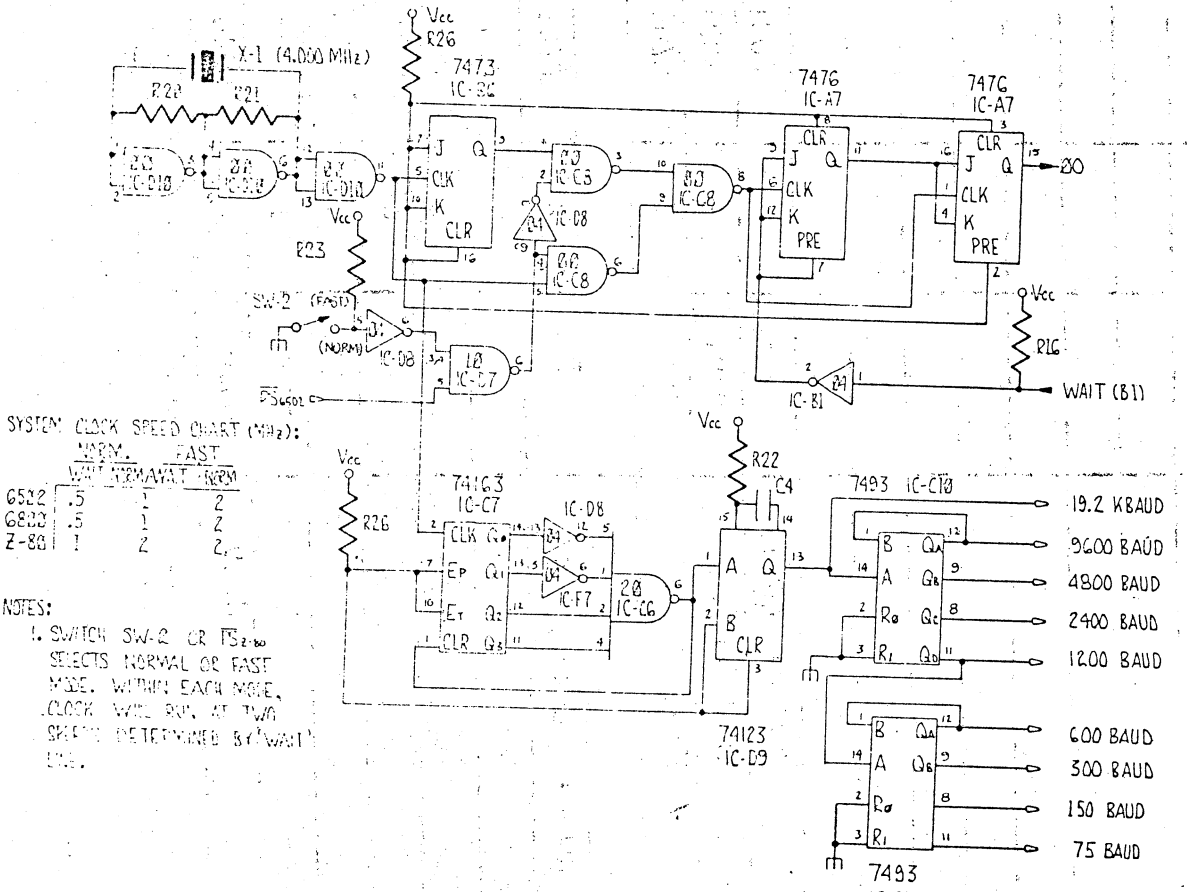
PAGE
DATE

#1 Program	#2 Track	#3 Sector or Format	#4 Start of Transfer	#5 Length in Pages	#6 Go Address	#7 Comments
Modified OS-65 V2.0	00	1	2180	A	2500	6502
Disk Copy	01	1	0200	5	0200	6502
Filler	02	1	----	5	----	
Filler	03	1	----	5	----	
Filler	04	1	----	5	----	
Modified I/O drivers	05	1	2200	3	----	6502
Modified File Controller	06	1	2B30	5	----	6502
Challenger III Utilities	07	1	3D70	3	----	3 processor program
Support utilities outside the operating system						
Challenger III Utilities	08	1	3D70	3	----	Copy of track 7
Mik Bug Simulator	09	1	E000	2	E0D0	6800 program
6800 LOAD/DUMP	10	1	1000	1	----	6800 program



NOTES:
1. FOR MANUAL PROCESSOR SWITCHING, USE SW-1 AND R-27,28,29. OMIT ALL OTHER PARTS ON THIS DIAGRAM. FOR SOFTWARE SWITCHING, OMIT SW-1 AND R- AND USE ALL OTHER PARTS PLUS PIA.
2. SEE DIAGRAM 7 FOR PCLo, PCHi, PS EXPLANATION.

DIAGRAM 8- PROCESSOR SWITCHING CIRCUITRY



SYSTEM CLOCK SPEED CHART (MHz):

	NORM. WAIT	NORM.	FAST WAIT	FAST NORM
6502	.5	1		2
6800	.5	1		2
Z-80	1	2		4

NOTES:
1. SWITCH SW-2 OR PS2-80 SELECTS NORMAL OR FAST MODE. WITHIN EACH MODE, CLOCK WILL RUN AT TWO SPEEDS DETERMINED BY WAIT LINE.

DIAGRAM 9- SYSTEM CLOCK AND BAUD RATE GENERATOR

Model 520
16K Static RAM

Description:

Model 520 16K RAM Board uses 4K x 8 EMM 4200 static RAM memories. These memories are ultra-low power, power-strobe chips. That is, they only draw appreciable amounts of power when they are being accessed. The Model 520 Memory Board requires power for both 12 Volt, 5 Volt, and -9 Volt supplies so that it cannot be used in 500-1 and Challenger IIP. The Model 520 Memory Board typically operates at a maximum of 1.5MHz with the 6502A or 6800 or approximately 3MHz with the Z-80.

Applications:

Main memory in medium to large scale computer systems (32 to 48K or more memory).

Specifications:

Available only as fully assembled, fully burned in memory board configured for 16K x 8 address strapable for any 16K partition within a 256K memory space. (18 address bits).

Electrical: Depend on access rate of the memory board but can be considered negligible in a stand-by condition.

Model 525
16K Dual Port RAM

Description:

The Model 525 16K Dual Port RAM Board utilizes 4K, 8K, or 16K of the popular 2114 static RAMs. The Model 525 can be configured for single or dual port operation. The second memory port allows memory transfers without processor paralyzing DMA.

Applications:

This board is a must in systems using the new 74 Megabyte disk, but, also has important applications in shared memory, multiprocessing, and high resolution video graphics where it is desirable to do memory transfers without interfering with processor performance.

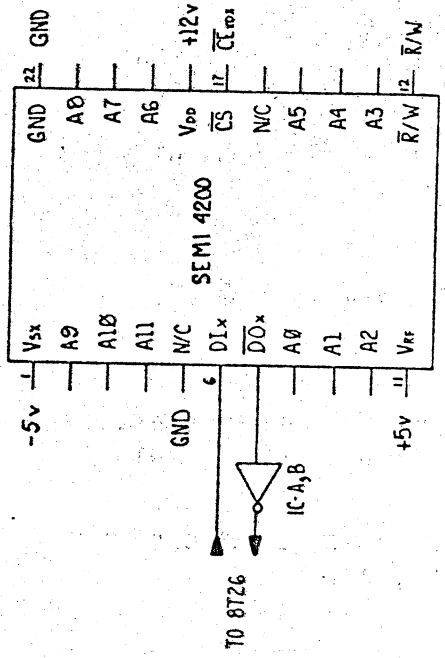
Specifications:

Mechanical: 8" X 10" G-10 Dougle-Sided Plated Through Hole Board

Electrical: Power consumption is dependent upon the power type and speed type of the 2114 memories.

Other Features: Can be populated at 4K, 8K, or 16K with single or dual ports.

NOTES:
1. BOARD IS NORMALLY CO
FIGURED FOR SEMI 4200
FOR USE WITH NEC μPD
CUT FOIL TO PIN 12 A
PIN 17 AND JUMPER
INDICATED. SEE OVERL
2. A0-A11 CONNECTED T
BUFFERED ADDRESS LIN
SEE DIAGRAM 1.



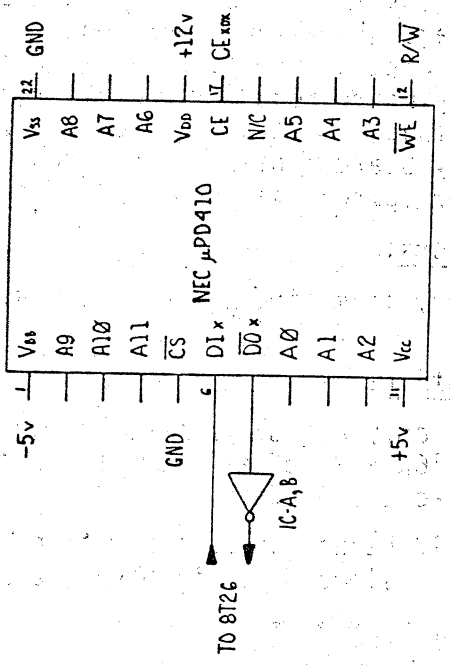


DIAGRAM 2 - MEMORY IMPLEMENTATION

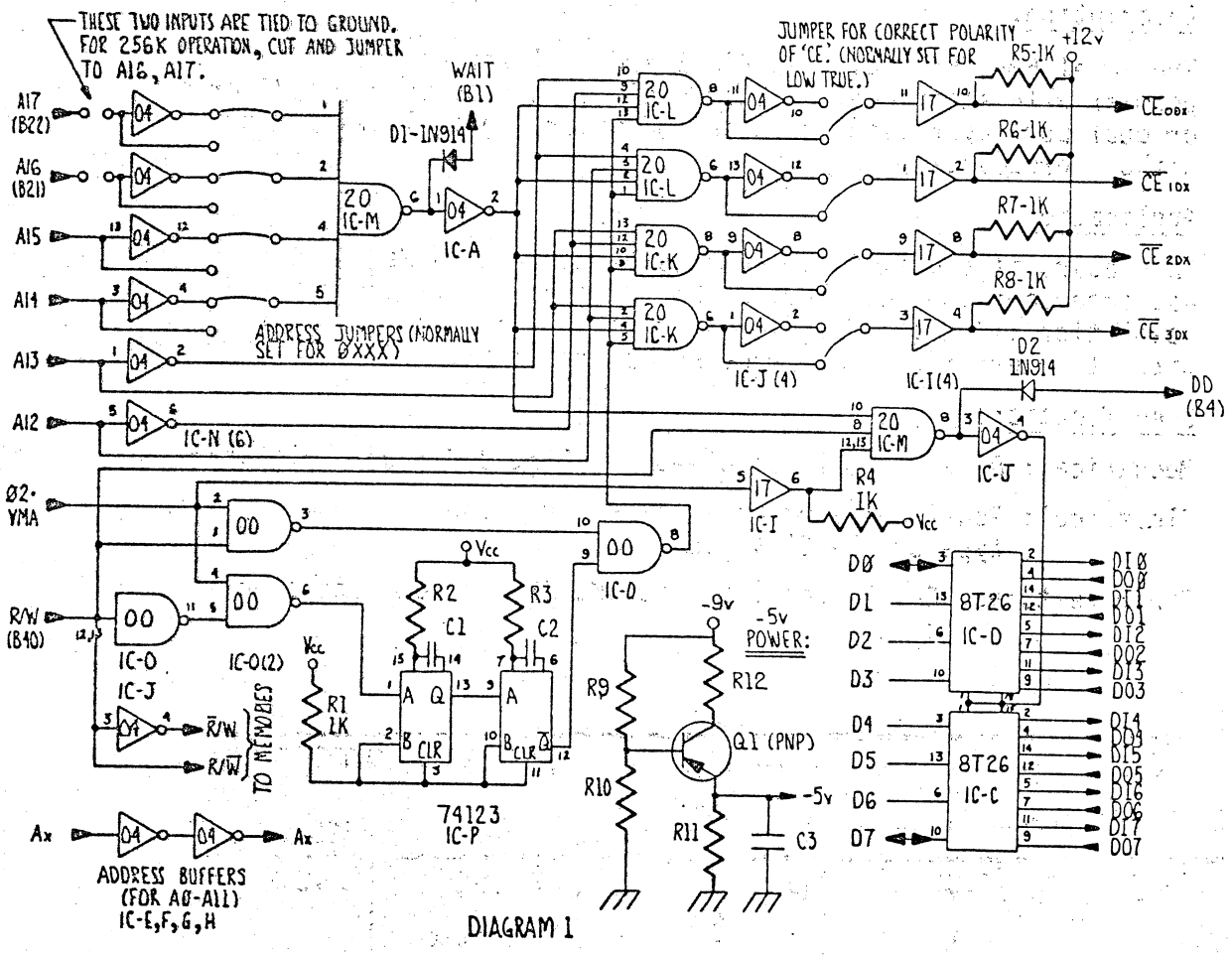
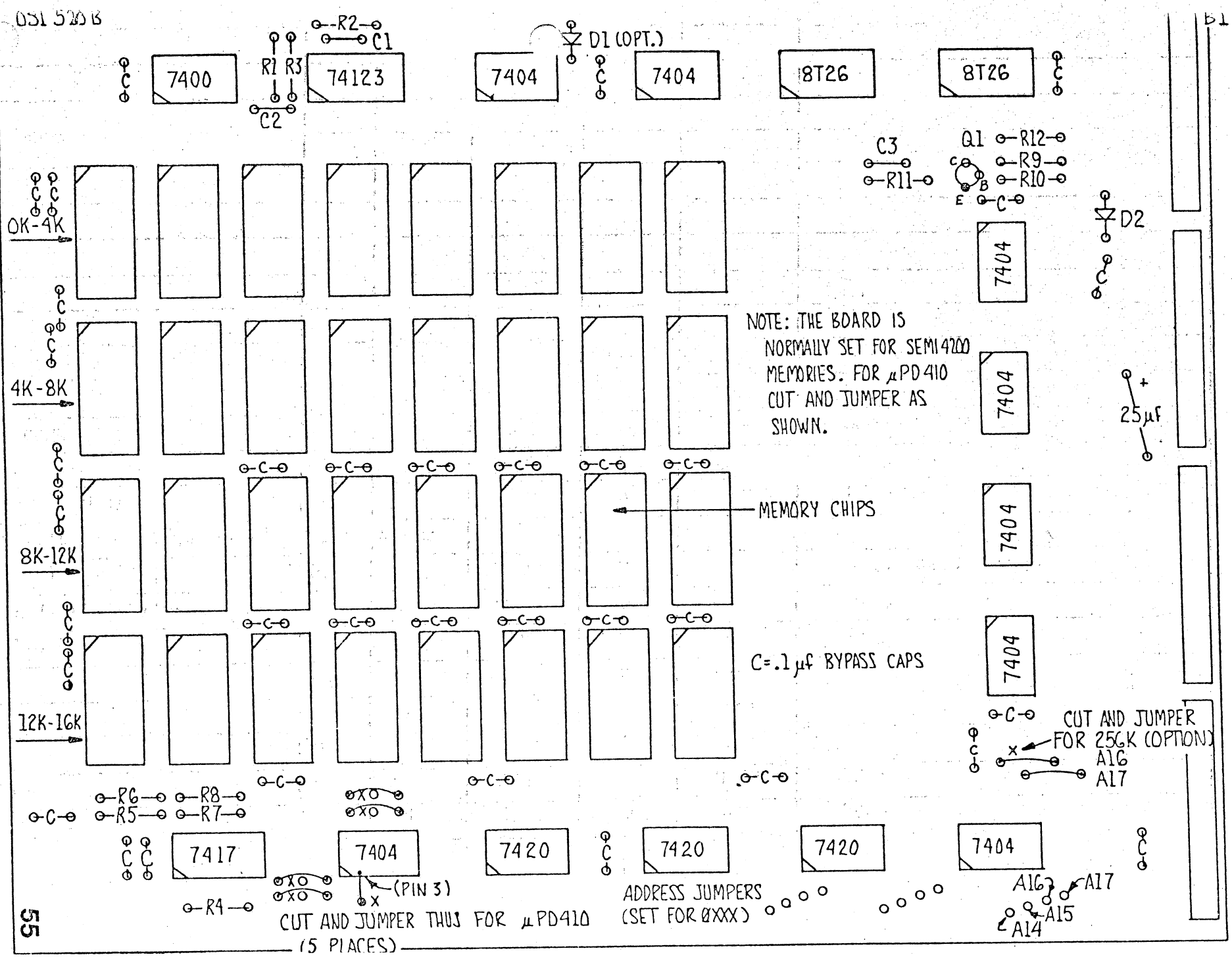


DIAGRAM 1


7400
74123
7404
7404
8T26
8T26
R1
R2
R3
C1
C2
D1 (OPT.)
C3
Q1
R12
R9
R10
R11
D2
0K-4K
4K-8K
8K-12K
12K-16K
NOTE: THE BOARD IS NORMALLY SET FOR SEMI 4200 MEMORIES. FOR μPD410 CUT AND JUMPER AS SHOWN.
MEMORY CHIPS
C=.1 μf BYPASS CAPS
25μf
CUT AND JUMPER FOR 256K (OPTION)
A16
A17
R6
R8
R5
R7
7417
7404
7420
7420
7404
(PIN 3)
R4
CUT AND JUMPER THUS FOR μPD410 (5 PLACES)
ADDRESS JUMPERS (SET FOR 0XXX)
A16
A17
A15
A14
55

DISK Challenger III Utilities
DIRECTORY

PAGE_____
DATE_____

#1	#2	#3	#4	#5	#6	#7
Program	Track	Sector or Format	Start of Transfer	Length in Pages	Go Address	Comments
Modified OS-65 V2.0	00	1	2180	A	2500	6502
Disk Copy	01	1	0200	5	0200	6502
Filler	02	1	----	5	----	
Filler	03	1	----	5	----	
Filler	04	1	----	5	----	
Modified I/O drivers	05	1	2200	3	----	6502
Modified File Controller	06	1	2B30	5	----	6502
Challenger III Utilities	07	1	3D70	3	----	3 processor program
Support utilities outside the operating system						
Challenger III Utilities	08	1	3D70	3	----	Copy of track 7
Mik Bug Simulator	09	1	E000	2	E0D0	6800 program
6800 LOAD/DUMP	10	1	1000	1	----	6800 program